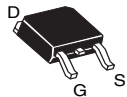


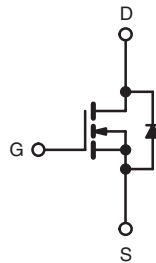
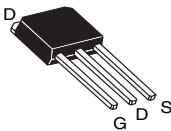
## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	250
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$   2.0
$Q_g$ (Max.) (nC)	8.2
$Q_{gs}$ (nC)	1.8
$Q_{gd}$ (nC)	4.5
Configuration	Single

DPAK (TO-252)



IPAK (TO-251)



N-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR9210, SiHFR9210)
- Straight Lead (IRFU9210, SiHFU9210)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available  
**RoHS\***  
 COMPLIANT  
 HALOGEN  
**FREE**  
 Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU, SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHFR214-GE3	SiHFR214TRL-GE3	SiHFR214TR-GE3	SiHFR214TRR-GE3	SiHFU214-GE3
Lead (Pb)-free	IRFR214PbF	IRFR214TRLPbF <sup>a</sup>	IRFR214TRPbF <sup>a</sup>	-	IRFU214PbF
	SiHFR214-E3	SiHFR214TL-E3 <sup>a</sup>	SiHFR214T-E3 <sup>a</sup>	-	SiHFU214-E3
SnPb	IRFR214	-	IRFR214TR <sup>a</sup>	IRFR214TRR <sup>a</sup>	IRFU214
	SiHFR214	-	SiHFR214T <sup>a</sup>	SiHFR214TR <sup>a</sup>	SiHFU214

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	250	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	2.2	
		$T_C = 100\text{ }^\circ\text{C}$	1.4	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	8.8	A	
Linear Derating Factor		0.20		
Linear Derating Factor (PCB Mount) <sup>e</sup>		0.020	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	190	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	2.2	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	2.5	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	25	W
Maximum Power Dissipation (PCB Mount) <sup>e</sup>	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	2.5	W
Peak Diode Recovery $dV/dt^c$	$dV/dt$	4.8	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	260 <sup>d</sup>		

#### Notes



- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 62\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 2.2\text{ A}$ ,  $dI/dt \leq 65\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 Material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	5.0		

### Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	0.39	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.3\text{ A}^b$	-	-	2.0	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 1.3\text{ A}$		0.80	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$ , see fig. 5		-	140	-	pF
Output Capacitance	$C_{oss}$			-	42	-	
Reverse Transfer Capacitance	$C_{rss}$			-	9.6	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 2.7\text{ A}, V_{DS} = 200\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	8.2	nC
Gate-Source Charge	$Q_{GS}$			-	-	1.8	
Gate-Drain Charge	$Q_{GD}$			-	-	4.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 2.7\text{ A}, R_G = 24\text{ }\Omega, R_D = 45\text{ }\Omega$ , see fig. 10 <sup>b</sup>		-	7.0	-	ns
Rise Time	$t_r$			-	7.6	-	
Turn-Off Delay Time	$t_{d(off)}$			-	16	-	
Fall Time	$t_f$			-	7.0	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	8.8	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.2\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.7\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	190	390	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.65	1.3	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

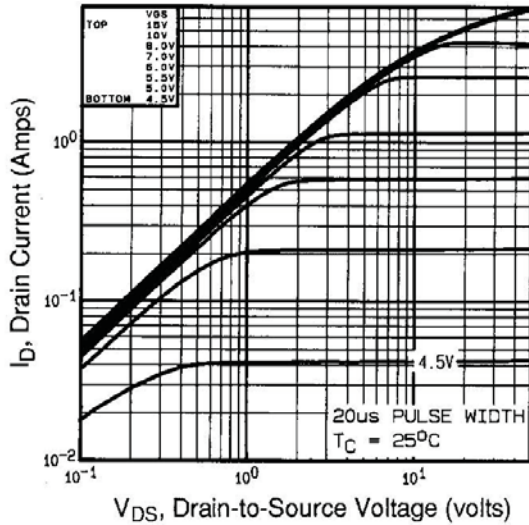


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

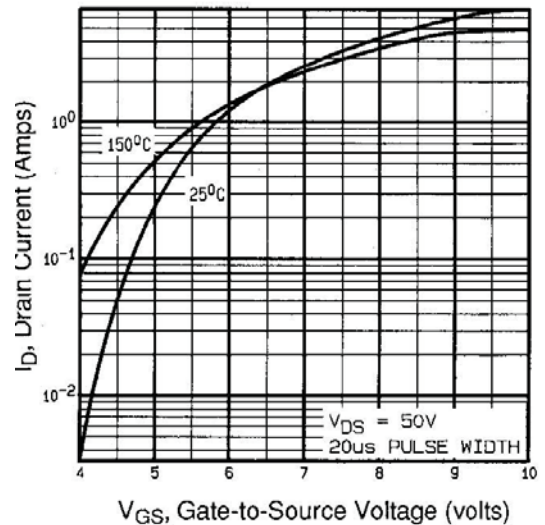


Fig. 3 - Typical Transfer Characteristics

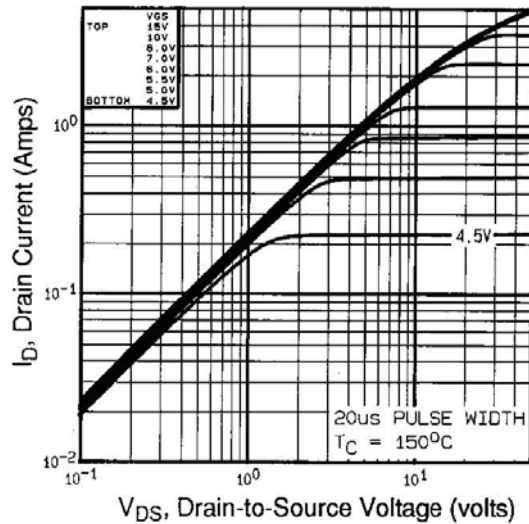


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

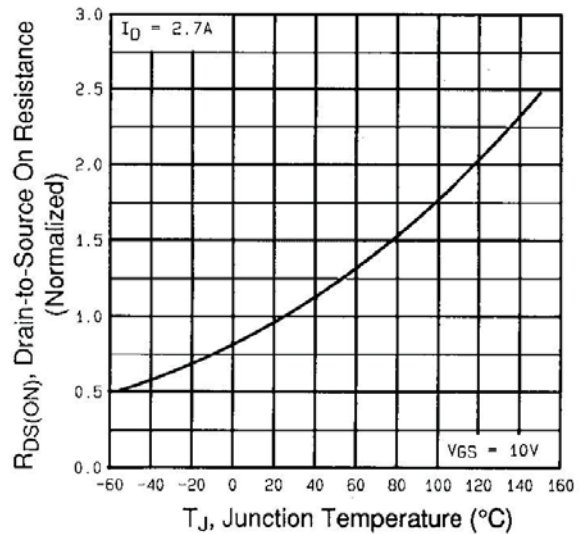


Fig. 4 - Normalized On-Resistance vs. Temperature

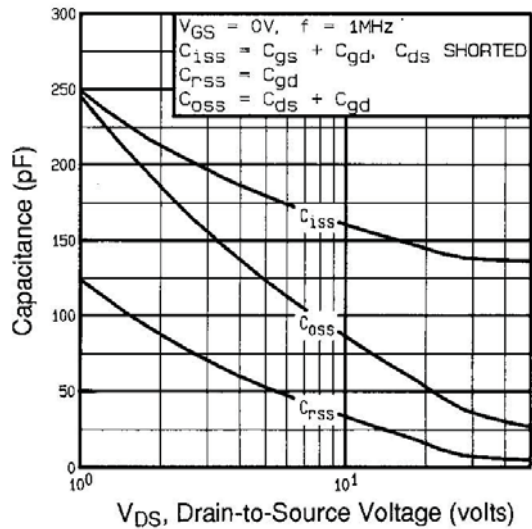


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

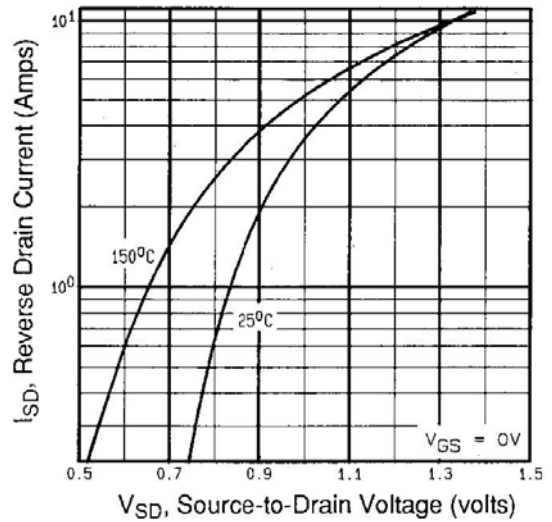


Fig. 7 - Typical Source-Drain Diode Forward Voltage

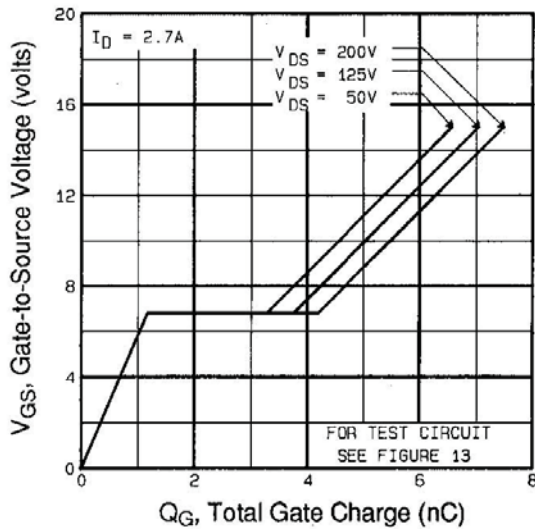


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

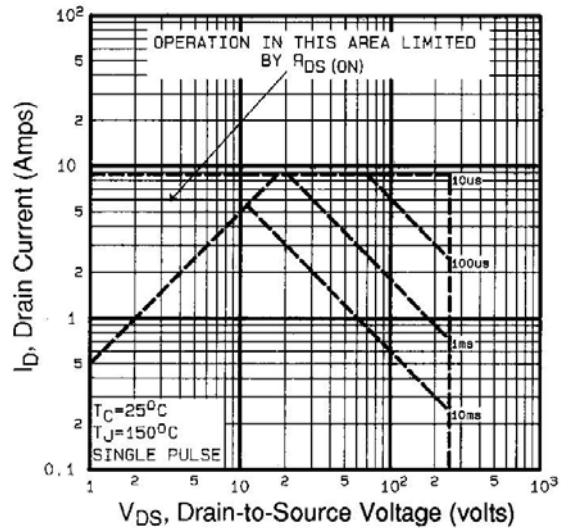


Fig. 8 - Maximum Safe Operating Area

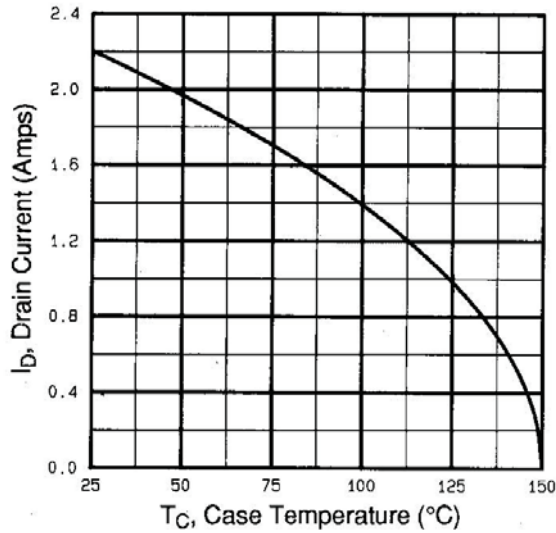


Fig. 9 - Maximum Drain Current vs. Case Temperature

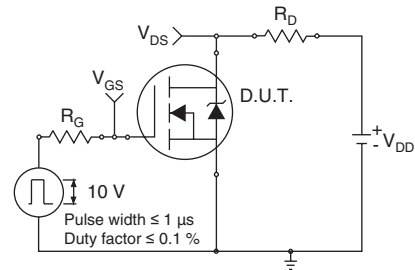


Fig. 10a - Switching Time Test Circuit

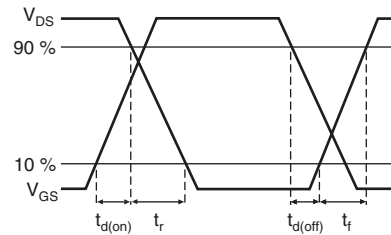


Fig. 10b - Switching Time Waveforms

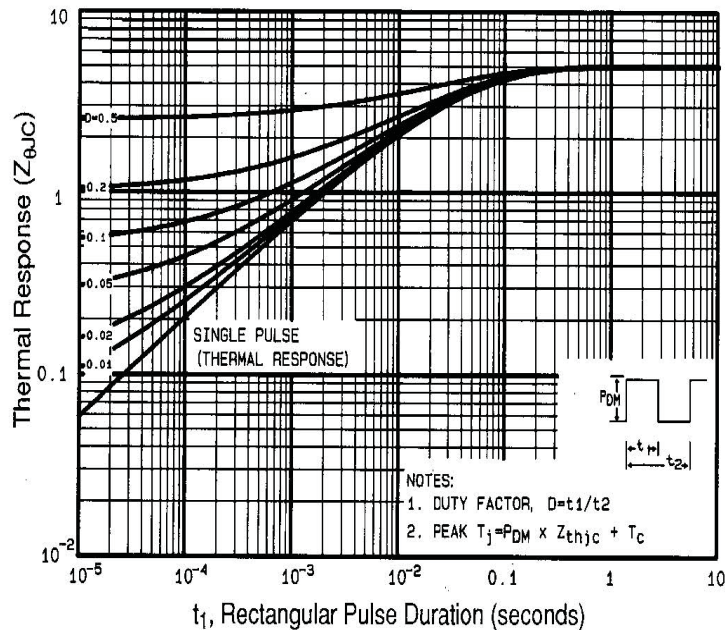


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

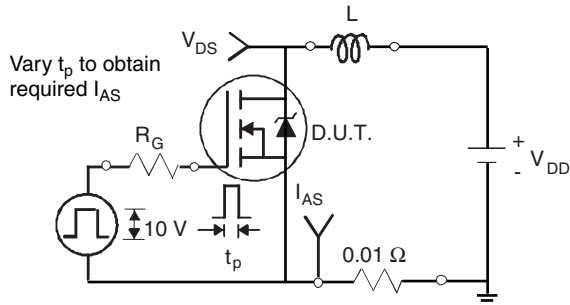


Fig. 12a - Unclamped Inductive Test Circuit

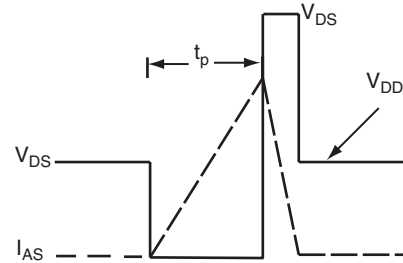


Fig. 12b - Unclamped Inductive Waveforms

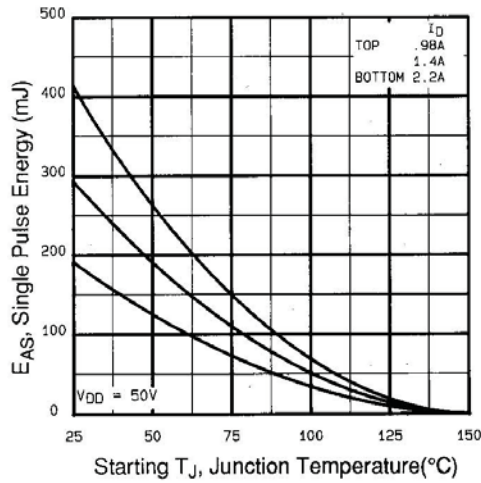


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

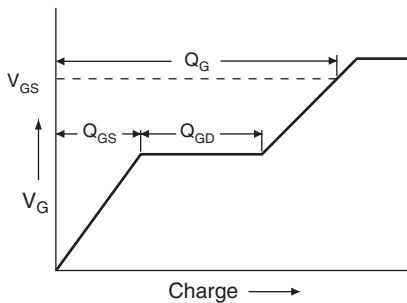


Fig. 13a - Basic Gate Charge Waveform

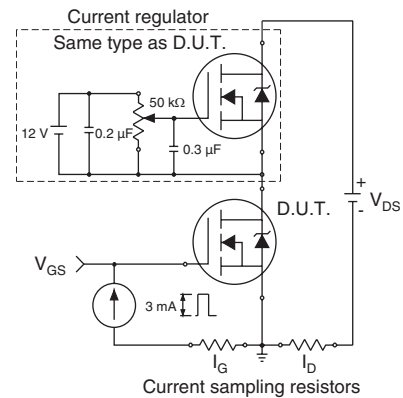
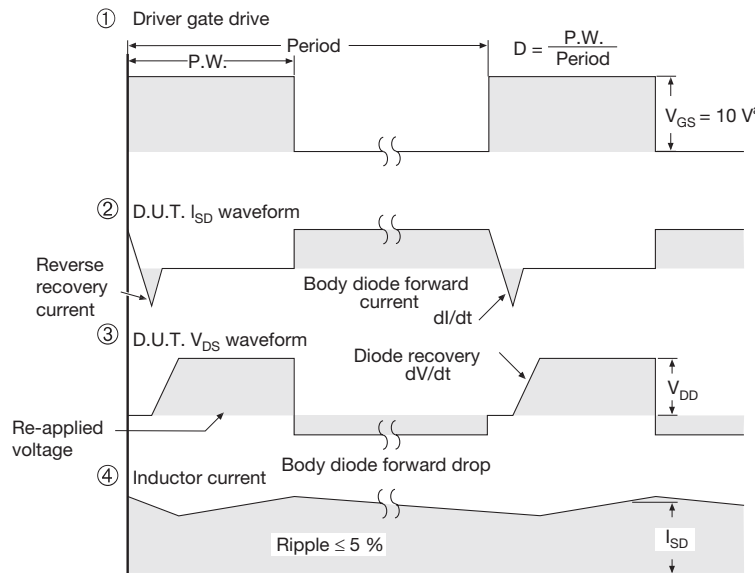
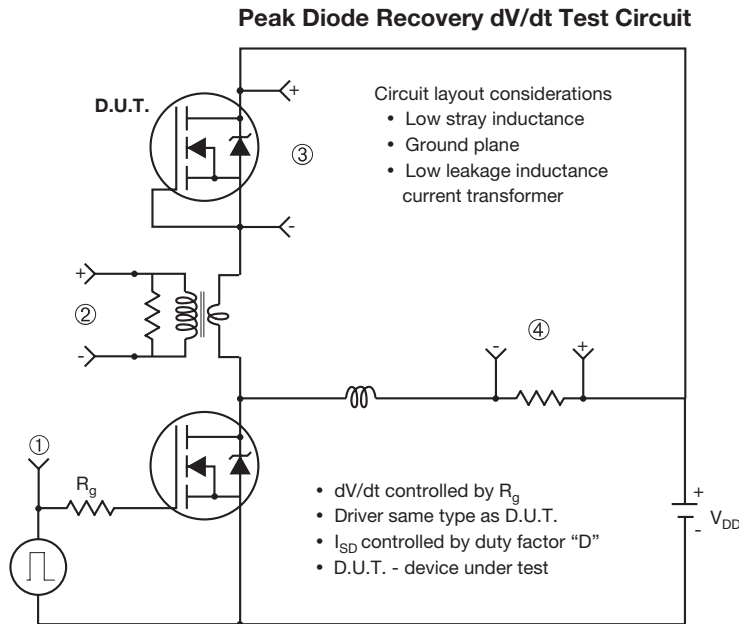


Fig. 13b - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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