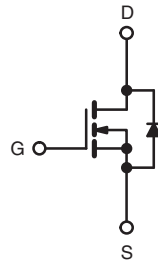
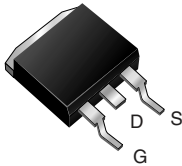


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	250	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.28
$Q_g$ (Max.) (nC)	68	
$Q_{gs}$ (nC)	11	
$Q_{gd}$ (nC)	35	
Configuration	Single	

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF644S-GE3	SiHF644STRL-GE3 <sup>a</sup>	SiHF644STRR-GE3 <sup>a</sup>
Lead (Pb)-free	IRF644SPbF	IRF644STRLPbF <sup>a</sup>	IRF644STRRPbF <sup>a</sup>
	SiHF644S-E3	SiHF644STL-E3 <sup>a</sup>	SiHF644STR-E3 <sup>a</sup>
SnPb	IRF644S	IRF644STRL <sup>a</sup>	IRF644STRR <sup>a</sup>
	SiHF644S	SiHF644STL <sup>a</sup>	SiHF644STR <sup>a</sup>

**Note**

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		250	V
Gate-Source Voltage	$V_{GS}$		$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	14	A
		$T_C = 100$ °C	8.5	
Pulsed Drain Current <sup>a</sup>			56	W/°C
Linear Derating Factor			1.0	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.025	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		550	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$		14	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		13	mJ
Maximum Power Dissipation	$T_C = 25$ °C		125	W
	$T_A = 25$ °C		3.1	

\* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	4.8	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

**Notes**

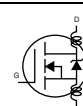
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 4.5 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 14 A (see fig. 12).
- c. I<sub>SD</sub> ≤ 14 A, dI/dt ≤ 150 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- d. 1.6 mm from case.
- e. When mounted on 1" square PCB (FR-4 or G-10 material).


THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	R <sub>thJA</sub>	-	40	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0	

**Note**

- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	250	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.34	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V	-	-	25	μA
		V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 8.4 A <sup>b</sup>	-	-	0.28	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 8.4 A <sup>b</sup>	6.7	-	-	S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5	-	1300	-	pF
Output Capacitance	C <sub>oss</sub>		-	330	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	85	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 7.9 A, V <sub>DS</sub> = 200 V, see fig. 6 and 13 <sup>b</sup>	-	-	68	nC
Gate-Source Charge	Q <sub>gs</sub>		-	-	11	
Gate-Drain Charge	Q <sub>gd</sub>		-	-	35	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 7.9 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 8.7 Ω, see fig. 10 <sup>b</sup>	-	11	-	ns
Rise Time	t <sub>r</sub>		-	24	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	53	-	
Fall Time	t <sub>f</sub>		-	49	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH
Internal Source Inductance	L <sub>S</sub>		-	7.5	-	



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 14\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.8	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 7.9\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	250	500	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	2.3	4.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** ( $25\text{ }^\circ\text{C}$ , unless otherwise noted)

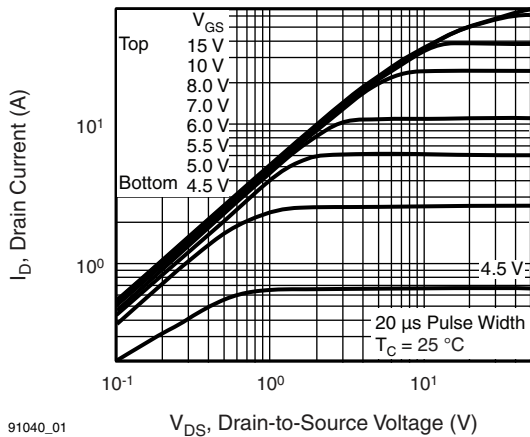


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$

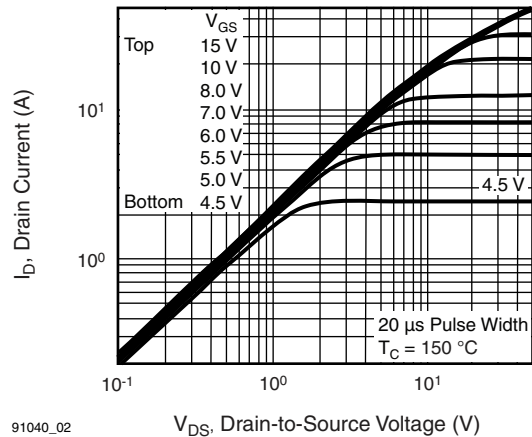


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$

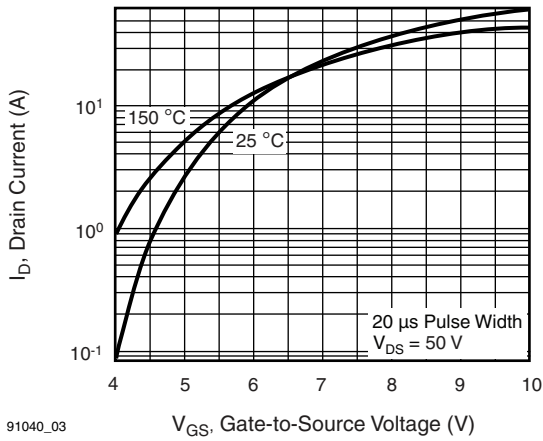


Fig. 3 - Typical Transfer Characteristics

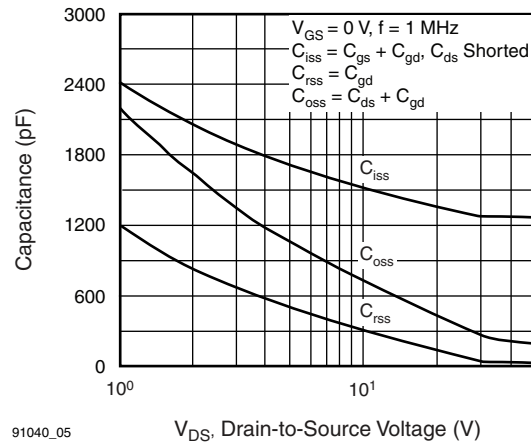


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

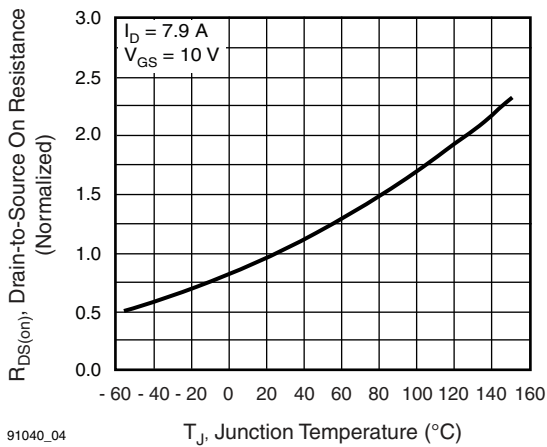


Fig. 4 - Normalized On-Resistance vs. Temperature

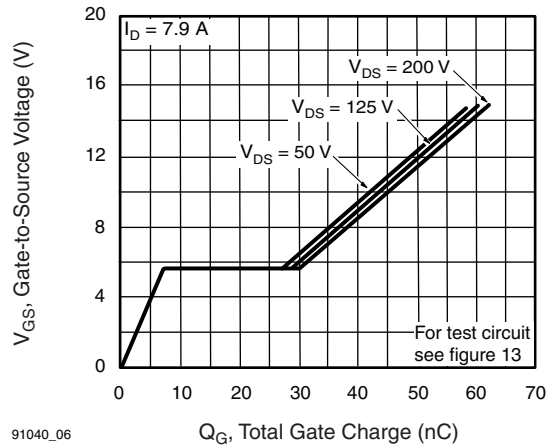
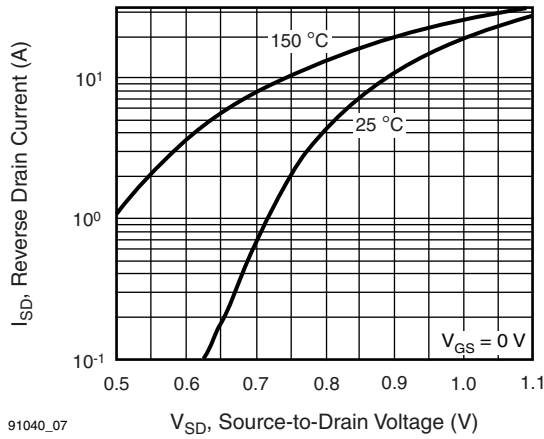
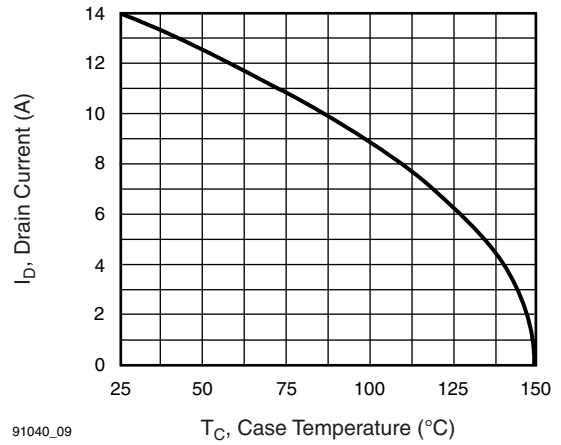


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



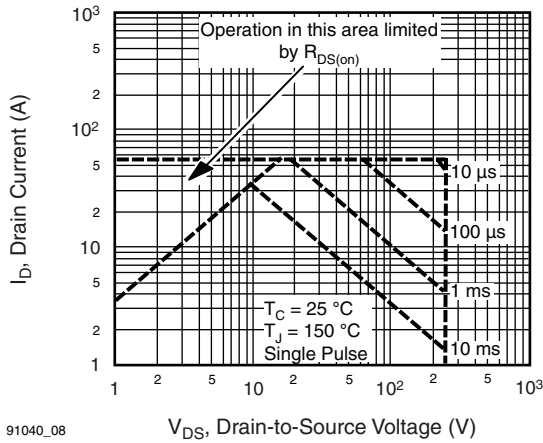
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**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



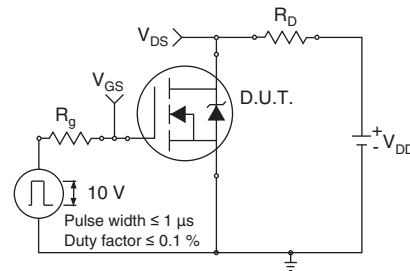
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**Fig. 9 - Maximum Drain Current vs. Case Temperature**

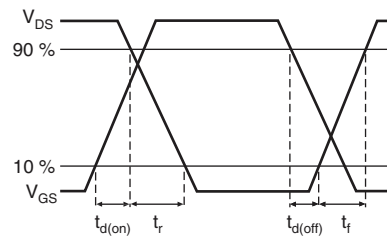


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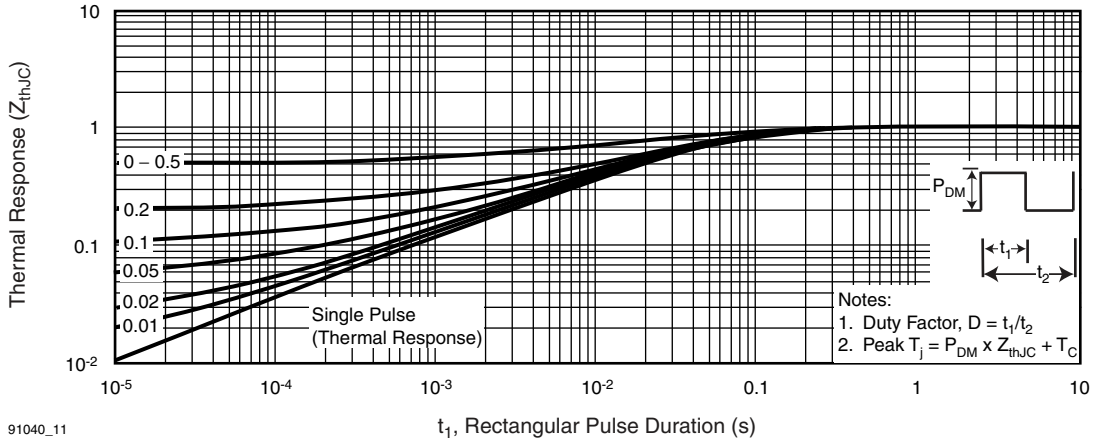
**Fig. 8 - Maximum Safe Operating Area**



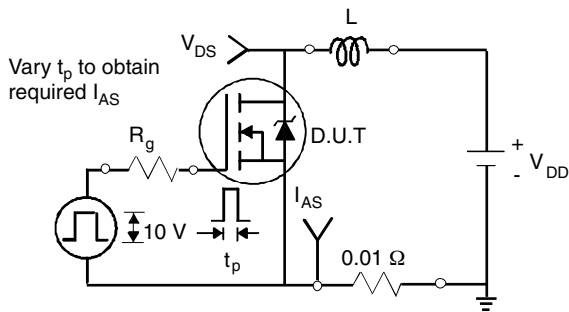
**Fig. 10a - Switching Time Test Circuit**



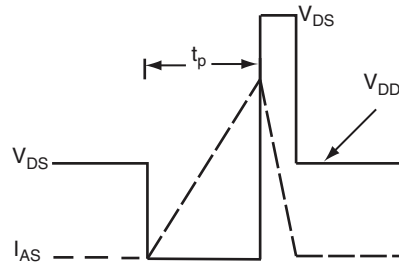
**Fig. 10b - Switching Time Waveforms**



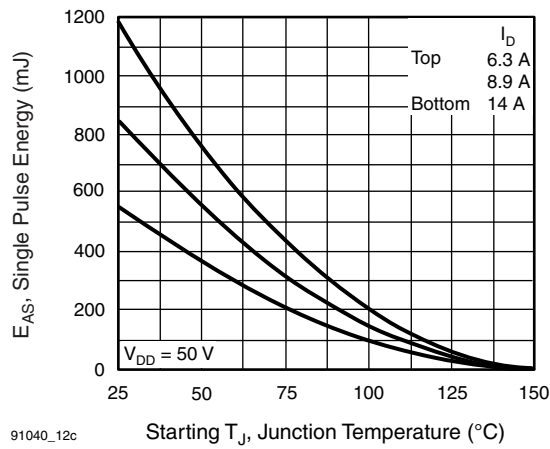
**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**



**Fig. 12a - Unclamped Inductive Test Circuit**



**Fig. 12b - Unclamped Inductive Waveforms**



**Fig. 13 - Maximum Avalanche Energy vs. Drain Current**

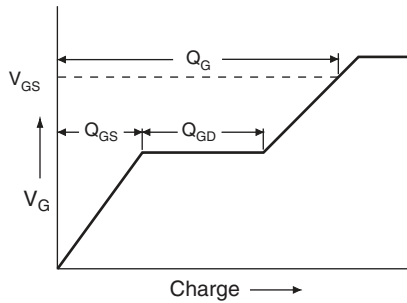


Fig. 13a - Basic Gate Charge Waveform

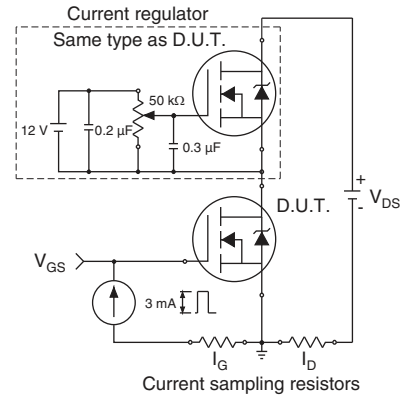
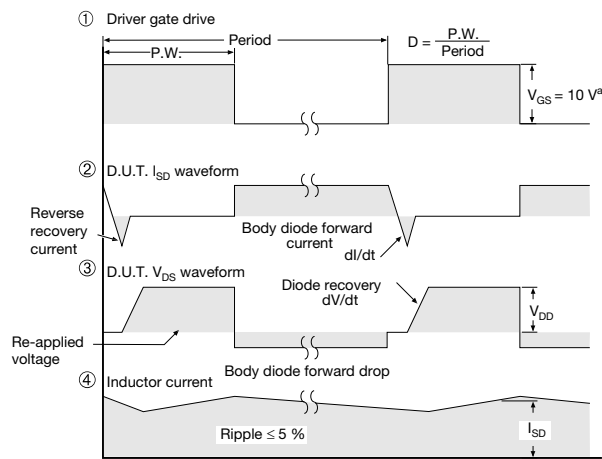
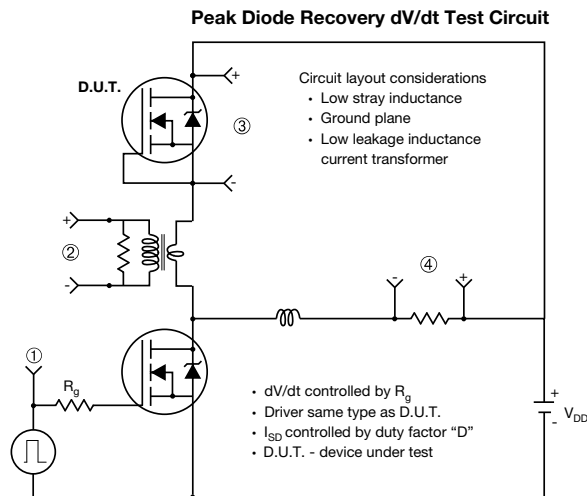


Fig. 13b - Gate Charge Test Circuit



Note  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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