



### N- and P-Channel 30-V (D-S) MOSFET

#### CHARACTERISTICS

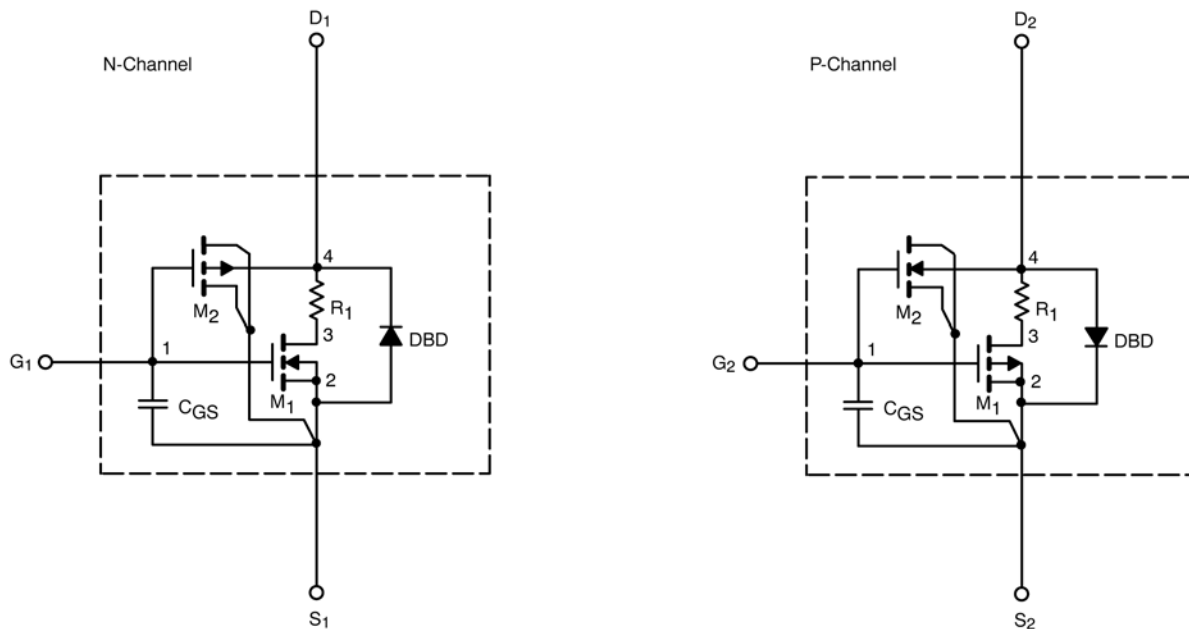
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Typical	Unit	
<b>Static</b>					
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V, V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1.9	V
		V <sub>DS</sub> = V, V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	2.13	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	N-Ch	51	A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -10 V	P-Ch	24	
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.5 A	N-Ch	0.090	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.8 A	P-Ch	0.177	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.0 A	N-Ch	0.134	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.2 A	P-Ch	0.281	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.5 A	N-Ch	4.3	S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1.2 A	P-Ch	2.5	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.05 A, V <sub>GS</sub> = 0 V	N-Ch	0.81	V
		I <sub>S</sub> = -1.05 V, V <sub>GS</sub> = 0 V	P-Ch	-0.81	
<b>Dynamic<sup>b</sup></b>					
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1.8 A P-Channel V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -5 V, I <sub>D</sub> = -1.8 A	N-Ch	2	nC
Gate-Source Charge	Q <sub>gs</sub>		P-Ch	2.4	
			N-Ch	0.7	
Gate-Drain Charge	Q <sub>gd</sub>		P-Ch	0.9	
			N-Ch	0.7	
Turn-On Delay Time	t <sub>d(on)</sub>		P-Ch	0.8	
		N-Ch	7		
Rise Time	t <sub>r</sub>	N-Channel V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω	N-Ch	8	ns
		Turn-Off Delay Time	t <sub>d(off)</sub>	N-Ch	
Fall Time	t <sub>f</sub>			P-Channel V <sub>DD</sub> = -15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 6 Ω	
		Source-Drain Reverse Recovery Time	t <sub>rr</sub>	N-Ch	
N-Ch	11				
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	N-Ch	14		
		P-Ch	12		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = A, I <sub>S</sub> = 1.05A, di/dt = 100 A/μs	N-Ch	35	
		I <sub>F</sub> = A, I <sub>S</sub> = -1.05A, di/dt = 100 A/μs	P-Ch	31	

**Notes**

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

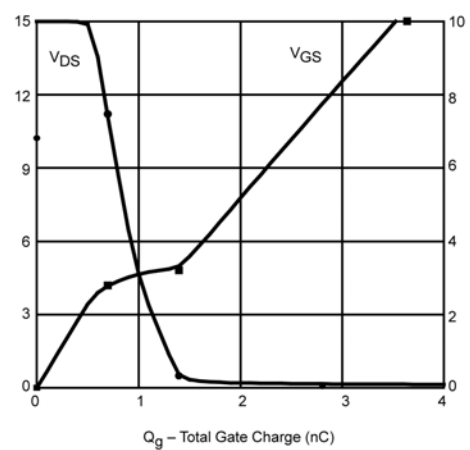
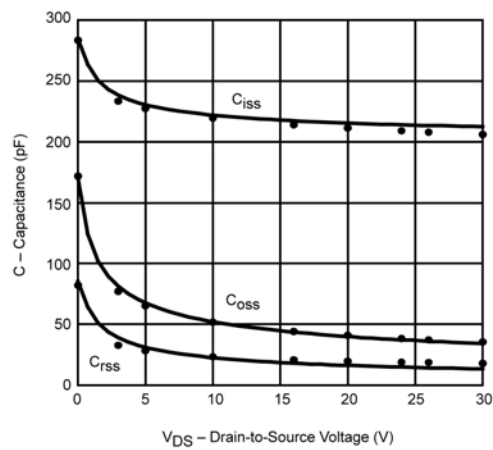
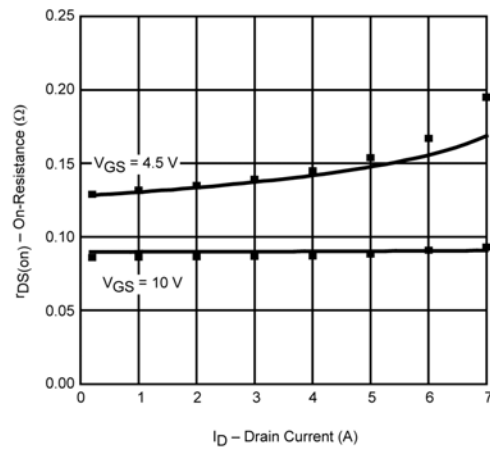
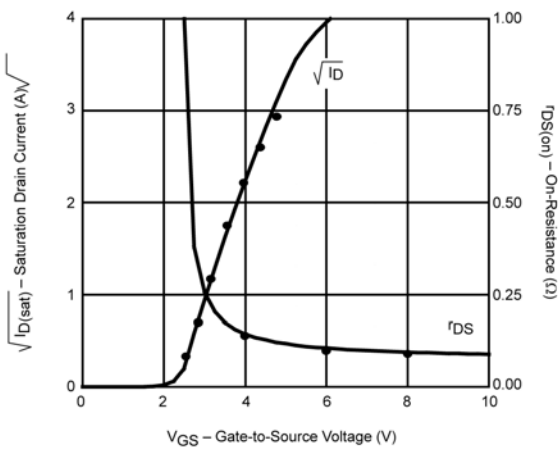
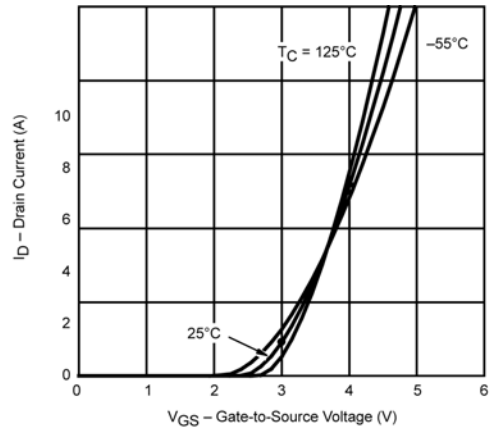
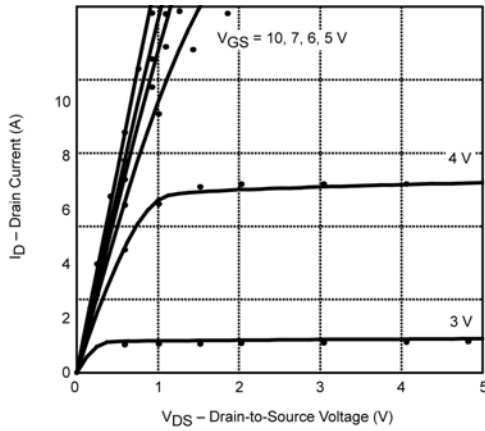


# SPICE Device Model Si3552DV

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

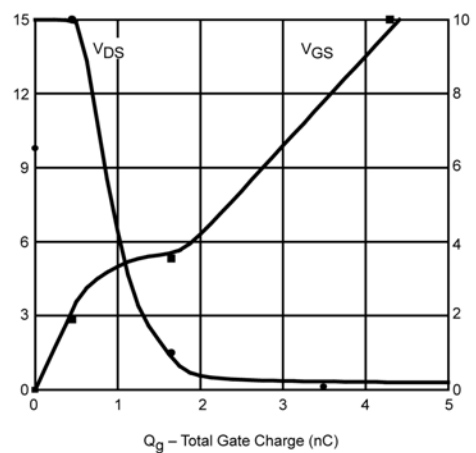
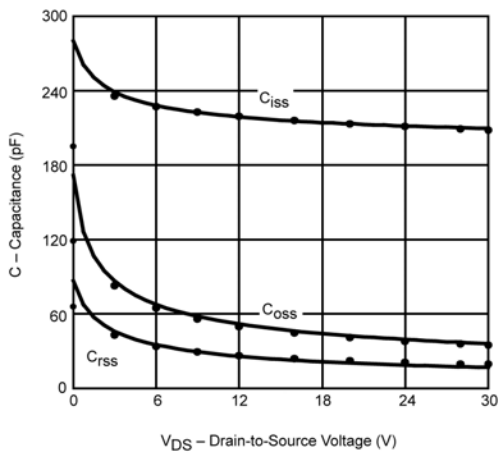
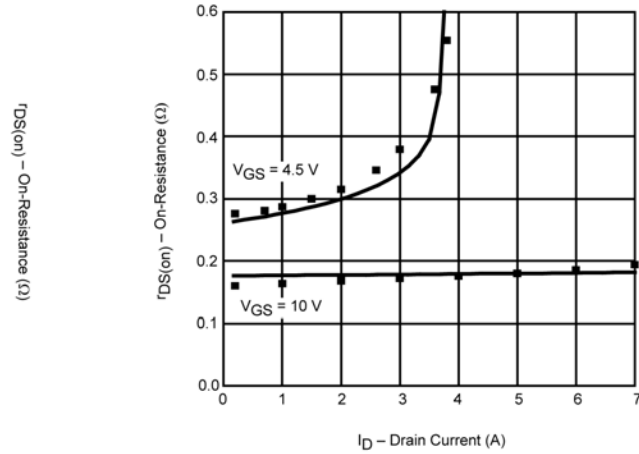
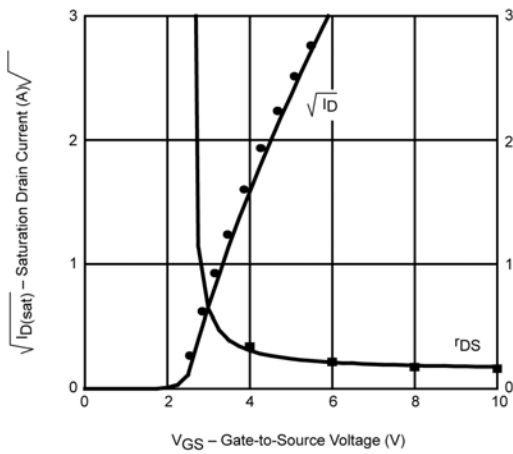
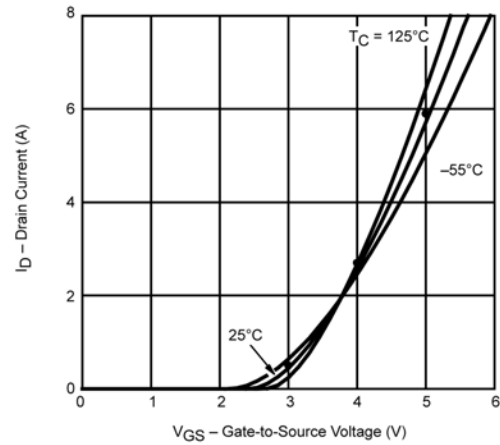
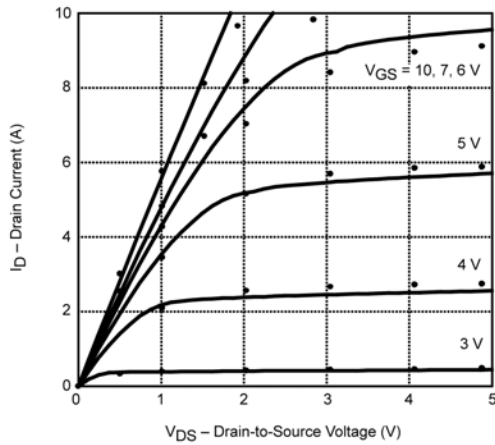
### N-Channel MOSFET



Note: Dots and squares represent measured data.



### P-Channel MOSFET



Note: Dots and squares represent measured data.



## Disclaimer

All product specifications and data are subject to change without notice.

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