ATF-521P8

High Linearity Enhancement Mode [1] Pseudomorphic HEMT in 2x2 mm^2 LPCC[3] Package

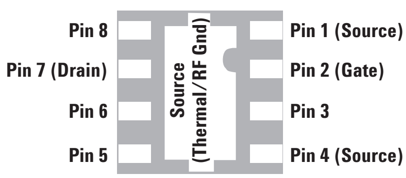
Data Sheet

Description

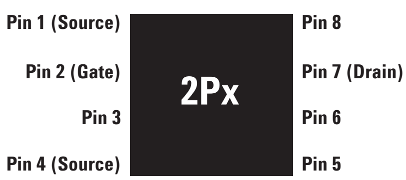
Avago Technologies' ATF-521P8 is a single-voltage high linearity, low noise E-pHEMT housed in an 8-lead JEDEC-standard leadless plastic chip carrier (LPCC[3]) package. The device is ideal as a medium-power, high-linearity amplifier. Its operating frequency range is from 50 MHz to 6 GHz.

The thermally efficient package measures only 2mm x 2mm x 0.75mm. Its backside metalization provides excellent thermal dissipation as well as visual evidence of solder reflow. The device has a Point MTTF of over 300 years at a mounting temperature of +85°C. All devices are 100% RF & DC tested.

Pin Connections and Package Marking



Bottom View



Top View

Note:
Package marking provides orientation and identification
"2P" = Device Code
"x" = Month code indicates the month of manufacture.

Note:
1. Enhancement mode technology employs a single positive V_{gs}, eliminating the need of negative gate voltage associated with conventional depletion mode devices.
2. Refer to reliability datasheet for detailed MTTF data
3. Conform to JEDEC reference outline MO229 for DRP-N
4. Linearity Figure of Merit (LFOM) is essentially OIP3 divided by DC bias power.

Features

- Single voltage operation
- High linearity and P1dB
- Low noise figure
- Excellent uniformity in product specifications
- Small package size: 2.0 x 2.0 x 0.75 mm^3
- Point MTTF > 300 years[2]
- MSL-1 and lead-free
- Tape-and-reel packaging option available

Specifications

- 2 GHz; 4.5V, 200 mA (Typ.)
- 42 dBm output IP3
- 26.5 dBm output power at 1 dB gain compression
- 1.5 dB noise figure
- 17 dB Gain
- 12.5 dB LFOM[4]

Applications

- Front-end LNA Q2 and Q3, driver or pre-driver amplifier for Cellular/PCS and WCDMA wireless infrastructure
- Driver amplifier for WLAN, WLL/RLL and MMDS applications
- General purpose discrete E-pHEMT for other high linearity applications

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A)
ESD Human Body Model (Class 1C)
Refer to Avago Technologies Application Note A004R: Electrostatic Discharge Damage and Control.

ATF-521P8 Absolute Maximum Ratings [1]

Symbol	Parameter	Units	Absolute Maximum
V_{DS}	Drain – Source Voltage [2]	V	7
V_{GS}	Gate –Source Voltage [2]	V	-5 to 1
V_{GD}	Gate Drain Voltage [2]	V	-5 to 1
I_{DS}	Drain Current [2]	mA	500
I_{GS}	Gate Current	mA	46
P_{diss}	Total Power Dissipation [3]	W	1.5
$P_{in\ max.}$	RF Input Power	dBm	27
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150
θ_{ch_b}	Thermal Resistance [4]	°C/W	45

Notes:
1. Operation of this device in excess of any one of these parameters may cause permanent damage.
2. Assumes DC quiescent conditions.
3. Board (package belly) temperature T_B is 25°C. Derate 22 mW/°C for T_B > 83°C.
4. Channel to board thermal resistance measured using 150°C Liquid Crystal Measurement method.
5. Device can safely handle +27dBm RF Input Power provided IGS is limited to 46mA. IGS at P1dB drive level is bias circuit dependent.

Product Consistency Distribution Charts [5, 6]

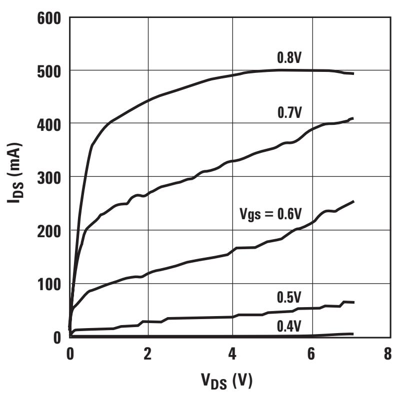


Figure 1. Typical I-V Curves. (V_{GS} = 0.1 V per step)

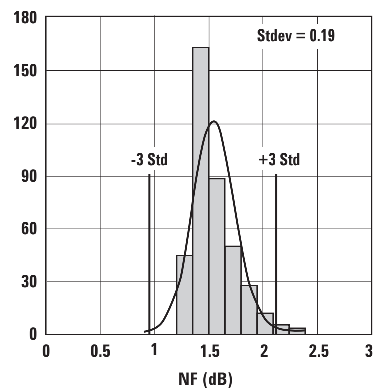


Figure 2. NF @ 2 GHz, 4.5 V, 200 mA. Nominal = 1.5 dB.

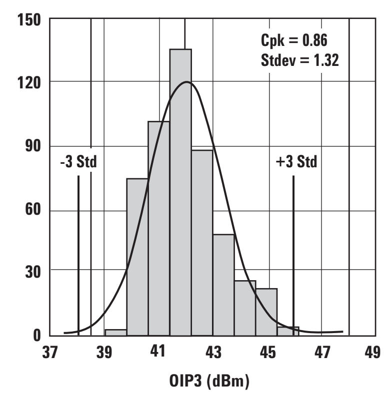


Figure 3. OIP3 @ 2 GHz, 4.5 V, 200 mA. Nominal = 41.9 dBm, LSL = 38.5 dBm.

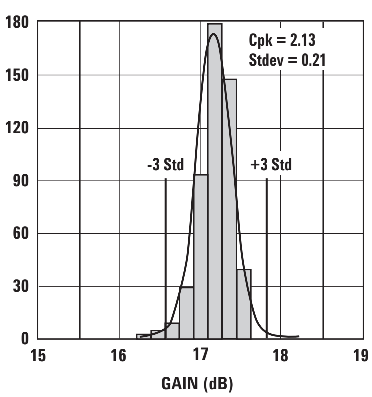


Figure 4. Gain @ 2 GHz, 4.5 V, 200 mA. Nominal = 17.2 dB, LSL = 15.5 dB, USL = 18.5 dB.

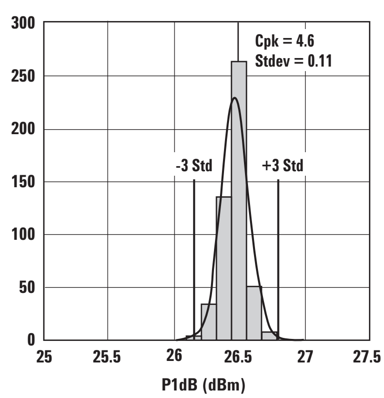


Figure 5. P1dB @ 2 GHz, 4.5 V, 200 mA. Nominal = 26.5 dBm, LSL = 25 dBm.

Notes:
5. Distribution data sample size is 500 samples taken from 5 different wafers. Future wafers allocated to this product may have nominal values anywhere between the upper and lower limits.
6. Measurements are made on production test board, which represents a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

ATF-521P8 Electrical Specifications

T_A = 25°C, DC bias for RF parameters is Vds = 4.5V and Ids = 200 mA unless otherwise specified.

Symbol	Parameter and Test Condition		Units	Min.	Typ.	Max.
Vgs	Operational Gate Voltage	Vds = 4.5V, Ids = 200 mA	V	—	0.62	—
Vth	Threshold Voltage	Vds = 4.5V, Ids = 16 mA	V	—	0.28	—
Idss	Saturated Drain Current	Vds = 4.5V, Vgs = 0V	µA	—	14.8	—
Gm	Transconductance	Vds = 4.5V, Gm = ΔIdss/ΔVgs; Vgs = Vgs1 - Vgs2 Vgs1 = 0.55V, Vgs2 = 0.5V	mmho	—	1300	—
Igss	Gate Leakage Current	Vds = 0V, Vgs = -4V	µA	-20	0.49	—
NF	Noise Figure [1]	f = 2 GHz f = 900 MHz	dB dB	— —	1.5 1.2	— —
G	Gain[1]	f = 2 GHz f = 900 MHz	dB dB	15.5 —	17 17.2	18.5 —
OIP3	Output 3rd Order Intercept Point[1]	f = 2 GHz f = 900 MHz	dBm dBm	38.5 —	42 42.5	— —
P1dB	Output 1dB Compressed[1]	f = 2 GHz f = 900 MHz	dBm dBm	25 —	26.5 26.5	— —
PAE	Power Added Efficiency	f = 2 GHz f = 900 MHz	% %	45 —	60 56	— —
ACLR	Adjacent Channel Leakage Power Ratio[1,2]	Offset BW = 5 MHz Offset BW = 10 MHz	dBc dBc	— —	-51.4 -61.5	— —

Notes:
1. Measurements obtained using production test board described in Figure 6.
2. ACLR test spec is based on 3GPP TS 25.141 V5.3.1 (2002-06)
– Test Model 1
– Active Channels: PCCPCH + SCH + CPICH + PICH + SCCPCH + 64 DPCH (SF=128)
– Freq = 2140 MHz
– Pin = -5 dBm
– Chan Integ Bw = 3.84 MHz

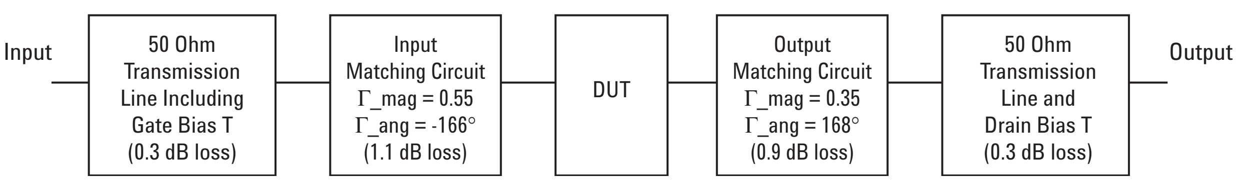


Figure 6. Block diagram of the 2 GHz production test board used for NF, Gain, OIP3 , P1dB and PAE and ACLR measurements. This circuit achieves a trade-off between optimal OIP3, P1dB and VSWR. Circuit losses have been de-embedded from actual measurements.

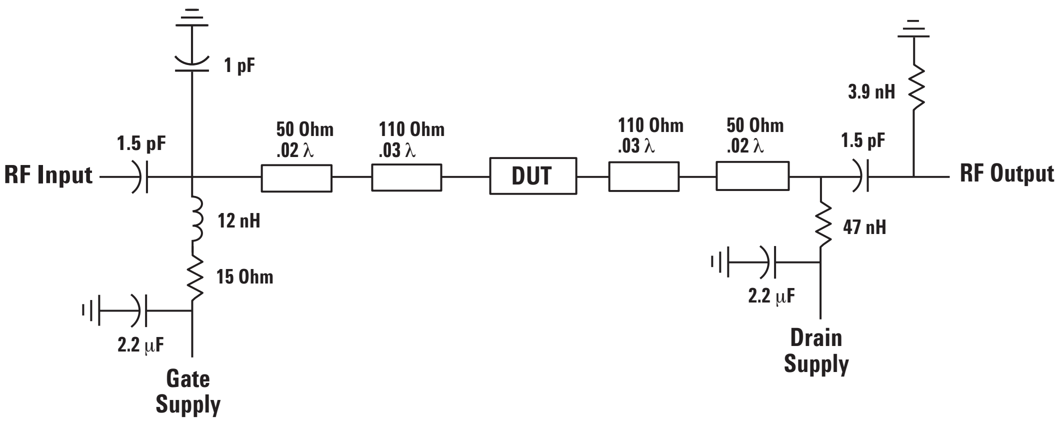


Figure 7. Simplified schematic of production test board. Primary purpose is to show 15 Ohm series resistor placement in gate supply. Transmission line tapers, tee intersections, bias lines and parasitic values are not shown.

Gamma Load and Source at Optimum OIP3 and P1dB Tuning Conditions

The device's optimum OIP3 and P1dB measurements were determined using a Maury load pull system at 4.5V, 200 mA quiesent bias:

	Optimum OIP3							
Freq	Gamma Source		Gamma Load		OIP3	Gain	P1dB	PAE
(GHz)	Mag	Ang (deg)	Mag	Ang (deg)	(dBm)	(dB)	(dBm)	(%)
0.9	0.413	10.5	0.314	179.0	42.7	16.0	27.0	54.0
2	0.368	162.0	0.538	-176.0	42.5	15.8	27.5	55.3
2.4	0.318	169.0	0.566	-169.0	42.0	14.1	27.4	53.5
3.9	0.463	-134.0	0.495	-159.0	40.3	9.6	27.3	43.9

	Optimum P1dB							
Freq	Gamma Source		Gamma Load		OIP3	Gain	P1dB	PAE
(GHz)	Mag	Ang (deg)	Mag	Ang (deg)	(dBm)	(dB)	(dBm)	(%)
0.9	0.587	12.7	0.613	-172.1	39.1	14.5	29.3	49.6
2	0.614	126.1	0.652	-172.5	39.5	12.9	29.3	49.5
2.4	0.649	145.0	0.682	-171.5	40.0	12.0	29.4	46.8
3.9	0.552	-162.8	0.670	-151.2	38.1	9.6	27.9	39.1

ATF-521P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

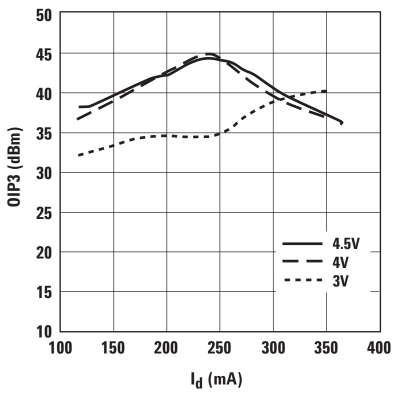


Figure 8. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

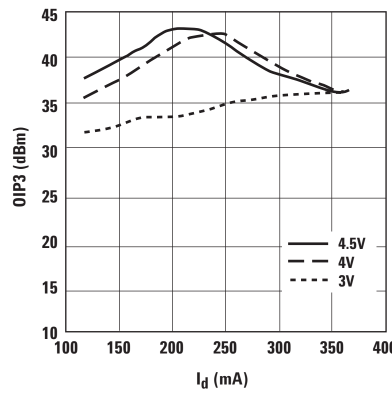


Figure 9. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

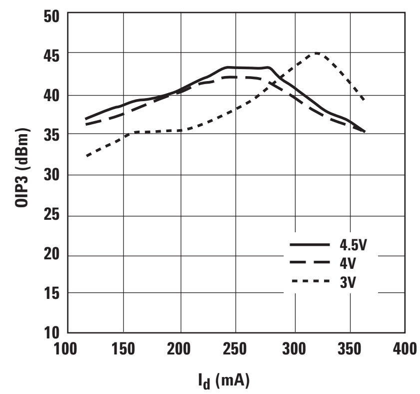


Figure 10. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

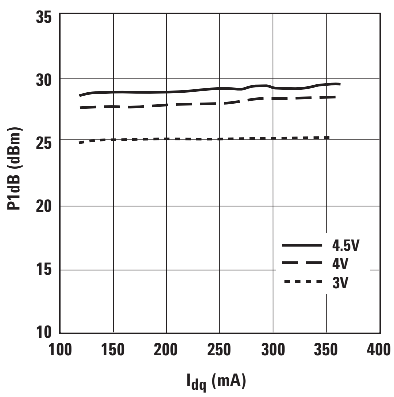


Figure 11. P1dB vs. I_{dq} and V_{ds} at 2 GHz.

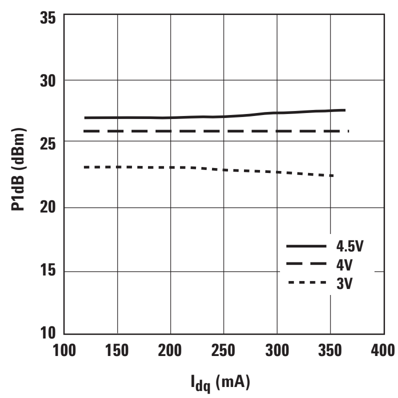


Figure 12. P1dB vs. I_{dq} and V_{ds} at 900 MHz.

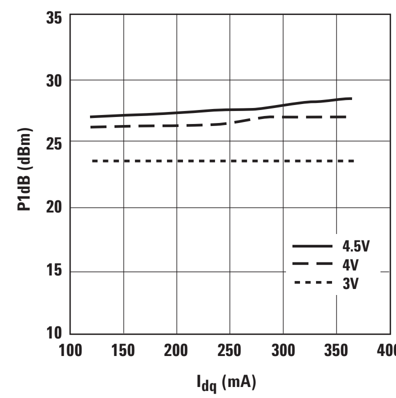


Figure 13. P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

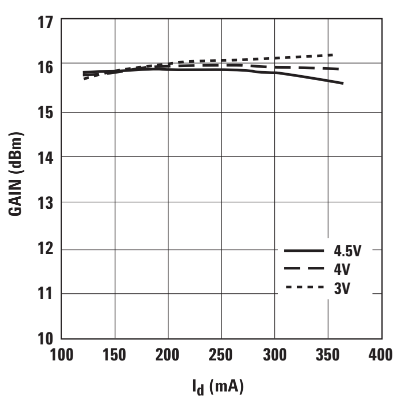


Figure 14. Small Signal Gain vs I_{ds} and V_{ds} at 2 GHz.

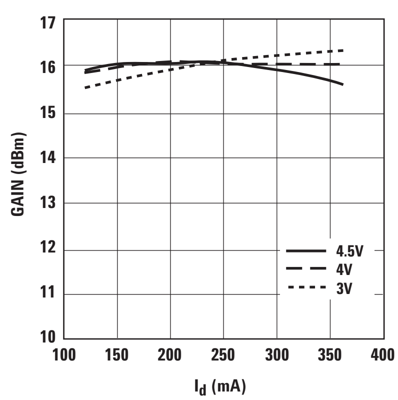


Figure 15. Small Signal Gain vs I_{ds} and V_{ds} at 900 MHz.

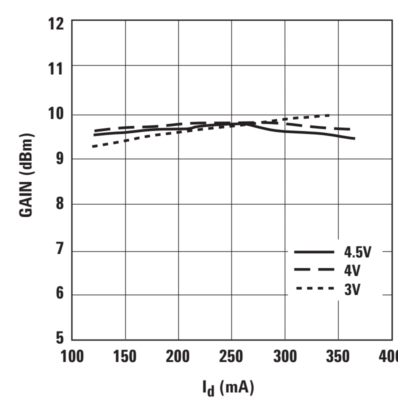


Figure 16. Small Signal Gain vs I_{ds} and V_{ds} at 3.9 GHz.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)
Tuned for Optimal OIP3

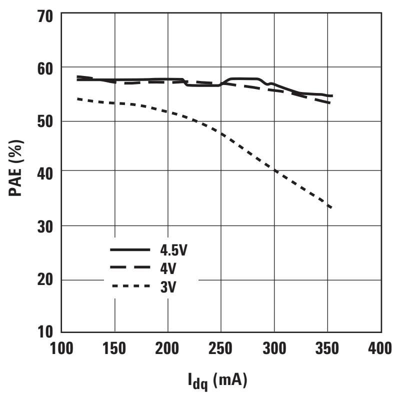


Figure 17. PAE @ P1dB vs. I_{dq} and V_{ds} at 2 GHz.

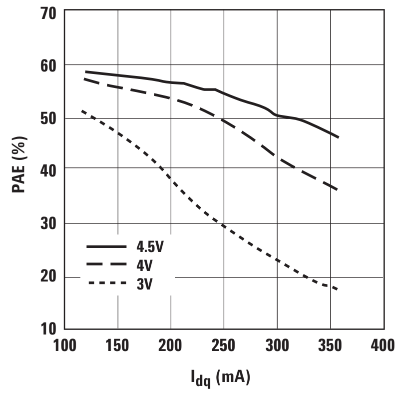


Figure 18. PAE @ P1dB vs. I_{dq} and V_{ds} at 900 MHz.

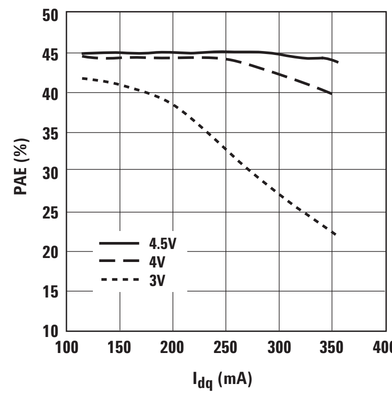


Figure 19. PAE @ P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

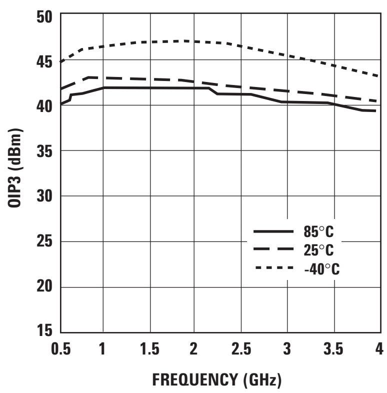


Figure 20. OIP3 vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

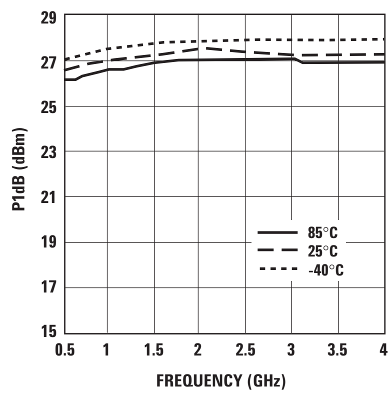


Figure 21. P1dB vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

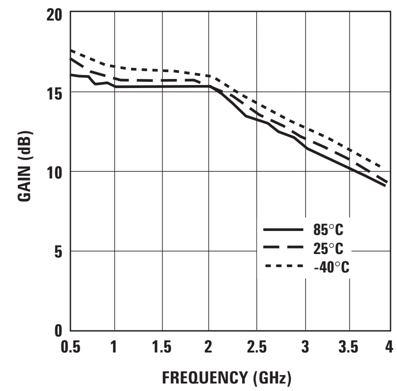


Figure 22. Gain vs. Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

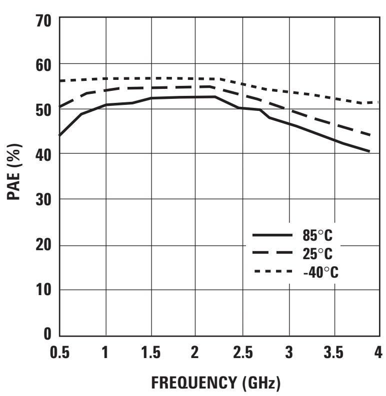


Figure 23. PAE vs Temp and Freq tuned for optimal OIP3 at 4.5V, 200 mA.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Performance Curves (at 25°C unless specified otherwise)
Tuned for Optimal P1dB

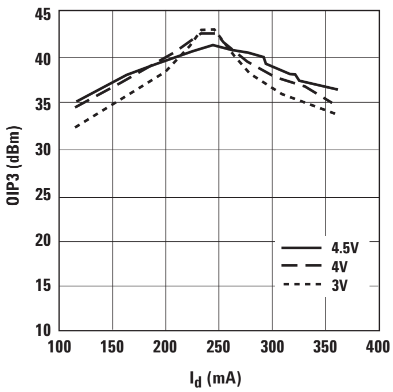


Figure 24. OIP3 vs. I_{ds} and V_{ds} at 2 GHz.

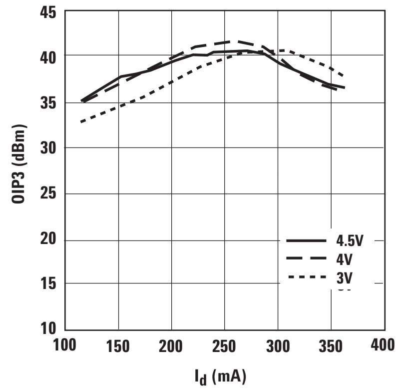


Figure 25. OIP3 vs. I_{ds} and V_{ds} at 900 MHz.

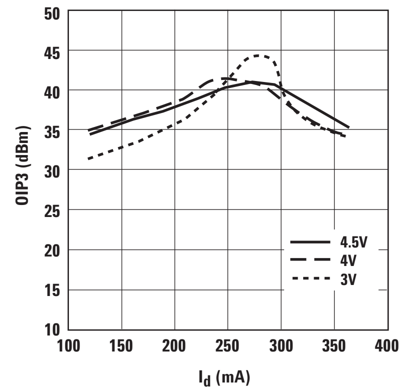


Figure 26. OIP3 vs. I_{ds} and V_{ds} at 3.9 GHz.

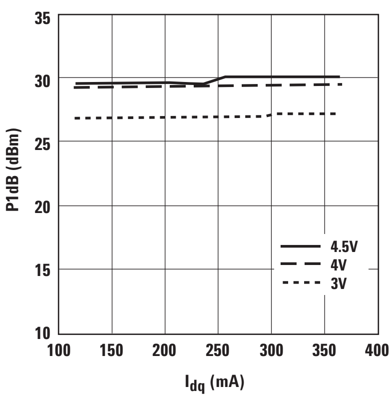


Figure 27. P1dB vs. I_{dq} and V_{ds} at 2 GHz.

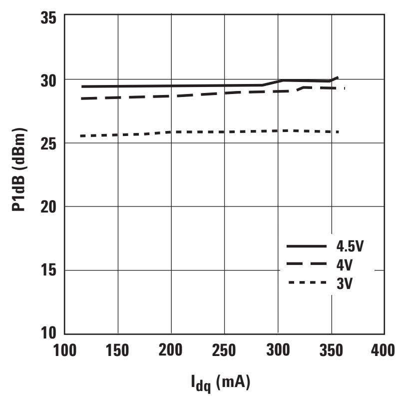


Figure 28. P1dB vs. I_{dq} and V_{ds} at 900 MHz.

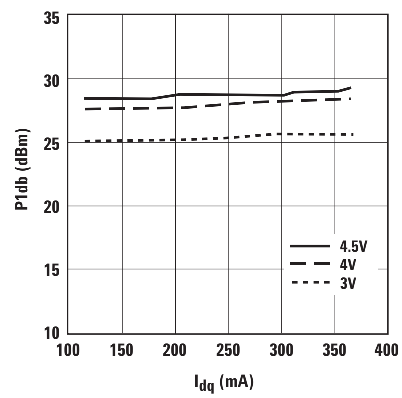


Figure 29. P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

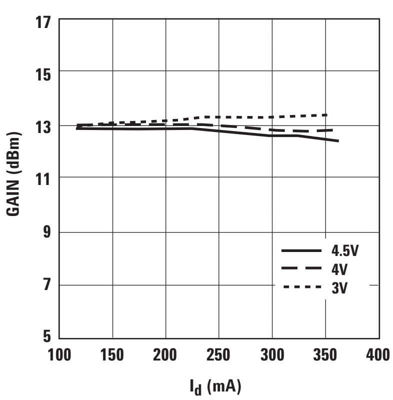


Figure 30. Gain vs I_{ds} and V_{ds} at 2 GHz.

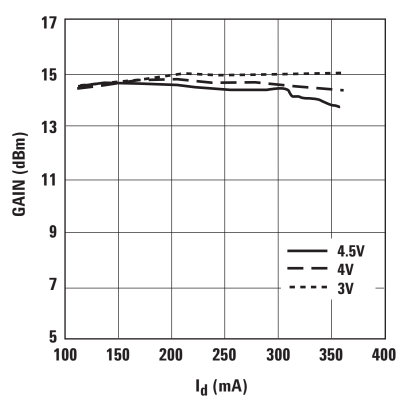


Figure 31. Gain vs I_{ds} and V_{ds} at 900 MHz.

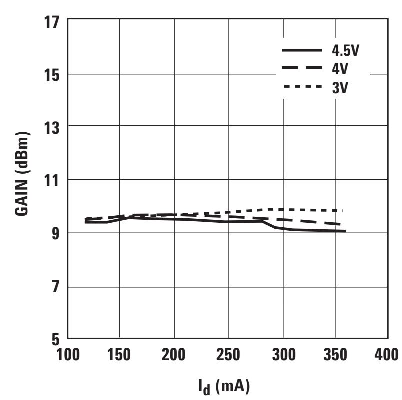


Figure 32. Gain vs I_{ds} and V_{ds} at 3.9 GHz.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Performance Curves, continued (at 25°C unless specified otherwise)

Tuned for Optimal P1dB

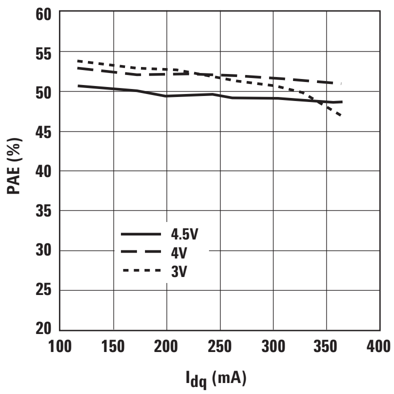


Figure 33. PAE @ P1dB vs. I_{dq} and V_{ds} at 2 GHz.

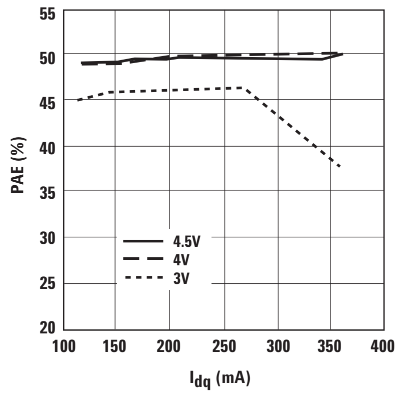


Figure 34. PAE @ P1dB vs. I_{dq} and V_{ds} at 900 MHz.

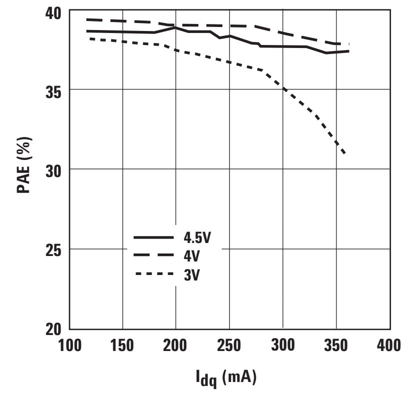


Figure 35. PAE @ P1dB vs. I_{dq} and V_{ds} at 3.9 GHz.

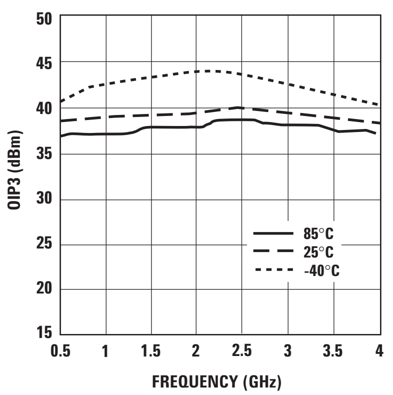


Figure 36. OIP3 vs. Temp and Freq tuned for optimal P1dB at 4.5V, 200 mA.

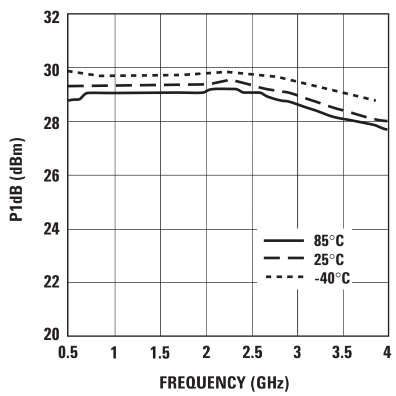


Figure 37. P1dB vs. Temp and Freq (tuned for optimal P1dB at 4.5V, 200 mA).

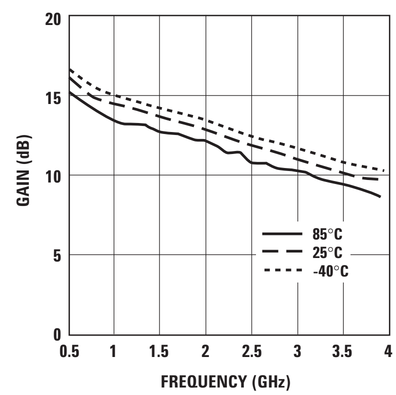


Figure 38. Gain vs. Temp and Freq tuned for optimal P1dB at 4.5V, 200 mA.

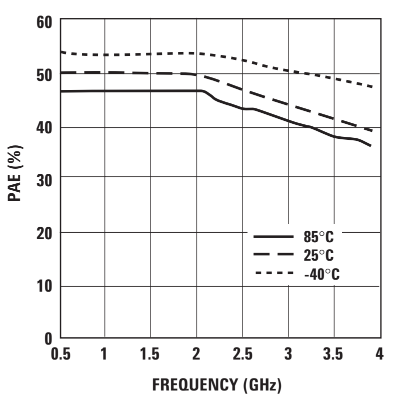


Figure 39. PAE vs Temp and Freq tuned for optimal P1dB at 4.5V.

Note:
Bias current for the above charts are quiescent conditions. Actual level may increase depending on amount of RF drive.

ATF-521P8 Typical Scattering Parameters at 25°C, V_{DS} = 4.5V, I_{DS} = 280 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.613	-96.9	33.2	45.79	141.7	-39.5	0.011	51.3	0.317	-108.3	36.2
0.2	0.780	-131.8	30.0	31.50	121.6	-36.7	0.015	37.1	0.423	-138.5	33.2
0.3	0.831	-147.2	27.3	23.26	111.0	-36.2	0.015	30.6	0.466	-152.4	31.9
0.4	0.855	-156.4	25.1	18.04	104.1	-35.4	0.017	28.2	0.483	-159.9	30.3
0.5	0.860	-162.0	23.5	14.98	99.7	-35.2	0.017	27.4	0.488	-163.8	29.5
0.6	0.878	-166.7	22.0	12.62	95.6	-35.0	0.018	26.1	0.496	-167.0	28.5
0.7	0.888	-170.2	20.8	10.95	92.8	-34.6	0.019	27.4	0.497	-169.9	27.6
0.8	0.887	-172.6	19.7	9.63	90.0	-34.3	0.019	28.9	0.500	-171.7	27.0
0.9	0.894	-174.5	18.7	8.65	87.9	-33.7	0.021	28.5	0.501	-173.6	26.1
1.0	0.886	-177.2	17.9	7.82	85.4	-33.8	0.020	30.3	0.502	-175.7	25.9
1.5	0.892	175.0	14.3	5.20	76.3	-32.8	0.023	34.6	0.502	178.8	23.5
2.0	0.883	168.7	12.1	4.01	68.4	-31.2	0.027	36.7	0.492	173.6	20.2
2.5	0.890	162.8	10.2	3.24	61.5	-30.0	0.032	36.8	0.490	169.8	18.5
3.0	0.884	157.2	8.6	2.71	54.5	-28.9	0.036	39.2	0.494	165.7	16.2
4.0	0.890	146.6	6.1	2.02	40.6	-27.0	0.045	36.1	0.505	157.8	13.8
5.0	0.893	137.0	4.1	1.60	27.6	-25.5	0.053	32.4	0.529	150.3	11.9
6.0	0.896	127.9	2.3	1.31	15.4	-24.2	0.061	28.2	0.551	142.9	10.4
7.0	0.906	119.5	0.9	1.11	3.7	-22.9	0.071	22.9	0.570	135.5	9.6
8.0	0.882	105.6	-0.8	0.92	-9.8	-21.3	0.086	14.5	0.567	127.3	6.8
9.0	0.887	96.4	-1.7	0.82	-22.2	-20.1	0.098	7.2	0.585	117.8	6.2
10.0	0.887	84.6	-2.9	0.72	-33.6	-19.3	0.109	-1.0	0.593	107.3	5.0
11.0	0.882	72.3	-3.9	0.64	-45.8	-18.5	0.119	-10.5	0.617	97.1	3.9
12.0	0.878	62.2	-5.0	0.56	-57.0	-18.0	0.126	-19.8	0.636	86.0	2.8
13.0	0.894	52.0	-6.4	0.48	-67.8	-17.8	0.130	-28.6	0.662	74.7	2.1
14.0	0.888	42.0	-7.6	0.42	-76.2	-17.3	0.137	-36.1	0.697	67.5	0.9
15.0	0.884	34.6	-8.3	0.38	-84.3	-16.6	0.147	-42.9	0.732	58.7	0.3
16.0	0.830	24.7	-9.5	0.34	-92.8	-16.1	0.156	-52.4	0.752	51.9	-1.8
17.0	0.708	11.0	-9.0	0.35	-99.5	-15.4	0.169	-63.8	0.816	46.1	-2.2
18.0	0.790	-12.7	-10.3	0.31	-93.1	-16.4	0.152	-82.8	0.660	41.2	-4.3

Typical Noise Parameters at 25°C, V_{DS} = 4.5V, I_{DS} = 280 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	R_n	G_a
GHz	dB	Mag.	Ang.		dB
0.5	1.20	0.47	170.00	2.8	22.8
1.0	1.30	0.53	-177.00	2.6	20.1
2.0	1.61	0.61	-166.34	2.7	17.3
3.0	1.68	0.69	-155.85	4.0	14.4
4.0	2.12	0.67	-146.98	8.4	11.6
5.0	2.77	0.71	-134.35	19.0	9.9
6.0	2.58	0.79	-125.22	26.7	8.8
7.0	2.85	0.82	-115.35	47.2	7.5
8.0	3.35	0.73	-105.76	65.2	5.7

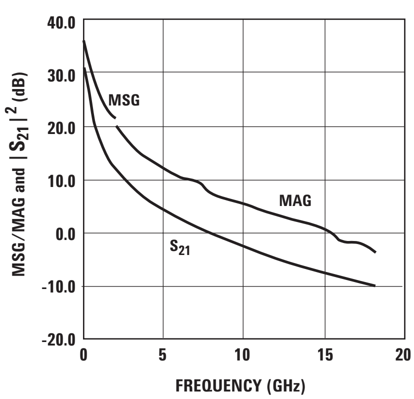


Figure 40. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4.5V, 280 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, V_{DS} = 4.5V, I_{DS} = 200 mA

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.	MSG/MAG dB
0.1	0.823	-89.9	34.4	52.21	135.6	-37.9	0.013	46.2	0.388	-113.0	36.0
0.2	0.873	-128.7	30.5	33.39	115.7	-35.6	0.017	32.0	0.478	-143.2	32.9
0.3	0.879	-145.5	27.6	23.90	106.3	-34.9	0.018	27.0	0.507	-156.0	31.2
0.4	0.885	-155.1	25.2	18.25	100.5	-34.7	0.018	25.8	0.518	-163.1	30.1
0.5	0.883	-161.1	23.6	15.12	96.6	-34.4	0.019	24.8	0.519	-166.7	29.0
0.6	0.897	-165.9	22.1	12.66	92.9	-34.1	0.020	24.2	0.525	-169.6	28.0
0.7	0.895	-169.5	20.8	10.95	90.5	-33.7	0.021	24.2	0.526	-172.2	27.2
0.8	0.894	-171.9	19.6	9.59	88.0	-33.6	0.021	25.3	0.528	-174.0	26.6
0.9	0.900	-174.7	18.7	8.64	86.2	-33.1	0.022	26.2	0.528	-175.6	25.9
1	0.893	-176.6	17.8	7.78	83.7	-33.1	0.022	27.6	0.529	-177.7	25.5
1.5	0.894	175.3	14.3	5.17	75.7	-32.1	0.025	32.6	0.527	177.2	23.2
2	0.889	168.5	12.0	4.00	67.8	-30.8	0.029	33.6	0.516	172.1	21.4
2.5	0.888	162.6	10.2	3.22	61.3	-29.8	0.032	35.2	0.514	168.1	18.4
3	0.892	157.0	8.6	2.69	54.5	-28.6	0.037	35.6	0.517	164.0	16.7
4	0.884	146.5	6.0	2.00	40.7	-26.8	0.046	34.4	0.526	156.0	13.5
5	0.891	137.0	4.0	1.59	28.3	-25.2	0.055	30.5	0.548	148.3	11.9
6	0.889	127.9	2.3	1.30	16.4	-24.0	0.063	26.4	0.568	141.0	10.1
7	0.902	119.6	0.9	1.11	4.8	-22.8	0.072	21.0	0.584	133.5	9.4
8	0.881	105.6	-0.9	0.90	-8.8	-21.3	0.086	13.3	0.580	124.9	6.7
9	0.891	96.0	-1.7	0.83	-20.1	-20.2	0.098	5.6	0.594	115.8	6.4
10	0.876	83.9	-2.9	0.72	-32.1	-19.3	0.108	-3.2	0.600	105.3	4.6
11	0.885	73.1	-3.6	0.66	-43.7	-18.5	0.119	-12.1	0.622	95.0	4.2
12	0.885	60.9	-4.8	0.57	-54.1	-18.0	0.126	-21.6	0.641	84.1	3.0
13	0.893	53.0	-6.3	0.48	-66.2	-17.7	0.131	-29.9	0.663	73.1	2.1
14	0.889	42.2	-7.2	0.44	-74.0	-17.2	0.138	-36.7	0.698	65.7	1.2
15	0.894	34.3	-7.8	0.41	-80.6	-16.9	0.143	-44.1	0.732	57.4	1.0
16	0.840	25.0	-8.4	0.38	-83.4	-16.2	0.154	-54.3	0.750	51.0	-0.8
17	0.719	9.1	-10.0	0.32	-90.1	-15.4	0.171	-64.8	0.815	44.5	-3.2
18	0.794	-8.1	-12.2	0.25	-102.3	-16.7	0.147	-84.1	0.655	40.4	-5.9

Typical Noise Parameters, V_{DS} = 4.5V, I_{DS} = 200 mA

Freq GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_a dB
0.5	0.60	0.30	130.00	2.8	20.2
1.0	0.72	0.35	150.00	2.6	18.4
2.0	0.96	0.47	-175.47	1.9	16.5
3.0	1.11	0.57	-162.03	2.1	13.8
4.0	1.44	0.62	-150.00	4.5	11.2
5.0	1.75	0.69	-136.20	10.0	9.8
6.0	1.99	0.74	-127.35	17.0	8.7
7.0	2.12	0.80	-116.83	28.5	7.5
8.0	2.36	0.69	-108.38	35.6	5.7

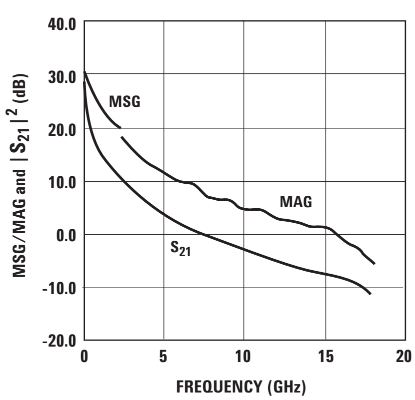


Figure 41. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4.5V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, V_{DS} = 4.5V, I_{DS} = 120 mA

Freq. GHz	S_{11} Mag.	S_{11} Ang.	S_{21} dB	S_{21} Mag.	S_{21} Ang.	S_{12} dB	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.	MSG/MAG dB
0.1	0.913	-84.6	34.2	51.26	135.4	-36.4	0.015	49.0	0.423	-106.6	35.3
0.2	0.900	-125.0	30.3	32.80	115.4	-33.9	0.020	31.2	0.499	-139.4	32.1
0.3	0.896	-142.0	27.4	23.39	106.1	-33.4	0.021	25.3	0.522	-153.4	30.5
0.4	0.893	-152.3	25.1	17.89	100.3	-32.9	0.023	23.5	0.530	-161.1	28.9
0.5	0.882	-158.4	23.4	14.75	96.3	-32.6	0.023	22.5	0.531	-165.0	28.1
0.6	0.895	-164.2	21.8	12.36	92.9	-32.7	0.023	20.6	0.537	-168.4	27.3
0.7	0.893	-167.8	20.6	10.71	90.5	-32.4	0.024	20.4	0.537	-171.2	26.5
0.8	0.895	-170.8	19.5	9.39	88.0	-32.3	0.024	21.1	0.539	-173.1	25.9
0.9	0.897	-173.0	18.5	8.44	86.1	-32.2	0.025	22.1	0.539	-174.8	25.3
1	0.895	-175.5	17.6	7.59	83.6	-31.8	0.026	23.0	0.540	-176.9	24.7
1.5	0.893	176.0	14.1	5.07	75.3	-31.1	0.028	25.5	0.538	177.4	22.6
2	0.889	169.2	11.8	3.89	67.8	-30.0	0.032	27.9	0.528	172.2	20.8
2.5	0.882	163.6	10.0	3.15	61.2	-29.0	0.036	30.2	0.526	168.1	19.4
3	0.888	157.9	8.4	2.62	54.6	-28.2	0.039	30.2	0.528	163.9	16.9
4	0.883	146.8	5.9	1.97	40.7	-26.5	0.047	29.7	0.536	155.7	13.6
5	0.885	137.7	3.8	1.55	28.2	-25.2	0.055	26.3	0.556	148.1	11.6
6	0.892	128.0	2.1	1.28	16.7	-24.0	0.063	21.9	0.576	140.5	10.2
7	0.894	120.4	0.6	1.08	5.1	-22.8	0.072	18.2	0.591	133.1	8.9
8	0.880	105.7	-1.0	0.89	-8.7	-21.2	0.087	10.6	0.585	124.3	6.6
9	0.876	96.5	-1.9	0.81	-20.8	-20.1	0.099	3.2	0.602	114.9	5.7
10	0.879	84.4	-3.0	0.71	-32.7	-19.3	0.108	-5.2	0.605	104.5	4.7
11	0.889	72.8	-3.8	0.65	-44.3	-18.6	0.118	-13.5	0.624	94.2	4.3
12	0.881	62.4	-5.2	0.55	-56.0	-18.1	0.125	-23.1	0.642	83.4	2.7
13	0.893	54.0	-6.3	0.48	-66.6	-17.7	0.130	-31.4	0.664	72.4	2.2
14	0.891	42.1	-7.2	0.44	-72.6	-17.3	0.136	-38.4	0.697	65.1	1.2
15	0.888	34.1	-8.3	0.39	-79.2	-16.8	0.144	-45.9	0.732	56.7	0.4
16	0.845	25.3	-9.1	0.35	-89.6	-16.1	0.157	-55.0	0.751	50.4	-1.5
17	0.828	13.2	-11.2	0.28	-95.9	-15.6	0.167	-64.2	0.821	44.0	-3.9
18	0.827	-10.2	-11.0	0.28	-92.5	-16.6	0.147	-86.1	0.654	39.9	-4.3

Typical Noise Parameters, V_{DS} = 4.5V, I_{DS} = 120 mA

Freq GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_a dB
0.5	0.60	0.19	162.00	3.0	20.0
1.0	0.72	0.30	164.00	2.6	18.3
2.0	0.81	0.44	176.97	2.0	15.9
3.0	0.92	0.56	-164.98	2.0	13.6
4.0	1.24	0.59	-155.51	3.4	11.1
5.0	1.50	0.70	-136.55	11.1	9.7
6.0	1.60	0.75	-128.59	16.0	8.7
7.0	1.88	0.81	-117.31	24.0	7.6
8.0	2.02	0.68	-109.54	28.8	5.6

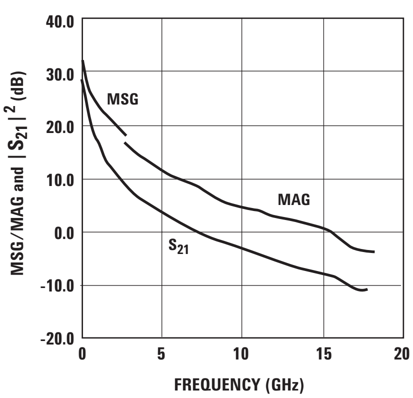


Figure 42. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4.5V, 120 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, V_{DS} = 4V, I_{DS} = 200 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.843	-90.5	34.3	51.89	134.8	-37.7	0.013	46.5	0.408	-118.1	36.0
0.2	0.879	-129.3	30.3	32.88	115.0	-35.4	0.017	32.1	0.507	-146.1	32.9
0.3	0.888	-146.1	27.4	23.48	105.8	-35.1	0.018	26.0	0.539	-158.3	31.2
0.4	0.892	-155.6	25.1	17.91	100.1	-34.4	0.019	25.1	0.549	-164.8	29.7
0.5	0.886	-161.5	23.4	14.80	96.3	-34.2	0.020	24.6	0.551	-168.2	28.7
0.6	0.896	-165.7	21.8	12.37	92.7	-34.2	0.020	24.1	0.556	-170.9	27.9
0.7	0.897	-169.5	20.6	10.74	90.5	-33.6	0.021	24.7	0.557	-173.5	27.1
0.8	0.898	-172.2	19.5	9.39	88.1	-33.5	0.021	24.4	0.559	-175.2	26.5
0.9	0.896	-174.9	18.6	8.47	85.9	-33.3	0.022	26.5	0.559	-176.9	25.9
1	0.896	-176.7	17.6	7.61	84.0	-32.9	0.023	26.3	0.560	-178.7	25.2
1.5	0.898	175.2	14.1	5.06	75.7	-32.1	0.025	29.9	0.558	176.0	23.1
2	0.887	168.0	11.8	3.91	68.1	-30.7	0.029	35.2	0.547	170.9	21.3
2.5	0.893	162.8	10.0	3.15	61.7	-29.5	0.034	35.8	0.545	166.9	18.9
3	0.886	156.9	8.4	2.63	55.1	-28.4	0.038	35.8	0.547	162.6	16.3
4	0.887	146.6	5.9	1.97	41.5	-26.7	0.046	33.2	0.554	154.3	13.6
5	0.894	136.8	3.9	1.57	29.4	-25.1	0.056	29.6	0.572	146.6	11.9
6	0.898	127.4	2.1	1.28	17.7	-23.9	0.064	25.5	0.590	139.0	10.3
7	0.896	119.7	0.7	1.09	6.3	-22.6	0.074	20.4	0.603	131.6	8.9
8	0.879	105.4	-0.9	0.90	-7.1	-21.1	0.088	12.4	0.594	122.7	6.6
9	0.888	95.0	-1.7	0.82	-19.3	-20.1	0.099	4.7	0.609	113.2	6.1
10	0.872	84.1	-2.9	0.72	-30.9	-19.2	0.110	-4.3	0.610	102.9	4.4
11	0.880	72.4	-3.8	0.65	-42.8	-18.6	0.118	-12.9	0.629	92.6	3.8
12	0.875	60.4	-4.8	0.58	-53.3	-18.0	0.126	-22.8	0.647	81.9	2.8
13	0.908	52.4	-6.2	0.49	-63.4	-17.7	0.130	-31.4	0.666	71.0	2.6
14	0.898	41.3	-7.1	0.44	-73.5	-17.2	0.138	-38.0	0.699	64.0	1.5
15	0.888	34.1	-8.2	0.39	-80.2	-16.8	0.144	-45.6	0.734	55.9	0.5
16	0.815	24.1	-8.9	0.36	-85.3	-16.2	0.156	-54.7	0.750	49.3	-1.7
17	0.725	11.3	-9.9	0.32	-90.9	-15.5	0.167	-66.0	0.809	43.5	-3.1
18	0.792	-9.8	-10.2	0.31	-95.1	-16.6	0.147	-84.8	0.652	39.7	-4.2

Typical Noise Parameters, V_{DS} = 4V, I_{DS} = 200 mA

Freq	F_{min}	Γ_{opt}	Γ_{opt}	R_n	G_a
GHz	dB	Mag.	Ang.		dB
0.5	0.67	0.21	155.00	2.8	20.1
1.0	0.74	0.30	164.00	2.6	18.4
2.0	0.96	0.46	-176.61	2.1	16.4
3.0	1.24	0.57	-162.19	2.8	13.9
4.0	1.44	0.62	-152.18	4.5	11.4
5.0	1.62	0.69	-135.43	10.0	10.0
6.0	1.83	0.74	-127.94	17.0	8.7
7.0	1.99	0.82	-117.20	27.7	7.7
8.0	2.21	0.71	-108.96	35.3	5.9

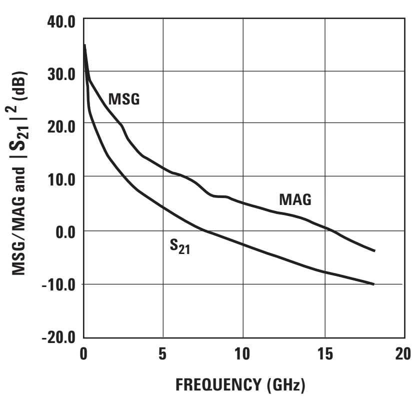


Figure 43. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 4V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Typical Scattering Parameters, V_{DS} = 3V, I_{DS} = 200 mA

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		MSG/MAG
GHz	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	dB
0.1	0.867	-94.6	33.7	48.20	132.4	-36.8	0.014	45.1	0.482	-132.4	35.4
0.2	0.894	-132.9	29.4	29.66	113.2	-34.9	0.018	28.5	0.601	-154.2	32.2
0.3	0.899	-148.2	26.5	21.06	104.4	-34.1	0.020	23.2	0.636	-163.8	30.2
0.4	0.896	-157.2	24.1	16.00	99.1	-34.0	0.020	23.7	0.647	-169.2	29.0
0.5	0.892	-162.8	22.4	13.20	95.6	-33.6	0.021	24.5	0.650	-171.9	28.0
0.6	0.910	-167.4	20.8	11.00	92.3	-33.2	0.022	22.9	0.655	-174.4	27.0
0.7	0.906	-170.8	19.6	9.51	90.2	-33.2	0.022	23.9	0.657	-176.7	26.4
0.8	0.902	-173.6	18.4	8.35	87.8	-33.0	0.022	24.6	0.658	-178.2	25.8
0.9	0.907	-175.2	17.5	7.51	86.3	-32.9	0.023	27.0	0.660	-179.5	25.1
1	0.902	-177.7	16.6	6.76	84.2	-32.5	0.024	26.9	0.659	178.6	24.5
1.5	0.900	174.2	13.1	4.50	76.4	-31.5	0.027	32.7	0.656	173.4	22.2
2	0.896	168.1	10.8	3.49	69.1	-29.9	0.032	32.9	0.647	167.9	20.4
2.5	0.896	162.3	9.0	2.82	63.0	-29.0	0.036	34.3	0.642	163.7	18.6
3	0.887	156.7	7.4	2.35	56.9	-27.7	0.041	35.0	0.643	159.2	15.6
4	0.890	145.7	4.9	1.76	43.8	-26.1	0.050	32.2	0.645	150.4	12.9
5	0.898	136.3	3.0	1.41	32.1	-24.5	0.059	28.3	0.659	142.1	11.3
6	0.896	127.4	1.3	1.16	21.6	-23.4	0.068	23.5	0.671	134.3	9.5
7	0.904	119.4	-0.2	0.98	10.3	-22.1	0.078	17.7	0.677	126.6	8.5
8	0.877	104.9	-1.6	0.83	-2.3	-20.7	0.092	9.0	0.651	117.0	5.9
9	0.883	94.8	-2.4	0.76	-13.0	-19.8	0.102	1.3	0.661	107.2	5.3
10	0.877	83.1	-3.5	0.67	-26.0	-18.9	0.113	-7.3	0.657	96.8	4.0
11	0.875	71.7	-4.4	0.60	-36.3	-18.3	0.121	-16.6	0.670	86.7	3.1
12	0.863	60.6	-5.4	0.54	-47.4	-17.8	0.128	-25.1	0.680	76.2	1.9
13	0.910	51.6	-6.5	0.47	-57.9	-17.6	0.132	-33.6	0.694	65.9	2.3
14	0.868	40.9	-7.5	0.42	-62.8	-17.2	0.138	-40.4	0.721	59.3	0.2
15	0.863	33.4	-8.1	0.39	-74.7	-16.8	0.144	-47.6	0.748	51.3	-0.2
16	0.835	25.2	-9.6	0.33	-78.2	-16.3	0.154	-56.8	0.758	44.9	-2.1
17	0.720	11.2	-9.5	0.33	-90.8	-15.8	0.161	-67.6	0.818	39.4	-2.6
18	0.780	-7.7	-11.6	0.26	-92.8	-17.0	0.142	-85.1	0.655	37.1	-5.7

Typical Noise Parameters, V_{DS} = 3V, I_{DS} = 200 mA

Freq GHz	F_{min} dB	Γ_{opt} Mag.	Γ_{opt} Ang.	R_n	G_a dB
0.5	0.66	0.22	147.00	2.9	20.0
1.0	0.72	0.30	160.00	2.6	18.3
2.0	0.87	0.42	-179.94	1.9	16.0
3.0	1.00	0.59	-163.63	1.6	13.7
4.0	1.32	0.63	-153.81	3.7	11.3
5.0	1.49	0.72	-135.10	10.0	9.9
6.0	1.59	0.74	-128.97	15.0	8.5
7.0	1.79	0.78	-117.68	25.1	7.6
8.0	1.96	0.70	-110.04	29.2	5.6

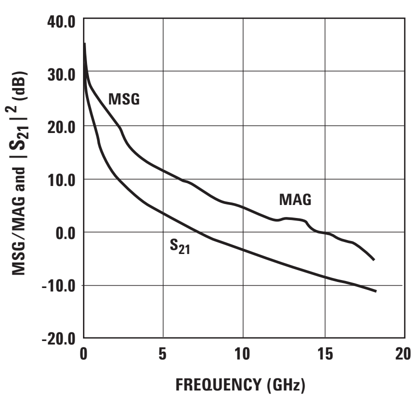


Figure 44. MSG/MAG and $|S_{21}|^2$ vs. Frequency at 3V, 200 mA.

Notes:

1. F_{min} values at 2 GHz and higher are based on measurements while the F_{mins} below 2 GHz have been extrapolated. The F_{min} values are based on a set of 16 noise figure measurements made at 16 different impedances using an ATN NP5 test system. From these measurements a true F_{min} is calculated. Refer to the noise parameter application section for more information.
2. S and noise parameters are measured on a microstrip line made on 0.025 inch thick alumina carrier. The input reference plane is at the end of the gate lead. The output reference plane is at the end of the drain lead.

ATF-521P8 Applications Information

Description

Avago Technologies' ATF-521P8 is an enhancement mode PHEMT designed for high linearity and medium power applications. With an OIP3 of 42 dBm and a 1dB compression point of 26 dBm, ATF-521P8 is well suited as a base station transmit driver or a first or second stage LNA in a receive chain. Whether the design is for a W-CDMA, CDMA, or GSM basestation, this device delivers good linearity in the form of OIP3 or ACLR, which is required for standards with high peak to average ratios.

Application Guidelines

The ATF-521P8 device operates as a normal FET requiring input and output matching as well as DC biasing. Unlike a depletion mode transistor, this enhancement mode device only requires a single positive power supply, which means a positive voltage is placed on the drain and gate in order for the transistor to turn on. This application note walks through the RF and DC design employed in a single FET amplifier. Included in this description is an active feedback scheme to accomplish this DC biasing.

RF Input & Output Matching

In order to achieve maximum linearity, the appropriate input (Γ_s) and output (Γ_L) impedances must be presented to the device. Correctly matching from these impedances to 50Ωs will result in maximum linearity. Although ATF-521P8 may be used in other impedance systems, data collected for this data sheet is all referenced to a 50Ω system.

The input load pull parameter at 2 GHz is shown in Figure 1 along with the optimum S11 conjugate match.

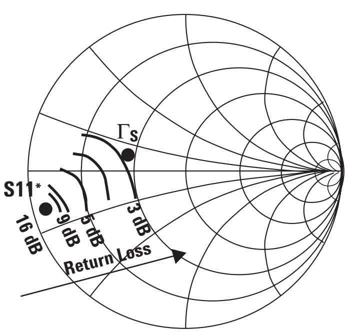


Figure 1. Input Match for ATF-521P8 at 2 GHz.

Thus, it should be obvious from the illustration above that if this device is matched for maximum return loss i.e. S11*, then OIP3 will be sacrificed. Conversely, if ATF-521P8 is matched for maximum linearity, then return loss will not be greater than 10 dB. For most applications, a designer requires VSWR greater than 2:1, hence limiting the input match close to S11*. Normally, the input return loss of a single ended amplifier is not critical as most basestation LNA and driver amplifiers are in a balanced configuration with 90° (quadrature) couplers.

Proceeding from the same premise, the output match of this device becomes much simpler. As background information, it is important to note that OIP3 is largely dependant on the output match and that output return loss is also required to be greater than 10 dB. So, Figure 2 shows how both good output return loss and good linearity could be achieved simultaneously with the same impedance point.

Of course, these points are valid only at 2 GHz, and other frequencies will follow the same design rules but will have different locations. Also, the location of these points is largely due to the manufacturing process and partly due to IC layout, but in either case beyond the scope of this application note.

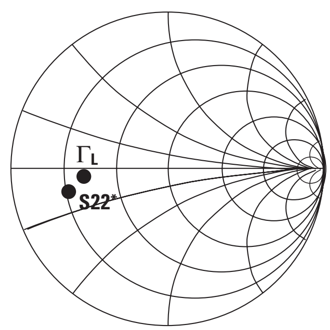


Figure 2. Output Match at 2 GHz.

Once a designer has chosen the proper input and output impedance points, the next step is to choose the correct topology to accomplish this match. For example to perform the above output impedance transformation from 50Ω to the given load parameter of 0.53∠-176°, two possible solutions exist. The first potential match is a high pass configuration accomplished by a shunt inductor and a series capacitor shown in Figure 3 along with its frequency response in Figure 4.

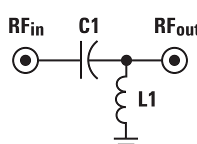


Figure 3. High Pass Circuit Topology.

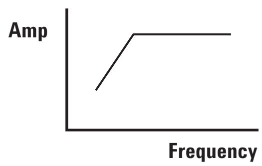


Figure 4. High Pass Frequency Response.

The second solution is a low pass configuration with a shunt capacitor and a series inductor shown in Figure 5 and 6.

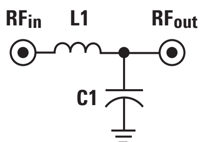


Figure 5. Low Pass Circuit Topology.

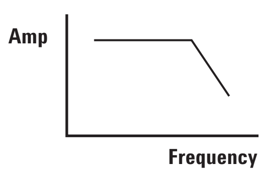


Figure 6. Low Pass Frequency Response.

The actual values of these components may be calculated by hand on a Smith Chart or more accurately done on simulation software such as ADS. There are some advantages and disadvantages of choosing a high pass versus a low pass. For instance, a high pass circuit cuts off low frequency gain, which narrows the usable bandwidth of the amplifier, but consequently helps avoid potential low frequency instability problems. A low pass match offers a much broader frequency response, but it has two major disadvantages. First it has the potential for low frequency instability, and second it creates the need for an extra DC blocking capacitor on the input in order to isolate the device gate from the preceding stages.

Figure 7 displays the input and output matching selected for ATF-521P8. In this example the input and output match both essentially function as high pass filters, but the high frequency gain of the device rolls off precipitously giving a narrow band frequency response, yet still wide enough to accommodate a CDMA or WCDMA transmit band. For more information on RF matching techniques refer to MGA-53543 application note.

Passive Bias [1]

Once the RF matching has been established, the next step is to DC bias the device. A passive biasing example is shown in Figure 8. In this example the voltage drop across resistor R3 sets the drain current (Id) and is calculated by the following equation:

$$R3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{bb}} \qquad (1)$$

where,

V_{dd} is the power supply voltage;

V_{ds} is the device drain to source voltage;

I_{ds} is the device drain to source current;

I_{bb} for DC stability is 10X the typical gate current;

A voltage divider network with R1 and R2 establishes the typical gate bias voltage (Vg).

$$R1 = \frac{V_g}{I_{bb}} \qquad (2)$$

$$R2 = \frac{(V_{dd} - V_g) \times R1}{V_g} \qquad (3)$$

Often the series resistor, R4, is added to enhance the low frequency stability. The complete passive bias example may be found in reference [1].

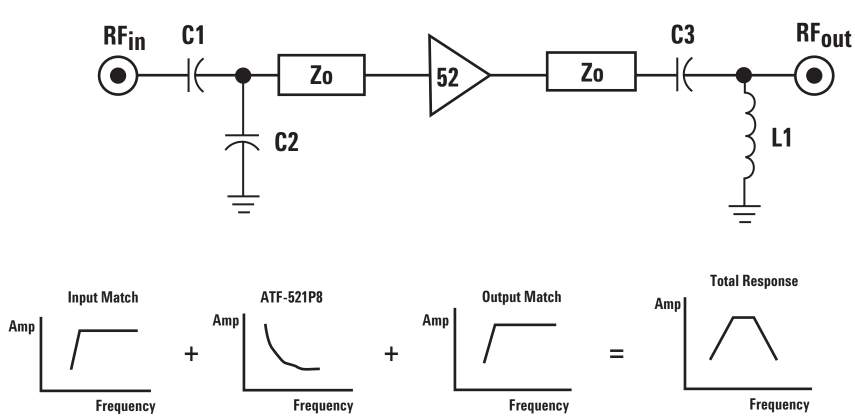


Figure 7. Input and Output Match for ATF-521P8 at 2 GHz.

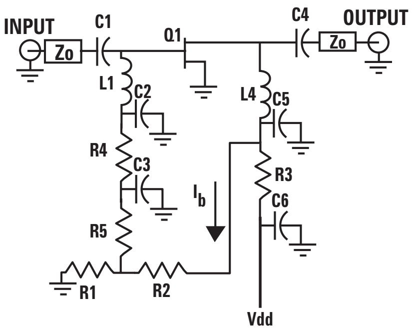


Figure 8. Passive Biasing.

Active Bias[2]

Due to very high DC power dissipation and small package constraints, it is recommended that ATF-521P8 use active biasing. The main advantage of an active biasing scheme is the ability to hold the drain to source current constant over a wide range of temperature variations.

A very inexpensive method of accomplishing this is to use two PNP bipolar transistors arranged in a current mirror configuration as shown in Figure 9. Due to resistors R1 and R3, this circuit is not acting as a true current mirror, but if the voltage drop across R1 and R3 is kept identical then it still displays some of the more useful characteristics of a current mirror. For example, transistor Q1 is configured with its base and collector tied together. This acts as a simple PN junction, which helps temperature compensate the Emitter-Base junction of Q2.

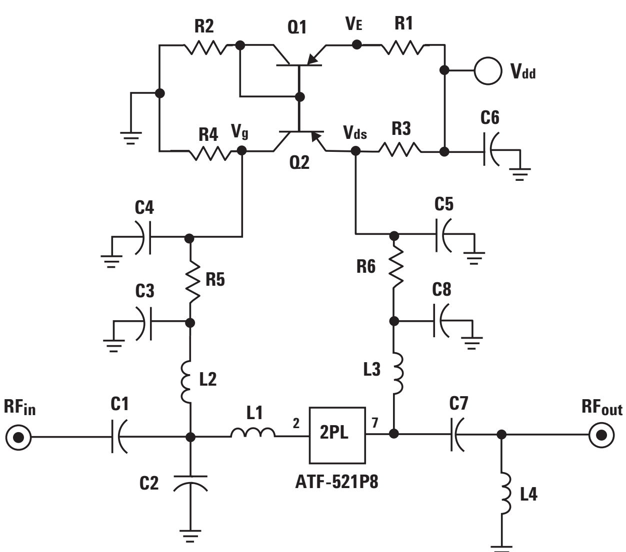


Figure 9. Active Bias Circuit.

To calculate the values of R1, R2, R3, and R4 the following parameters must be know or chosen first:

I_{ds} is the device drain-to-source current;

I_R is the Reference current for active bias;

V_{dd} is the power supply voltage available;

V_{ds} is the device drain-to-source voltage;

V_g is the typical gate bias;

V_{be1} is the typical Base-Emitter turn on voltage for Q1 & Q2;

Therefore, resistor R3, which sets the desired device drain current, is calculated as follows:

$$R3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{C2}} \qquad (4)$$

where,

I_{C2} is chosen for stability to be 10 times the typical gate current and also equal to the reference current I_R.

The next three equations are used to calculate the rest of the biasing resistors for Figure 9. Note that the voltage drop across R1 must be set equal to the voltage drop across R3, but with a current of I_R.

$$R1 = \frac{V_{dd} - V_{ds}}{I_R} \qquad (5)$$

R2 sets the bias current through Q1.

$$R2 = \frac{V_{ds} - V_{be1}}{I_R} \qquad (6)$$

R4 sets the gate voltage for ATF-521P8.

$$R4 = \frac{V_g}{I_{C2}} \qquad (7)$$

Thus, by forcing the emitter voltage (V_E) of transistor Q1 equal to V_{ds}, this circuit regulates the drain current similar to a current mirror. As long as Q2 operates in the forward active mode, this holds true. In other words, the Collector-Base junction of Q2 must be kept reversed biased.

PCB Layout

A recommended PCB pad layout for the Leadless Plastic Chip Carrier (LPCC) package used by the ATF-521P8 is shown in Figure 10. This layout provides plenty of plated through hole vias for good thermal and RF grounding. It also provides a good transition from microstrip to the device package. For more detailed dimensions refer to Section 9 of the data sheet.

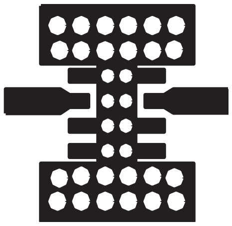


Figure 10. Microstripline Layout.

RF Grounding

Unlike SOT packages, ATF-521P8 is housed in a leadless package with the die mounted directly to the lead frame or the belly of the package shown in Figure 11.

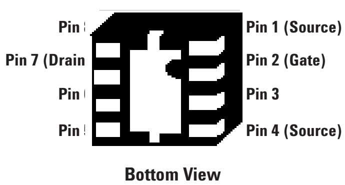


Figure 11. LPCC Package for ATF-521P8.

This simplifies RF grounding by reducing the amount of inductance from the source to ground. It is also recommended to ground pins 1 and 4 since they are also connected to the device source. Pins 3, 5, 6, and 8 are not connected, but may be used to help dissipate heat from the package or for better alignment when soldering the device.

This three-layer board (Figure 12) contains a 10-mil layer and a 52-mil layer separated by a ground plane. The first layer is Getek RG200D material with dielectric constant of 3.8. The second layer is for mechanical rigidity and consists of FR4 with dielectric constant of 4.2.

High Linearity Tx Driver

The need for higher data rates and increased voice capacity gave rise to a new third generation standard know as Wideband CDMA or UMTS. This new standard requires higher performance from radio components such as higher dynamic range and better linearity. For example, a WCDMA waveform has a very high peak to average ratio which forces amplifiers in a transmit chain to have very good Adjacent Channel Leakage power Ratio or ACLR, or else operate in a backed off mode. If the amplifier is not backed off then the waveform is compressed and the signal becomes very nonlinear.

This application example presents a highly linear transmit drive for use in the 2.14GHz frequency range. Using the RF matching techniques described earlier, ATF-521P8 is matched to the following input and output impedances:

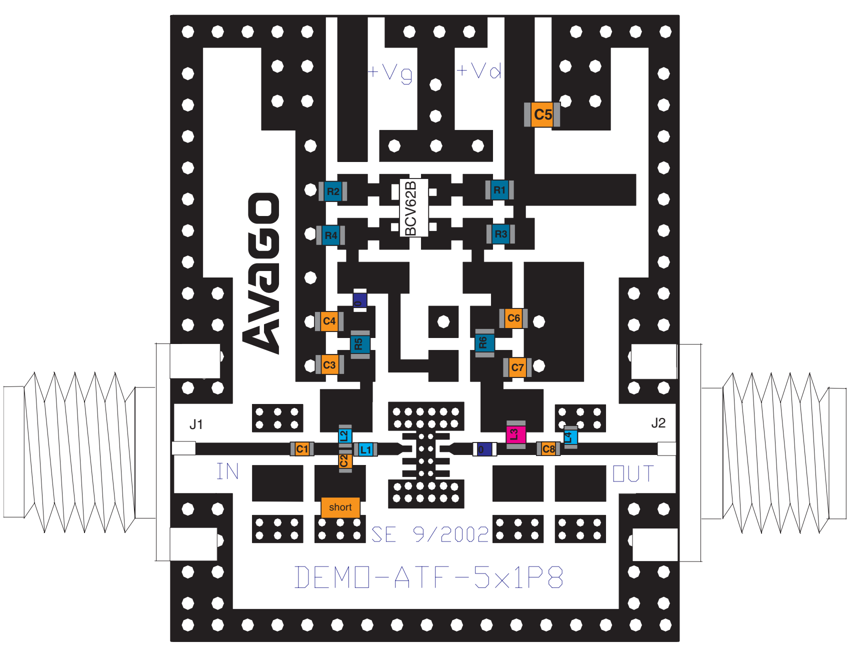


Figure 12. ATF-521P8 demoboard.

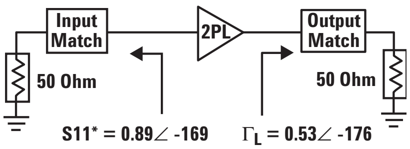


Figure 13. ATF-521P8 Matching.

As described previously the input impedance must be matched to S11* in order to guarantee return loss greater than 10 dB. A high pass network is chosen for this match. The output is matched to Γ_L with another high pass network. The next step is to choose the proper DC biasing conditions. From the data sheet, ATF-521P8 produces good linearity at a drain current of 200mA and a drain to source voltage of 4.5V. Thus to construct the active bias circuit described, the following parameters are given:

Ids = 200 mA

I_R = 10 mA

V_{dd} = 5 V

V_{ds} = 4.5V

V_g = 0.62V

V_{be1} = 0.65 V

Using equations 4, 5, 6, and 7, the biasing resistor values are calculated in column 2 of table 1, and the actual values used are listed in column 3.

Table 1. Resistors for Active Bias.

Resistor	Calculated	Actual
R1	50Ω	49.9Ω
R2	385Ω	383Ω
R3	2.38Ω	2.37Ω
R4	62Ω	61.9Ω

The entire circuit schematic for a 2.14 GHz Tx driver amplifier is shown below in Figure 14. Capacitors C4, C5, and C6 are added as a low frequency bypass. These terminate second order harmonics and help improve linearity. Resistors R5 and R6 also help terminate low frequencies, and can prevent resonant frequencies between the two bypass capacitors.

Performance of ATF-521P8 at 2140 MHz

ATF-521P8 delivers excellent performance in the WCDMA frequency band. With a drain-to-source voltage of 4.5V and a drain current of 200 mA, this device has 16.5 dB of gain and 1.55 dB of noise figure as show in Figure 15.

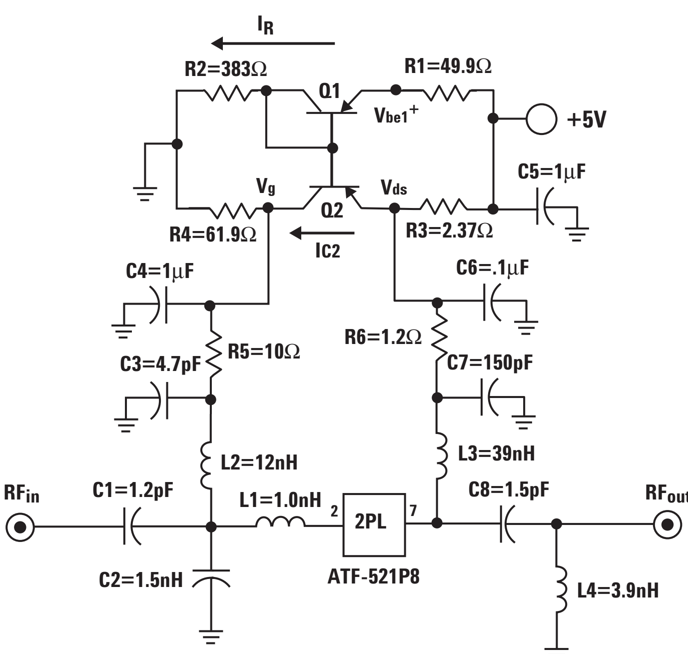


Figure 14. 2140 MHz Schematic.

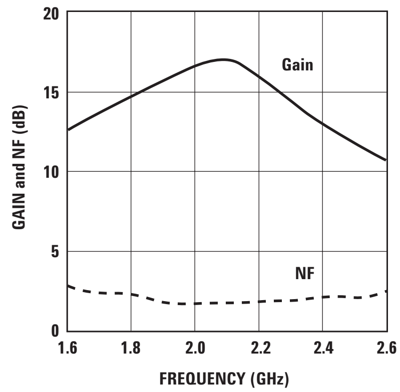


Figure 15. Gain and Noise Figure vs. Frequency.

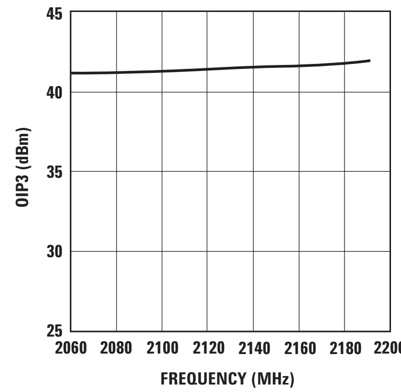


Figure 17. OIP3 vs. Frequency in WCDMA Band (Pout = 12 dBm).

Input and output return loss are both greater that 10 dB. Although somewhat narrowband, the response is adequate in the frequency range of 2110 MHz to 2170 MHz for the WCDMA downlink. If wider band response is need, using a balanced configuration improves return loss and doubles OIP3.

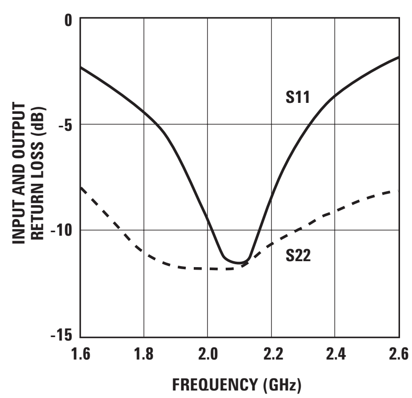


Figure 16. Input and Output Return Loss vs. Frequency.

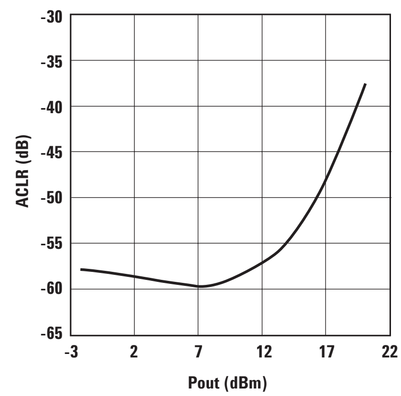


Figure 18. ACLR vs. Pout at 5 MHz Offset.

Perhaps the most critical system level specification for the ATF-521P8 lies in its distortion-less output power. Typically, amplifiers are characterized for linearity by measuring OIP3. This is a two-tone harmonic measurement using CW signals. But because WCDMA is a modulated waveform spread across 3.84 MHz, it is difficult to correlated good OIP3 to good ACLR. Thus, both are measured and presented to avoid ambiguity.

Table 2. 2140 MHz Bill of Material.

C1=1.2 pF	Phycomp 0402CG129C9B200
C2,C8=1.5 pF	Phycomp 0402CG159C9B200
C3=4.7 pF	Phycomp 0402CG479C9B200
C4,C6=.1 µF	Phycomp 06032F104M8B200
C5=1 µF	AVX 0805ZC105KATZA
C7=150 pF	Phycomp 0402CG151J9B200
L1=1.0 nH	TOKO LL1005-FH1n0S
L2=12 nH	TOKO LL1005-FS12N
L3=39 nH	TOKO LL1005-FS39
L4=3.9 nH	TOKO LL1005-FH3N9S
R1=49.9Ω	RohmRK73H1J49R9F
R2=383Ω	Rohm RK73H1J3830F
R3=2.37Ω	Rohm RK73H1J2R37F
R4=61.9Ω	Rohm RK73H1J61R9F
R5=10Ω	Rohm RK73H1J10R0F
R6=1.2Ω	Rohm RK73H1J1R21F
Q1, Q2	Philips BCV62B
J1, J2	142-0701-851

Using the 3GPP standards document Release 1999 version 2002-6, the following channel configuration was used to test ACLR. This table contains the power levels of the main channels used for Test Model 1. Note that the DPCH can be made up of 16, 32, or 64 separate channels each at different power levels and timing offsets. For a listing of power levels, channelization codes and timing offset see the entire 3GPP TS 25.141 V3.10.0 (2002-06) standards document at: http://www.3gpp.org/specs/specs.htm

Table 3. ACLR Channel Power Configuration.

3GPP TS 25.141 V3.10.0 (2002-06) Type	Pwr (dB)
P-CCPCH+SCH	-10
Primary CPICH	-10
PICH	-18
S-CCPCH containing PCH (SF=256)	-18
DPCH-64ch (SF=128)	-1.1

Thermal Design

When working with medium to high power FET devices, thermal dissipation should be a large part of the design. This is done to ensure that for a given ambient temperature the transistor's channel does not exceed the maximum rating, T_{CH}, on the data sheet. For example, ATF-521P8 has a maximum channel temperature of 150°C and a channel to board thermal resistance of 45°C/W, thus the entire thermal design hinges from these key data points. The question that must be answered is whether this device can operate in a typical environment with ambient temperature fluctuations from -25°C to 85°C. From Figure 19, a very useful equation is derived to calculate the temperature of the channel for a given ambient temperature. These calculations are all incorporated into Avago Technologies AppCAD.

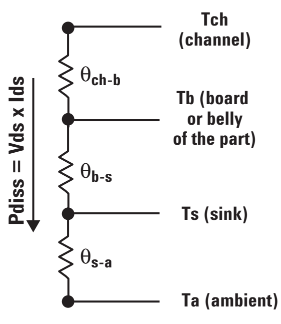


Figure 19. Equivalent Circuit for Thermal Resistance.

Hence very similar to Ohms Law, the temperature of the channel is calculated with equation 8 below.

$$T_{CH} = P_{diss}\,(\theta_{ch-b} + \theta_{b-s} + \theta_{s-a}) + T_{amb} \qquad (8)$$

If no heat sink is used or heat sinking is incorporated into the PCB board then equation 8 may be reduced to:

$$T_{CH} = P_{diss}\,(\theta_{ch-b} + \theta_{b-a}) + T_{amb} \quad (9)$$

where,

θ_{b-a} is the board to ambient thermal resistance;

θ_{ch-b} is the channel to board thermal resistance.

The board to ambient thermal resistance thus becomes very important for this is the designer's major source of heat control. To demonstrate the influence of θ_{b-a}, thermal resistance is measured for two very different scenarios using the ATF-521P8 demoboard. The first case is done with just the demoboard by itself. The second case is the ATF demoboard mounted on a chassis or metal casing, and the results are given below:

Table 4. Thermal resistance measurements.

ATF Demoboard	θ_{b-a}
PCB 1/8" Chassis	10.4°C/W
PCB no HeatSink	32.9°C/W

Therefore calculating the temperature of the channel for these two scenarios gives a good indication of what type of heat sinking is needed.

Case 1: Chassis Mounted @ 85°C

$Tch = P \times (\theta_{ch-b} + \theta_{b-a}) + Ta$

$= .9W \times (45+10.4)°C/W + 85°C$

$Tch = 135°C$

Case 2: No Heatsink @ 85°C

$Tch = P \times (\theta_{ch-b} + \theta_{b-a}) + Ta$

$= .9W \times (45+32.9)°C/W + 85°C$

$Tch = 155°C$

In other words, if the board is mounted to a chassis, the channel temperature is guaranteed to be 135°C safely below the 150°C maximum. But on the other hand, if no heat sinking is used and the θ_{b-a} is above 27°C/W (32.9°C/W in this case), then the power must be derated enough to lower the temperature below 150°C. This can be better understood with Figure 20 below. Note power is derated at 13 mW/°C for the board with no heat sink and no derating is required for the chassis mounted board until an ambient temperature of 100°C.

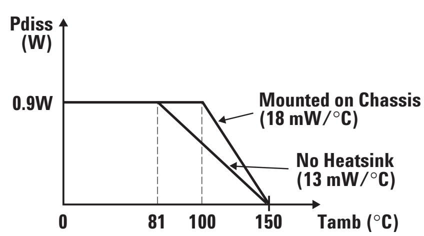


Figure 20. Derating for ATF- 521P8.

Thus, for reliable operation of ATF-521P8 and extended MTBF, it is recommended to use some form of thermal heatsinking. This may include any or all of the following suggestions:

- Maximize vias underneath and around package;
- Maximize exposed surface metal;
- Use 1 oz or greater copper clad;
- Minimize board thickness;
- Metal heat sinks or extrusions;
- Fans or forced air;
- Mount PCB to Chassis.

Summary

A high linearity Tx driver amplifier for WCDMA has been presented and designed using Agilent's ATF-521P8. This includes RF, DC and good thermal dissipation practices for reliable lifetime operation. A summary of the typical performance for ATF-521P8 demoboard at 2140 MHz is as follows:

Demo Board Results at 2140 MHz	
Gain	16.5 dB
OIP3	41.2 dBm
ACLR	-58 dBc
P1dB	24.8 dBm
NF	1.55 dB

References

[1] Ward, A. (2001) **Avago Technologies ATF-54143 Low Noise Enhancement Mode Pseudomorphic HEMT in a Surface Mount Plastic Package**, 2001 [Internet], Available from:

<http://www.avagotech.com>

[2] **Biasing Circuits and Considerations for GaAs MESFET Power Amplifiers**, 2001 [Internet], Available from: <http://www.rf-solutions.com/pdf/AN-0002_ajp.pdf> [Accessed 22 August, 2002]

Device Models

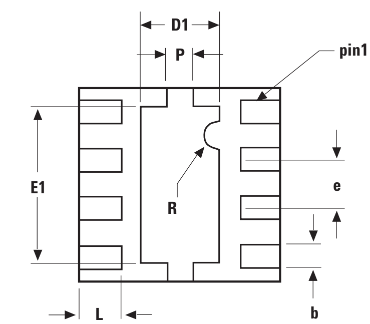
Refer to Avago Technologies' Web Site:

www.avagotech.com

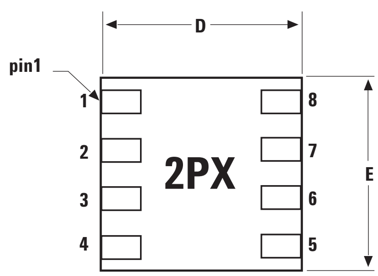
Ordering Information

Part Number	No. of Devices	Container
ATF-521P8-TR1	3000	7" Reel
ATF-521P8-TR2	10000	13"Reel
ATF-521P8-BLK	100	antistatic bag

2 x 2 LPCC (JEDEC DFP-N) Package Dimensions



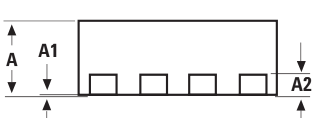
Bottom View



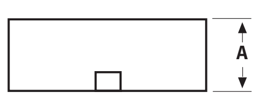
Top View

SYMBOL	DIMENSIONS MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2		0.203 REF	
b	0.225	0.25	0.275
D	1.9	2.0	2.1
D1	0.65	0.80	0.95
E	1.9	2.0	2.1
E1	1.45	1.6	1.75
e		0.50 BSC	
P	0.2	0.25	0.3
L	0.35	0.4	0.45

DIMENSIONS ARE IN MILLIMETERS

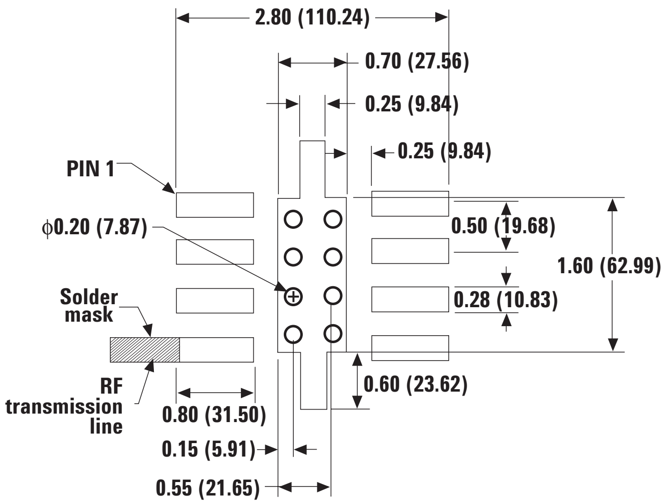


End View

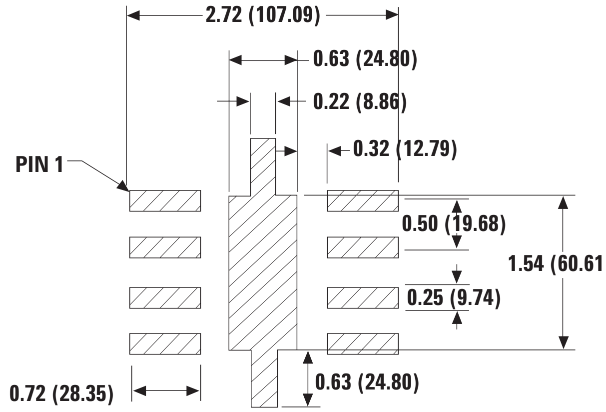


End View

PCB Land Pattern and Stencil Design

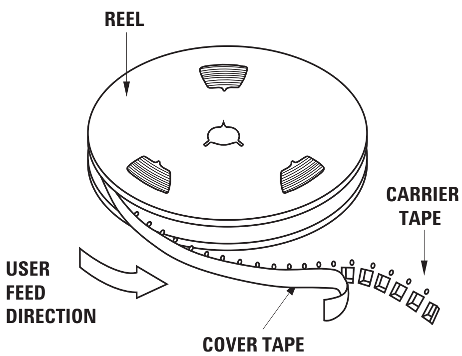


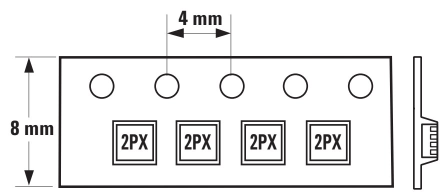
PCB Land Pattern (top view)



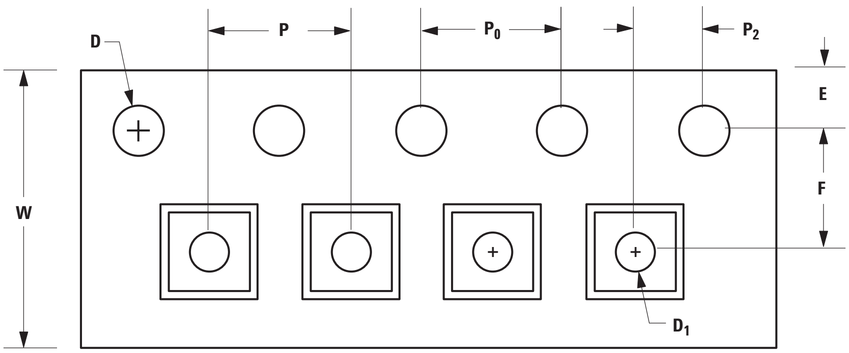
Stencil Layout (top view)

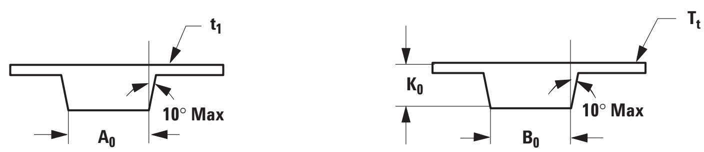
Device Orientation





Tape Dimensions





DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (inches)
CAVITY	LENGTH WIDTH DEPTH PITCH BOTTOM HOLE DIAMETER	A_0 B_0 K_0 P D_1	2.30 ± 0.05 2.30 ± 0.05 1.00 ± 0.05 4.00 ± 0.10 1.00 + 0.25	0.091 ± 0.004 0.091 ± 0.004 0.039 ± 0.002 0.157 ± 0.004 0.039 + 0.002
PERFORATION	DIAMETER PITCH POSITION	D P_0 E	1.50 ± 0.10 4.00 ± 0.10 1.75 ± 0.10	0.060 ± 0.004 0.157 ± 0.004 0.069 ± 0.004
CARRIER TAPE	WIDTH THICKNESS	W t_1	8.00 + 0.30 8.00 – 0.10 0.254 ± 0.02	0.315 ± 0.012 0.315 ± 0.004 0.010 ± 0.0008
COVER TAPE	WIDTH TAPE THICKNESS	C T_t	5.4 ± 0.10 0.062 ± 0.001	0.205 ± 0.004 0.0025 ± 0.0004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION) CAVITY TO PERFORATION (LENGTH DIRECTION)	F P_2	3.50 ± 0.05 2.00 ± 0.05	0.138 ± 0.002 0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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