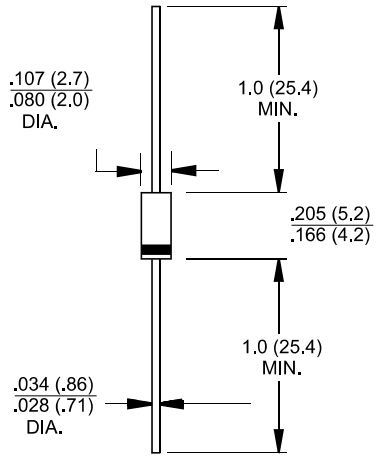
BA157 THRU BA159

1.0 AMP. Fast Recovery Rectifiers

Voltage Range
400 to 1000 Volts
Current
1.0 Ampere

DO-41



Dimensions in inches and (millimeters)

Features

- ✧ Low forward voltage drop
- ✧ High current capability
- ✧ High reliability
- ✧ High surge current capability

Mechanical Data

- ✧ Cases: DO-41 Molded plastic
- ✧ Epoxy: UL 94V-0 rate flame retardant
- ✧ Lead: Axial leads, solderable per MIL-STD-202, Method 208 guaranteed
- ✧ Polarity: Color band denotes cathode end
- ✧ High temperature soldering guaranteed: 250°C/10 seconds/.375",(9.5mm) lead lengths at 5 lbs.,(2.3kg) tension
- ✧ Weight: 0.34 gram

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60 Hz, resistive or inductive load.
For capacitive load, derate current by 20%

Type Number	BA157	BA158	BA159	Units
Maximum Recurrent Peak Reverse Voltage	400	600	1000	V
Maximum RMS Voltage	280	420	700	V
Maximum DC Blocking Voltage	400	600	1000	V
Maximum Average Forward Rectified Current .375"(9.5mm) Lead Length @T_A = 45°C	1.0			A
Peak Forward Surge Current, 8.3 ms Single Half Sine-wave Superimposed on Rated Load (JEDEC method)	30			A
Maximum Instantaneous Forward Voltage @ 1.0A	1.2			V
Maximum DC Reverse Current @ T_A=25°C at Rated DC Blocking Voltage @ T_A=100°C	5.0 100			uA uA
Maximum Reverse Recovery Time (Note 1)	150		250	nS
Typical Junction Capacitance (Note 2)	15			pF
Operating Temperature Range T_J	-65 to +150			°C
Storage Temperature Range T_{STG}	-65 to +150			°C

Notes: 1. Reverse Recovery Test Conditions: I_F=0.5A, I_R=1.0A, I_{RR}=0.25A
2. Measured at 1 MHz and Applied Reverse Voltage of 4.0 Volts D.C.

RATINGS AND CHARACTERISTIC CURVES (BA157 THRU BA159)

FIG.1- MAXIMUM FORWARD CURRENT DERATING CURVE

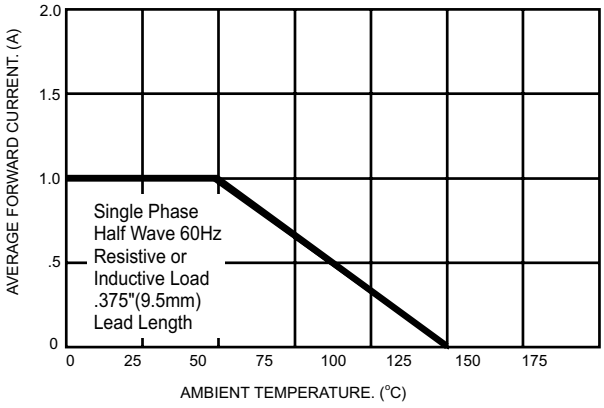


FIG.2- MAXIMUM NON-REPETITIVE PEAK FORDWARD SURGE CURRENT

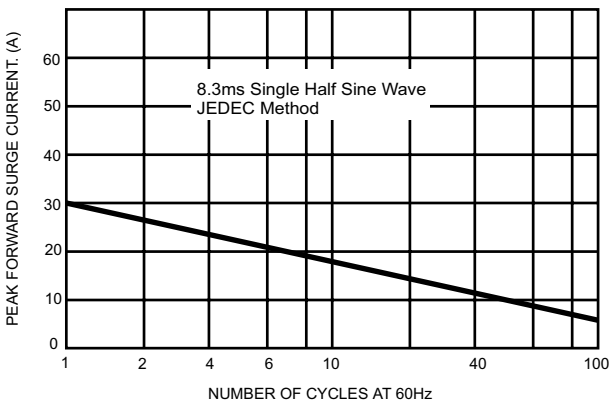


FIG.3- TYPICAL FORWARD CHARACTERISTICS

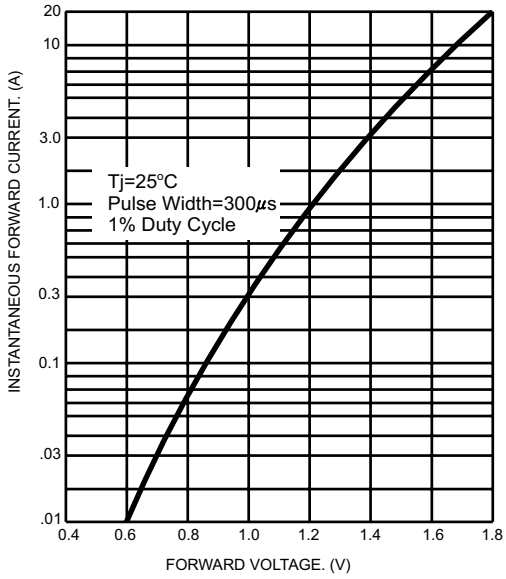


FIG.4- TYPICAL JUNCTION CAPACITANCE

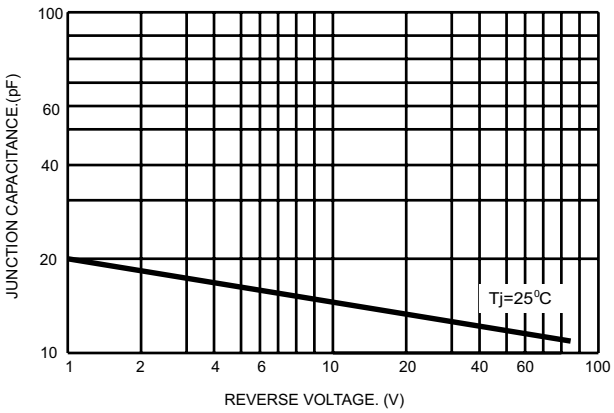


FIG.5- REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM