

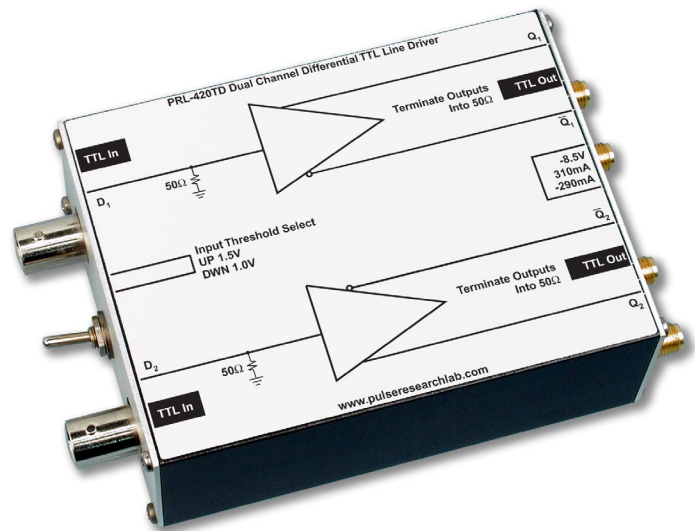
# PRL-420TD DUAL CHANNEL DIFFERENTIAL TTL LINE DRIVER

## APPLICATIONS

- Converting TTL/CMOS signals to Differential TTL Signals
- Converting TTL/CMOS Signals to RS422 Signals
- High Speed Digital Communications Systems Testing
- Differential Long Line Drivers

## FEATURES

- $f_{\max} > 250$  MHz
- 1.2ns Typical Output Rise & Fall Times
- TTL Compatible 50 $\Omega$  Input
- 1.5V or 1V Selectable Input Threshold
- Complementary 50 $\Omega$  Outputs
- BNC Input/SMA Output Connectors
- DC Coupled I/O's
- Self-contained 1.3 x 2.9 x 3.9-in. unit including an AC/DC Adaptor



## DESCRIPTION

The PRL-420TD is a dual channel single-ended input, differential output TTL Line Driver. Each channel has a 50 $\Omega$  TTL/CMOS compatible input and a pair of differential 50 $\Omega$  outputs for driving long lines, in excess of 100ft, with or without 50 $\Omega$  terminations. The input threshold voltage can be selected between 1.5V and 1V using a front panel switch. The 1V threshold makes easy interfacing with 3.3V TTL/CMOS devices.

The PRL-420TD is intended for use in testing and interfacing of high speed digital communication circuits, where conversion from single-ended TTL/CMOS level signals to differential signals is often required. The differential outputs are ideal for driving RS422 input circuits and for high speed A/D's where differential clock input is often required. The PRL-420TD complements other PRL-series Level Translators, such as the PRL-420ND/PD, PRL-450ND/PD, and PRL-460NPD/PND, etc., in systems integration applications where interconnections among different logic signals are often necessary.

The PRL-420TD is a ready-to-use functional module housed in a 1.3 x 2.9 x 3.9-in. extruded aluminum enclosure and is supplied with a  $\pm 8.5$ V AC/DC Adaptor. BNC input and SMA output connectors are provided. A block diagram showing the equivalent input and output circuits of the PRL-420TD is shown in Fig. 1.

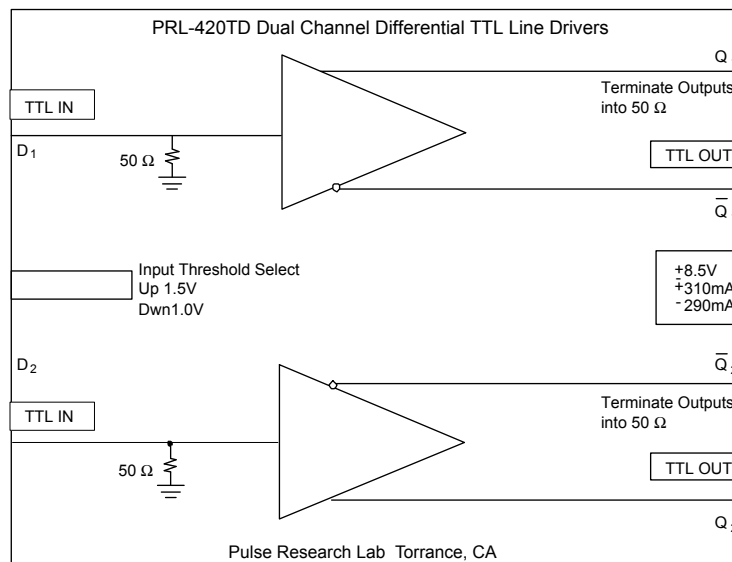


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## SPECIFICATIONS (0° C ≤ T<sub>A</sub> ≤ 35° C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50Ω.

SYMBOL	PARAMETER	Min	Typ	Max	UNIT	Comments
R <sub>in</sub>	Input Resistance	49.5	50	50.5	Ω	
R <sub>out</sub>	Output Resistance	49.5	50	50.5	Ω	
V <sub>TOSH</sub>	Input Threshold Voltage (high)	1.4	1.5	1.6	V	
V <sub>TOSL</sub>	Input Threshold Voltage (low)	0.9	1	1.1	V	
V <sub>IL</sub>	TTL input Low Level	-0.5	0	0.5	V	
V <sub>IHH</sub>	TTL input High Level	1.8	2	5	V	V <sub>TOSH</sub>
V <sub>IHL</sub>	TTL input High Level	1.2	1.3	5	V	V <sub>TOSL</sub>
V <sub>OL</sub>	TTL Output Low Level	-0.1	0	0.5	V	
V <sub>OH</sub>	TTL Output High Level	2	2.2	2.4	V	
I <sub>DC</sub>	DC Input Currents		310 -285	330 -310	mA mA	
V <sub>DC</sub>	DC Input Voltages	±7.5	±8.5	±12	V	
V <sub>AC</sub>	AC/DC Adaptor Input Voltage	103	115	127	V	
T <sub>PLH</sub>	Propagation Delay to output ↑		2		ns	
T <sub>PHL</sub>	Propagation Delay to output ↓		2		ns	
t <sub>r</sub> /t <sub>f</sub>	Rise/Fall Times (10%-90%)		1.2	1.4	ns	Note (1)
T <sub>SKEW</sub>	Skew between any 2 outputs		150	400	ps	
f <sub>max</sub>	Max Clock Frequency	250	300		MHz	Note (2)
Size		1.3x2.9x3.9			in.	
Weight		5			Oz	



**PRL-420TD Block Diagram**

### Notes:

(1). The output rise and fall times are measured with both the Q and  $\bar{Q}$  outputs terminated into 50Ω. If an unused complementary output is left unterminated, a slight increase in rise and fall times will result.

(2). f<sub>MAX</sub> is measured by connecting its inputs to the PRL450ND, ECL to TTL Logic Level Translator, and its outputs to the PRL-350ECL comparator. The input threshold voltage of the PRL-350ECL is set to 2V. The outputs of the PRL-350ECL are divided by two using the PRL-255. The outputs of the PRL 255 are then measured using the PRL-550NQ5X, four channel ECL Terminators, connected to a 50Ω input sampling 'scope.



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