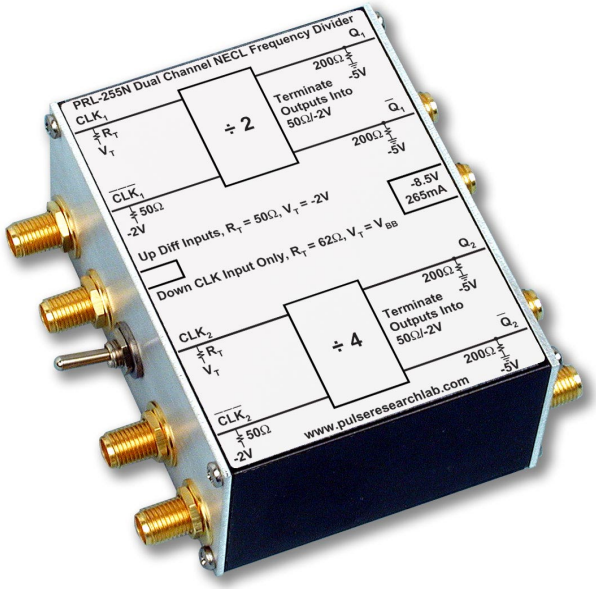
PRL-255N/P ÷2 and ÷4 NECL/PECL FREQUENCY DIVIDERS

APPLICATIONS

- GHz Frequency Division in Device Test and Systems Integration
- High speed Clock signal Generation for SONET applications
- An Essential Lab Tool for Working with GHz NECL/PECL Circuits

FEATURES

- 3 GHz Toggle Frequency
- Single-ended or Differential Inputs
- Internal 50 Ω/V_{TT} Input Terminations
- Complementary Outputs drive 50 Ω Loads terminated to V_{TT}, AC coupled or floating 50 Ω Loads
- DC Coupled I/O's Compatible with ECLinPS or 10KH Devices
- BNC or SMA I/O Connectors
- Ready-to-Use 1.3 x 2.9 x 2.2-in. Module includes a ±8.5V AC/DC Adaptor



PRL-255N NECL Frequency Divider

DESCRIPTION

The PRL-255N and PRL-255P are, respectively, NECL and PECL frequency divider modules, each containing ÷2 and a ÷4 frequency dividers capable of toggling at frequencies in excess of 3GHz. The module can also provide the ÷8 function by cascading the two dividers. The PRL-255N and the PRL-255P are essential lab tools for device test and systems integration in wireless and digital communications applications.

Each divider in the module has differential inputs and complementary outputs. A common switch selects either single-ended or differential inputs. In the differential input mode, both inputs CLK and $\overline{CLK}$ are terminated internally into 50Ω/V_{TT}, where V_{TT} is equal to -2V for NECL and +3V for PECL, and, therefore, either one or both inputs can accept AC coupled signals as well. In the single input mode, input signals should be connected to the CLK inputs only. The $\overline{CLK}$ inputs are internally switched to V_{BB}, nominally -1.3Vfor NECL and +3.7V for PECL, and input resistors R_T's for the $\overline{CLK}$ input channels are changed to 62Ω. Complementary outputs of both channels are designed for driving 50Ω loads terminated into V_{TT}, AC coupled or floating 50Ω loads.

Either output from the PRL-255N can drive a single-ended NECL input. The PRL-255P complementary outputs, however, must be used together for driving differential PECL inputs only, because the reduced output logic swing of 400mVp-p, due to short circuit protection reasons, is not logic level compatible with single-ended PECL input.

Block diagrams of the PRL-255N and PRL-255P are shown in Figs. 1A and 1B.

The PRL-255N and PRL-255P are each housed in a 1.3 x 2.9 x 2.2-in. extruded aluminum enclosure and is supplied with a ±8.5V/1A AC/DC Adaptor.

If mounting is desired, a pair of 35001420 mounting brackets can accommodate two PRL modules of the same length. A number of PRL modules can also share a single ±8.5V AC/DC adaptor using the PRL-730 or PRL-746 voltage distribution module. Please see the Accessories Section for more detail.

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*SPECIFICATIONS (0^{o} C ≤ T_A ≤ 35^{o}C)

Unless otherwise specified, dynamic measurements are made with all outputs terminated into 50 Ω/V_{TT}

SYMBOL	PARAMETER	PRL-255N			PRL-255P			UNIT
		Min	Typical	Max	Min	Typical	Max	
R_{in}	Input Resistance	49.5	50	50.5	49.5	50	50.5	Ω
V_{TT}	D Input Termination Voltage (fixed)	-2.2	-2	-1.8	2.7	3	3.3	V
V_T	$\overline{D}$ Input Termination Voltage (variable)	-1.17/-2.2	-1.3/-2	-1.43/-1.8	3.33/2.7	3/3.7	4.07/3.3	V
V_{IL}	Input Lo Voltage	-1.95	-1.6	-1.48	3.05	3.4	3.52	V
V_{IH}	Input Hi Voltage	-1.13	-0.9	-.81	3.87	4.1	4.19	V
V_{OL}	Output Lo Voltage	-1.95	-1.7	-1.48	3.0	3.15	3.3	V
V_{OH}	Output Hi Voltage	-1.13	-0.9	-.81	3.4	3.55	3.8	V
I_{DC}	DC Input Current		-250	-265		240	265	mA
V_{DC}	DC Input Voltage	-7.5	-8.5	-12	7.5	8.5	12	V
V_{AC}	AC/DC Adaptor Input Voltage	103	115	127	103	115	127	V
t_{PLH} (÷2)	Propagation Delay to output ↑		1.1	1.5		1.1	1.5	ns
t_{PHL} (÷2)	Propagation Delay to output ↓		1.1	1.5		1.1	1.5	ns
t_{PLH} (÷4)	Propagation Delay to output ↑		1.25	1.65		1.25	1.65	ns
t_{PHL} (÷4)	Propagation Delay to output ↓		1.25	1.65		1.25	1.65	ns
t_r/t_f	Rise/Fall Times (20%-80%)(1)		325	425		325	425	ps
t_{SKEW}	Skew between Q& $\overline{Q}$ outputs		20	75		20	75	ps
f_{MAX}	Max clock frequency(3)	2.5	3.2		2.5	3.2		GHz
V_{CMR}	Common Mode Range(2)	-2.7		-0.4	2.5		4.6	V
	Size	1.3 x 2.9 x 2.2			1.3 x 2.9 x 2.2			in.
	Weight	5			5			Oz

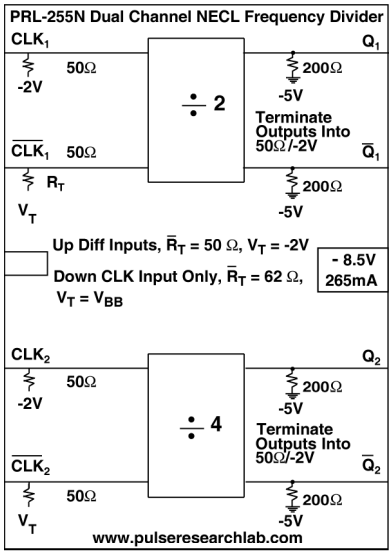

Fig. 1A: PRL-255N Block Diagram

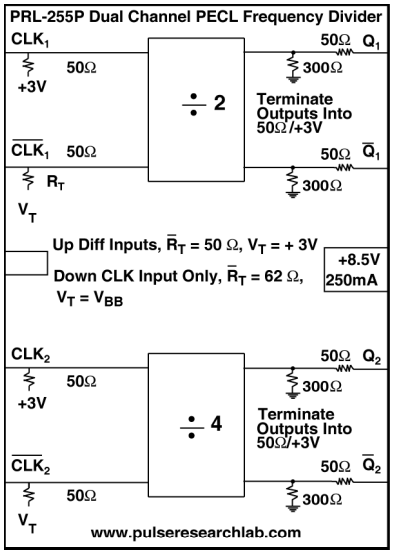

Fig. 1B: PRL-255P Block Diagram

*All measurements are made with outputs terminated into 50Ω/V_{TT}, using the PRL-550NQ4X/PQ4X, four-channel NECL/PECL Terminator, connected to a 50Ω input sampling oscilloscope.

Notes:

(1). The output rise and fall times are measured with all outputs terminated into 50Ω /V_{TT}. For best performance, all outputs should be terminated into 50Ω/V_{TT} or AC coupled into a 50Ω loads. However, if only one pair of complementary outputs is used, the other pair may be left unterminated. If a single output is used, one other complementary output must be terminated; otherwise, output waveform distortion and rise time degradation will occur. Use the PRL-550NQ/PQ4X, four channel NECL/PECL Terminators, respectively, for the 50 Ω/V_{TT} termination and for connection of NECL/PECL signals to 50Ω input oscilloscopes. If preservation of DC levels is not required, then the 56003265-1, 0.1 µf DC block or the 56003270-2 12 dB AC-coupled attenuator may be used to connect the NECL/PECL outputs to 50 Ω input instruments.

(2). These parameters are not supplied by the device manufacturer and are, therefore, not guaranteed.

(3). fMAX is measured by AC coupling a sine wave to the ÷2 CLK input using the differential input mode (switch up). The ÷2 and the ÷4 dividers are cascaded, and the ÷8 outputs are then measured. The fMAX measurement is then repeated by clocking the ÷4 CLK input with the sine wave.

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