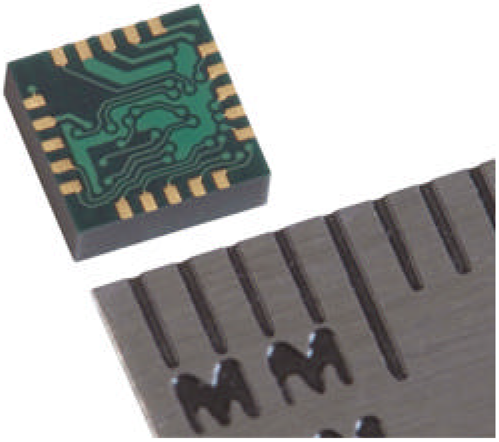
Honeywell

3-Axis Digital Compass IC
HMC5843

Advanced Information

The Honeywell HMC5843 is a surface mount multi-chip module designed for low field magnetic sensing with a digital interface for applications such as low cost compassing and magnetometry. The HMC5843 includes our state of the art 1043 series magneto-resistive sensors plus Honeywell developed ASIC containing amplification, strap drivers, offset cancellation, 12-bit ADC and an I^2C serial bus interface. The HMC5843 is in a 4.0 by 4.0 by 1.3mm surface mount leadless chip carrier (LCC). Applications for the HMC5843 include Consumer Electronics, Auto Navigation Systems, Personal Navigation Devices, and Magnetometers.



The HMC5843 utilizes Honeywell's Anisotropic Magnetoresistive (AMR) technology that provides advantages over other magnetic sensor technologies. The sensors feature precision in-axis sensitivity and linearity, solid-state construction with very low cross-axis sensitivity designed to measure both direction and magnitude of Earth's magnetic fields, from tens of micro-gauss to 6 gauss. Honeywell's Magnetic Sensors are among the most sensitive and reliable low-field sensors in the industry.

Honeywell continues to maintain product excellence and performance by introducing innovative solid-state magnetic sensor solutions. These are highly reliable, top performance products that are delivered when promised. Honeywell's magnetic sensor solutions provide real solutions you can count on.

FEATURES	BENEFITS
▸ 3-Axis Magnetoresistive Sensors and ASIC in a Single Package	▸ Small Size for Highly Integrated Products. Just Add a Micro-Controller Interface, Plus Two External SMT Capacitors
▸ Low Cost	▸ Designed for High Volume, Cost Sensitive OEM Designs
▸ 4.0 x 4.0 x 1.3mm Low Height Profile LCC Surface Mount Package	▸ Easy to Assemble & Compatible with High Speed SMT Assembly
▸ Low Voltage Operations (2.4 to 3.3V)	▸ Compatible for Battery Powered Applications
▸ Built-In Strap Drive Circuits	▸ Set/Reset and Offset Strap Drivers for Degaussing, Self Test, and Offset Compensation
▸ I^2C Digital Interface	▸ Popular Two-Wire Serial Data Interface for Consumer Electronics
▸ Lead Free Package Construction	▸ Complies with Current Environmental Standards
▸ Wide Magnetic Field Range (+/-6 Oe)	▸ Sensors Can Be Used in Strong Magnetic Field Environments
▸ Available in Tape & Reel Packaging	▸ High Volume OEM Assembly

SPECIFICATIONS

Characteristics	Conditions*	Min	Typ	Max	Units
Power Supply					
Supply Voltage	AVDD Referenced to AGND	2.4	3.0	3.3	Volts
	DVDD Referenced to DGND	1.62		1.98	Volts
Current Draw	ASIC Only – Sleep Mode (dual supplies)	-	2	-	uA
	ASIC Only – Idle Mode (dual supplies)	-	180	-	uA
	ASIC and Sensors – Measurement Mode (dual supplies, default register modes) AVDD = 3.3 volts, DVDD = 1.98 volts	-	2	-	mA
Magnetic Sensors					
Field Range	Full scale (FS) – total applied field	-4		+4	gauss
Cross-Axis Sensitivity	Cross field = 0.5 gauss, Happlied = ±3 gauss		±0.2%		%FS/gauss
Disturbing Field	Sensitivity starts to degrade. Use S/R pulse to restore sensitivity.			20	gauss
Max. Exposed Field	No perming effect on zero reading			10000	gauss
ASIC Digital					
Measurement Period	Output Rate = 50Hz (10Hz typ.)		-	10	msec
I^2C Address	7-bit address		0x1E		hex
	8-bit read address		0x3D		hex
	8-bit write address		0x3C		hex
I^2C Rate	Controlled by I^2C Master	-10		+10	%
I^2C bus pull-up	Internal passive resistors		50		kilo-ohms
I^2C Hysteresis	Hysteresis of Schmitt trigger inputs on SCL and SDA - Fall (DVDD=1.8V)		0.603		Volts
	Rise (DVDD=1.8V)		1.108		Volts
Mux/Amplifier Section					
Mag Dynamic Range	3-bit gain control	±0.7	±1.0	±4	gauss
Linearity	Full scale input range			0.1	±% FS
Output Noise	100 sample standard deviation			TBD	Bit
Gain Tolerance	All gain/dynamic range settings		±5		%
Bandwidth	-3dB point		10		kHz
ADC Section					
Resolution	3-bit gain control		TBD		μgauss
Signal-to Noise Ratio		70			dB
General					
ESD Voltage				700	V
Operating Temperature	Ambient	-30		85	°C
Storage Temperature	Ambient, unbiased	-40		125	°C
Weight	Nominal		TBD		milli-grams

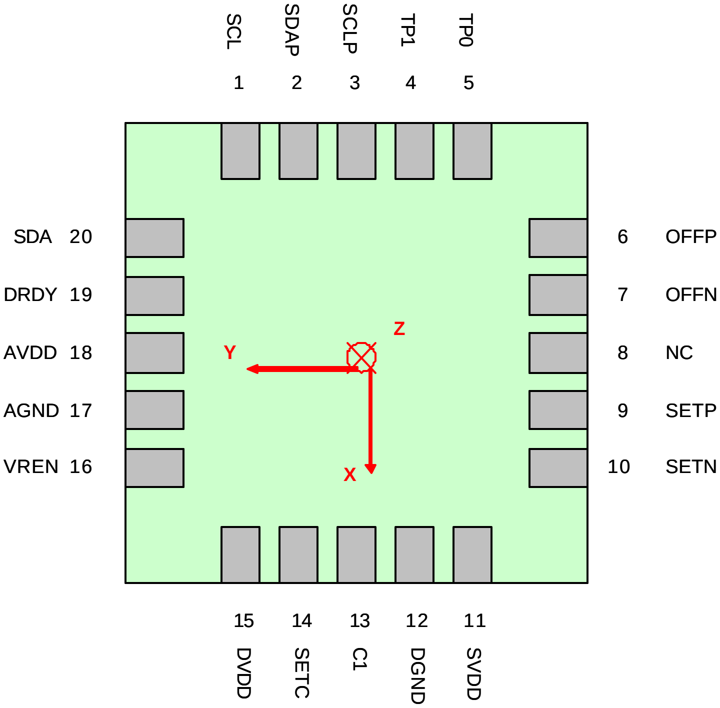
* Tested at 25°C except stated otherwise.

PIN CONFIGURATIONS

(Arrow indicates direction of applied field that generates a positive output voltage after a SET pulse.)

Pin	Name	Description
1	SCL	Serial Clock – I2C Master/Slave Clock
2	SDAP	Serial Data Pull-up Resistor – 50k-ohm to VDD
3	SCLP	Serial Clock Pull-up Resistor – 50k-ohm to VDD
4	TP1	Test Point One – Factory Test Use Only - NC
5	TP0	Test Point Zero – Factory Test Use Only - NC
6	OFFP	Offset Strap Positive
7	OFFN	Offset Strap Negative
8	NC	No Connection
9	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
10	SETN	Set/Reset Strap Negative – Test Point
11	SVDD	Sensor Supply – Test Point
12	DGND	Digital Supply Ground/Return
13	C1	Reservoir Capacitor (C1) Connection
14	SETC	S/R Capacitor (C2) Connection – Driver Side
15	DVDD	Digital Positive Supply
16	VREN	Voltage Regulator Enable, (GND = Dual Supply, AVDD = Single Supply)
17	AGND	Analog Supply Ground/Return
18	AVDD	Analog Positive Supply
19	DRDY	Data Ready – Test Point
20	SDA	Serial Data – I2C Master/Slave Data

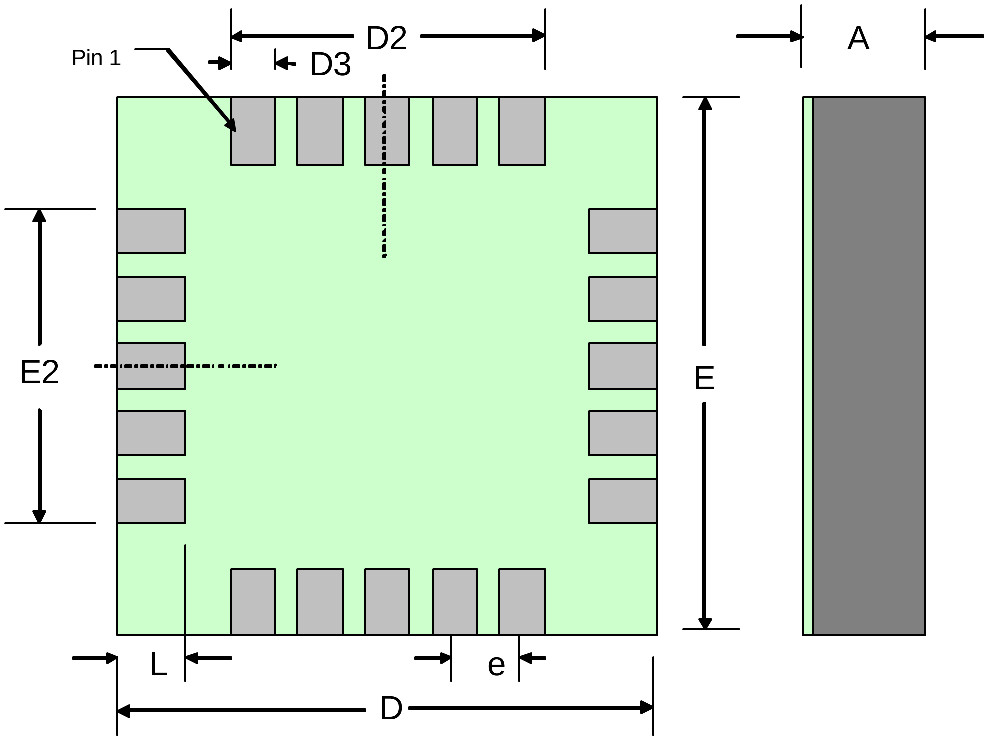
Table 1: Pin Configurations



HMC5843 – bottom view

PACKAGE OUTLINES

PACKAGE DRAWING HMC5843 (20-PIN LPCC, dimensions in millimeters)



HMC5843 – bottom view

Sym	Min	Nom	Max
A	1.20	1.36	1.46
D		4.0 BSC	
D2		2.25	
D3		0.25 x 20 pins	
E		4.0 BSC	
E2		2.25	
e		0.50 Basic	
L		0.40 x 20 pins	

MOUNTING CONSIDERATIONS

The following is the recommend printed circuit board (PCB) footprint for the HMC5843.

PCB Pad Definition and Traces

The HMC5843 is a fine pitch LCC package with a 0.50mm pin pitch (spacing), with the pin pads defined as 0.40mm by 0.25mm in size. PCB pads are recommended to be oversized by 0.025mm from each pad for a short dimension oversize of 0.05mm. The interior PCB pad is recommended to be 0.05mm oversized per pin with an exterior oversize of 0.20mm for proper package centering and to permit test probing. Lead finish is SnAgCu. Size the traces between the HMC5843 and the external capacitors (C1 and C2) to handle the 1 ampere peak current pulses with low voltage drop on the traces.

Stencil Design and Solder Paste

A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

Pick and Place

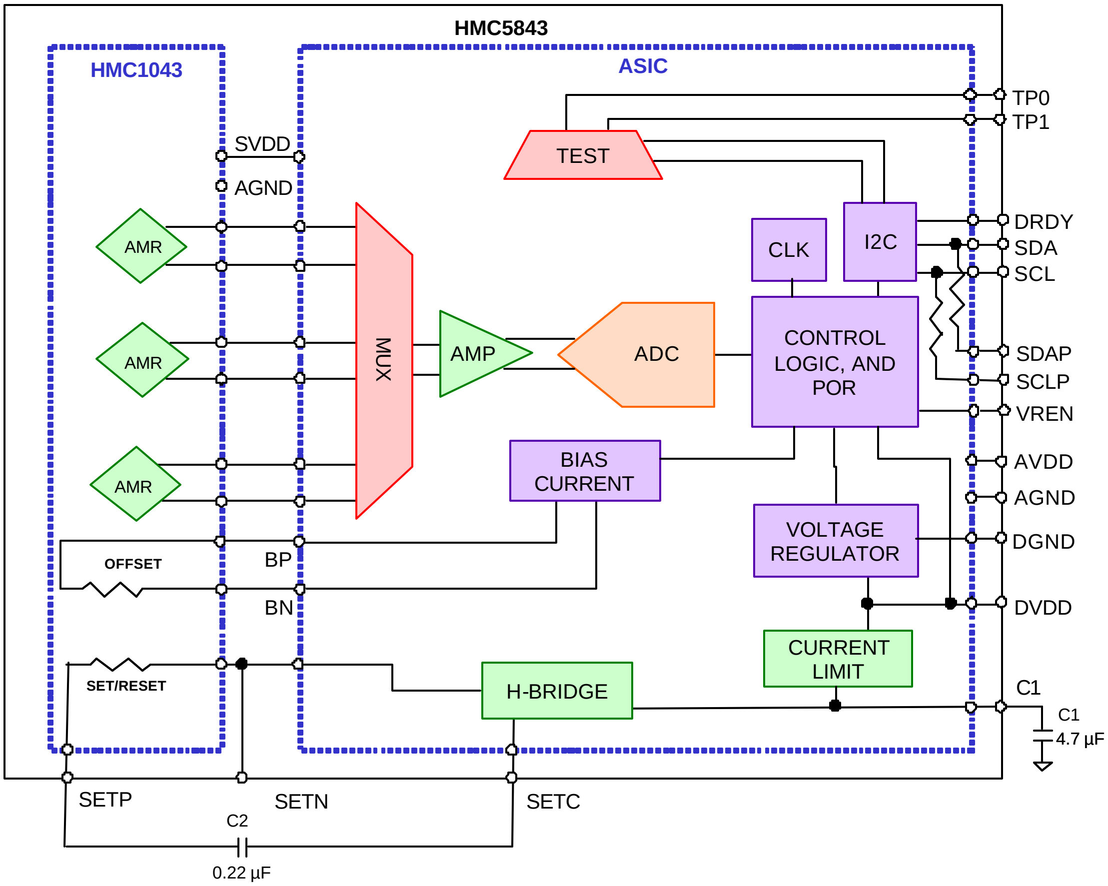
Placement is machine dependant and no restrictions are recommended, and have been tested with mechanical centering. Placement force should be equivalent 1206 SMT resistors and enough force should be used to squeeze the paste out from the package/contact pad overlap and to keep the package pin contacts vertical.

Reflow and Rework

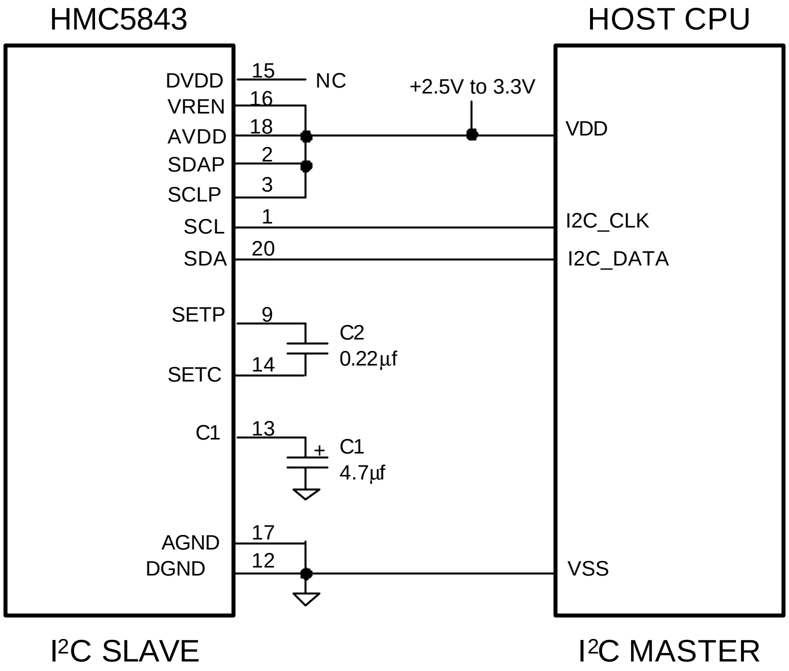
No special profile is required for the HMC5843 and compatible with lead eutectic and lead-free solder paste reflow profiles. Honeywell recommends the adherence to solder paste manufacturer's guidelines. The HMC5843 may be reworked with soldering irons, but extreme care must be taken not to overheat the copper pads from the part's fiberglass substrate. Irons with a tip temperature no greater than 315°C should be used. Excessive rework risks the copper pads pulling away into the molten solder.

INTERNAL SCHEMATIC DIAGRAM

HMC5843



SINGLE SUPPLY REFERENCE DESIGN



BASIC DEVICE OPERATION

Anisotropic Magneto-Resistive Sensors

The Honeywell HMC5843 magnetoresistive sensor circuit is a trio of sensors and application specific support circuits to measure magnetic fields. With power supply applied, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output. The magnetoresistive sensors are made of a nickel-iron (Permalloy) thin-film deposited on a silicon wafer and patterned as a resistive strip element. In the presence of a magnetic field, a change in the bridge resistive elements causes a corresponding change in voltage across the bridge outputs.

These resistive elements are aligned together to have a common sensitive axis (indicated by arrows on the pinouts) that will provide positive voltage change with magnetic fields increasing in the sensitive direction. Because the output only is in proportion to the one-dimensional axis (the principle of anisotropy) and its magnitude, additional sensor bridges placed at orthogonal directions permit accurate measurement of arbitrary field direction. The combination of sensor bridges in two and three orthogonal axis permit applications such as compassing and magnetometry.

Offset Strap

The offset strap is a spiral of metallization that couples in the sensor element's sensitive axis. The offset strap measures nominally 13 ohms, and requires 10mA for each gauss of induced field. The straps will easily handle currents to buck or boost fields through the ±6 gauss linear measurement range, but designers should note the extreme thermal heating on the sensor die when doing so.

With most applications, the offset strap is not utilized and can be ignored. Designers can leave one or both strap connections (Off- and Off+) open circuited, or ground one connection node. Do not tie both strap connections together to avoid shorted turn magnetic circuits.

Set/Reset Strap

The set/reset strap is another spiral of metallization that couples to the sensor elements easy axis (perpendicular to the sensitive axis on the sensor die. Each set/reset strap has a nominal total resistance of 2.25 ohms with a nominal required peak current of 800mA for reset or set pulses. With rare exception, the set/reset strap must be used to periodically condition the magnetic domains of the magneto-resistive elements for best and reliable performance.

ASIC Description

The ASIC has inputs for three differential signals from Honeywell's magneto-resistive sensors. The sensors' signals are multiplexed (MUX) into the instrumentation amplifier (AMP), which is then fed into an analog to digital converter (ADC). The logic block controls system timing, I^2C interface, Set/Reset function, and bias current generator. The ASIC is developed by Honeywell for use specifically for our magnetoresistive sensors.

Instrumentation Amplifier (AMP)

The Instrumentation amplifier is used to amplify differential signals from the magnetic sensors. The output impedance from each channel of the sensor is typically 1kO. Differential signal into the instrumentation amplifier is in the mV range and common mode signal is near AVDD / 2. Typical operation for the sensors is near DC.

Multiplexer (MUX)

The multiplexer is used to MUX the signals from the sensors. The MUX is a low noise device, and the power-on default state for the MUX is channel 1.

Analog to Digital Converter (ADC)

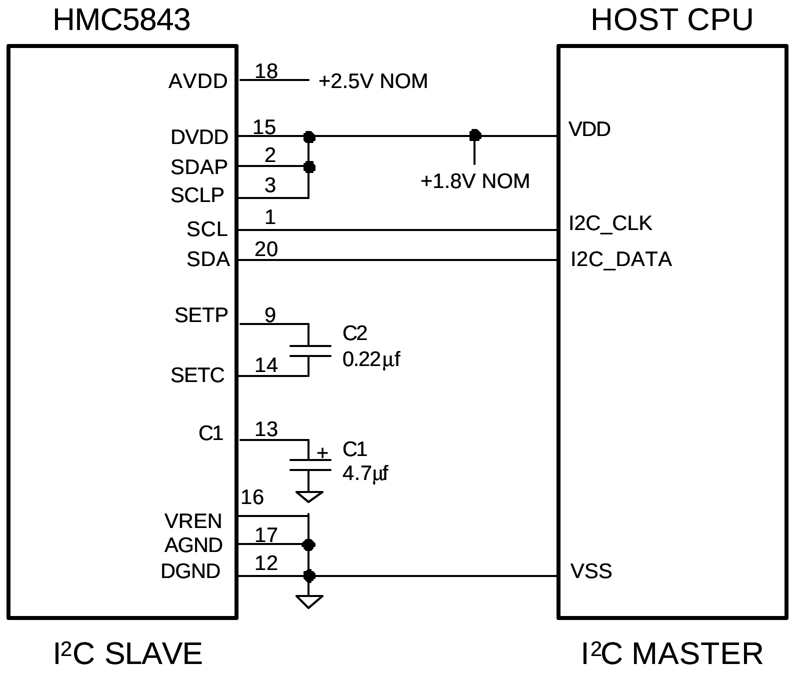
The ADC converts the analog signals from the amplifier into digital signals. The ADC resolution is 12 bits.

Power Management

This device is capable of operating with a single supply (AVDD) or dual supplies (AVDD and DVDD). Pin VREN makes this selection by enabling the internal digital supply voltage regulator. When VREN is tied to AVDD, the device is in single supply operation; this device is powered from AVDD; and the internal voltage regulator is enabled. When VREN is tied to AGND this devices operates with both AVDD and DVDD as supplies. The table below shows the modes available at the various power supply conditions.

DVDD	**AVDD**	**Pin VREN**	**Modes Supported**	**Description**
High	High	AGND	All, except Off	Internal voltage regulator: Disabled. Digital I/O pins: Range from DGND to DVDD. Device fully functional. Digital logic blocks are powered from DVDD supply, including all on-board clocks.
High	Low	AGND	Idle, Sleep	Internal voltage regulator: Disabled. Digital I/O pins: Range from DGND to DVDD. Device Measurement functionality not supported. Device I^{2}C bus and register access supported.
Internally regulated	High	AVDD	All, except Off	Internal voltage regulator: Enabled Digital I/O pins: Range from AGND to AVDD Device fully functional. Digital logic blocks are powered through on-board regulator.
Low	Low	--	Off	Device in off mode.

Table 2: Operational Modes and Supply States



DUAL SUPPLY REFRENCE DESIGN

ASIC Turn-On Times

The table below shows the turn-on time for individual functions within this ASIC.

Parameter	Sym.	Condition	Min	Typ	Max	Units
Clock Turn-on	t_{CLK_ON}	Stabilized			4.5	ms
Logic Turn-on	t_{LOG_ON}	Register values and DRDY pin defined			0.5	ms
Analog Turn-on	t_{ANL_N}	Includes ADC, Amplifier, MUX. Capable of completing an ADC conversion within specifications.			0.5	ms
Voltage Regulator Turn-on	t_{VR_ON}	Enabled and stable			5	ms

Table 3: Turn-On Times

Voltage Regulator

This ASIC has an internal voltage regulator which, depending on the application needs, may be used instead of supplying voltage to pin DVDD. If DVDD pin is used, the internal voltage regulator is not engaged. When both supplies are used, DVDD is typically high before AVDD, but no latch-up conditions will exist if DVDD is brought high after AVDD.

Power on Reset

Power on reset (POR) circuit shall return the device to the power-on default state. All registers shall be returned to their default values. Circuitry shall return to it default state, such as, but not limited to: MUX channel, ADC state machine, and bias current.

I^2C Interface

Control of this device is carried out via the I^2C bus. This device will be connected to this bus as a slave device under the control of a master device, such as the processor.

This device shall be compliant with *I^2C-Bus Specification*, document number: 9398 393 40011. As an I^2C compatible device, this device has a 7-bit serial address and supports I^2C protocols. This device shall support standard and fast modes, 100kHz and 400kHz respectively, but cannot support the high speed mode (Hs). External pull-up resistors are required to support these standard and fast speed modes. Depending on the application, the internal pull-ups may be used to support slower data speeds than specified by I^2C standards. This device does not contain 50nsec spike suppression as required by fast mode operation in the I^2C-Bus Specification, “Table 4 Characteristics of the SDA and SCL I/O stages for F/S-mode I^2C-bus devices”.

Activities required by the master (register read and write) have priority over internal activities, such as the measurement. The purpose of this priority is to not keep the master waiting and the I^2C bus engaged for longer than necessary.

I^2C Pull-up Resistors

Pull-up resistors are placed on the two I^2C bus lines. Typically these resistors are off-chip, but, to conserve board space in specific low clock speed applications, they are internal to this device.

Internal Clock

The device has an internal clock for internal digital logic functions and timing management.

H-Bridge for Set/Reset Strap Drive

The ASIC contains large switching FETs capable of delivering a large but brief pulse to the Set / Reset strap of the sensor. This strap is largely a resistive load.

Charge Current Limit

The current that reservoir capacitor (C1) can draw when charging is limited. When using dual supplies this device shall limit the current drawn from DVDD source to charge this capacitor. When only a single supply is used, Pin DVDD is externally tied to pin C1. In this configuration, current is still limited. For example, the internal voltage regulator will limit this current draw.

Bias Current Generator

The bias current generator is used to apply a bias current to the offset strap of the magneto-resistive sensor, which creates an artificial magnetic field bias on the sensor. This function is enabled and the polarity is set by bits MS[n] in the configuration register. The bias current generator generates dc current supplied from the AVDD supply.

MODES OF OPERATION

This device has several modes whose primary purpose is power management. This section describes these modes.

Continuous-Measurement Mode

During continuous-measurement mode, the device continuously makes measurements and places measured data in data output registers. Settings in the configuration register affect the data output rate (bits DO[n]), the measurement configuration (bits MS[n]), the gain (bits GN[n]), and the delay (bits DL[n]) when in continuous-measurement mode. To conserve current between measurements, the device is placed in a state similar to idle mode, but the mode is not changed to idle mode. That is, MD[n] bits are unchanged. Data can be re-read from the data output registers if necessary; however, if the master does not ensure that the data register is accessed before the completion of the next measurement, the new measurement may be lost. All registers maintain values while in continuous-measurement mode. The I^2C bus is enabled for use by other devices on the network in while continuous-measurement mode.

Single-Measurement Mode

This is the default single supply power-up mode. In dual supply configuration this is the default mode when AVDD goes high. During single-measurement mode, the device makes a single measurement and places the measured data in data output registers. Settings in the configuration register affect the measurement configuration (bits MS[n]), the gain (bits GN[n]), and the delay (bits DL[n]) when in single-measurement mode. After the measurement is complete and output data registers are updated, the device is placed sleep mode, and the mode register *is* changed to sleep mode by setting MD[n] bits. All registers maintain values while in single-measurement mode. The I^2C bus is enabled for use by other devices on the network while in single-measurement mode.

Idle Mode

During this mode the device is accessible through the I^2C bus, but major sources of power consumption are disabled, such as, but not limited to, the ADC, the amplifier, the SVDD pin, and the sensor bias current. All registers maintain values while in idle mode. The I^2C bus is enabled for use by other devices on the network while in idle mode.

Sleep Mode

This is the default dual supply power-up mode when only DVDD goes high and AVDD remains low. During sleep mode the device functionality is limited to listening to the I^2C bus. The internal clock is not running and register values are not maintained while in sleep mode. The only functionality that exists during this mode is the device is able to recognize and execute any instructions specific to this device but does not change from sleep mode due to other traffic on the I^2C bus. The I^2C bus is enabled for use by other devices on the network while in sleep mode. This mode has two practical differences from idle mode. First this state will create less noise on system since the clock is disabled, and secondly this state is a lower current consuming state since the clock is disabled.

Off Mode

During off mode device is off. No device functionality exists. Both AVDD and DVDD are low. The I^2C bus is enabled for use by other devices on the network in off mode. In this mode the I^2C pins shall be in a high impedance state.

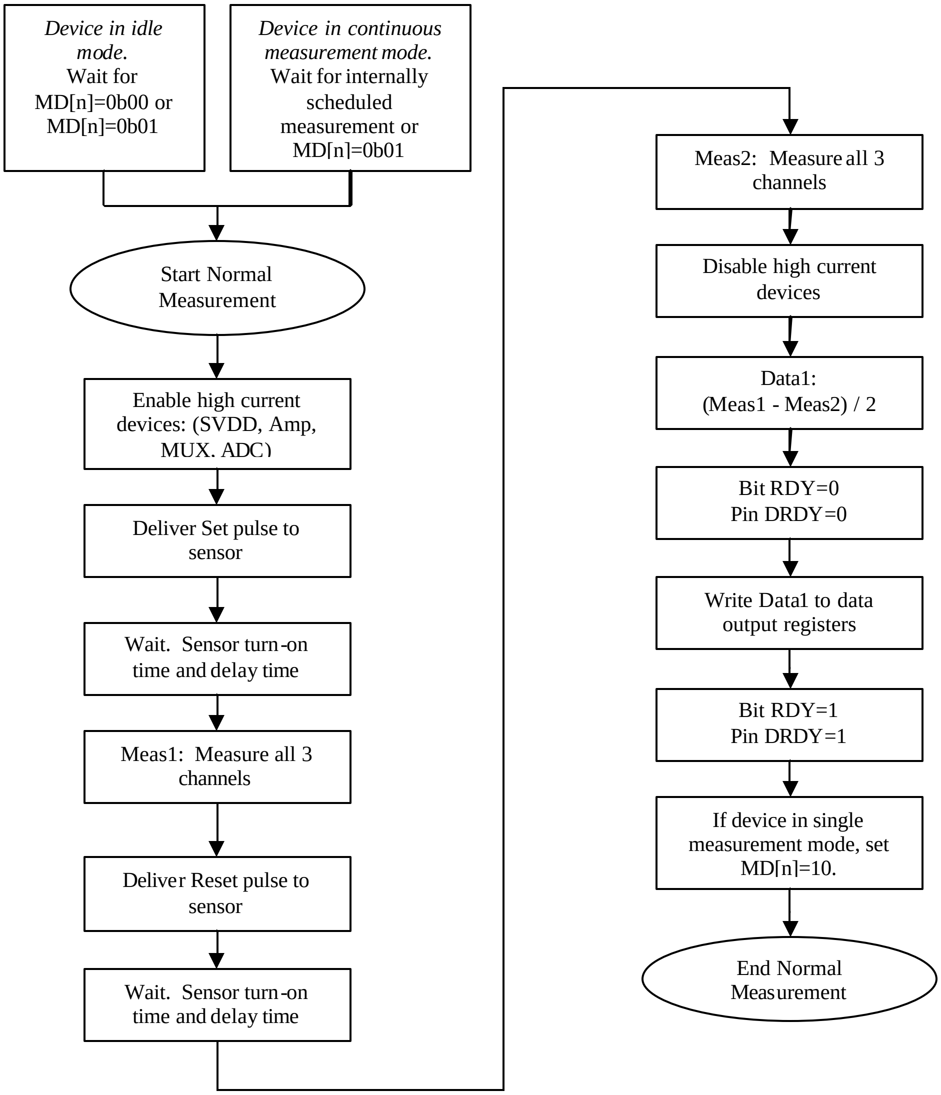
MAGNETIC MEASUREMENTS

The measurement type is set by bits MS[n] in the configuration registers. There are two main configurations, normal measurement and bias measurement, where the self-test bias measurement can be a positive or a negative bias current on the offset strap to emulate an external magnetic field. The gain, GN[n]; the delay, DL[n]; and the data output rate, DO[n] settings are common to all measurement configurations.

In the normal measurement process, the sensor's and amplifier's differential offset are removed through differencing the sensor's output after a SET pulse and after a RESET pulse. This technique is not used during the bias measurement process. The differencing technique is completed as follows: ([Measurement after Set pulse] – [Measurement after Reset pulse])] / 2.

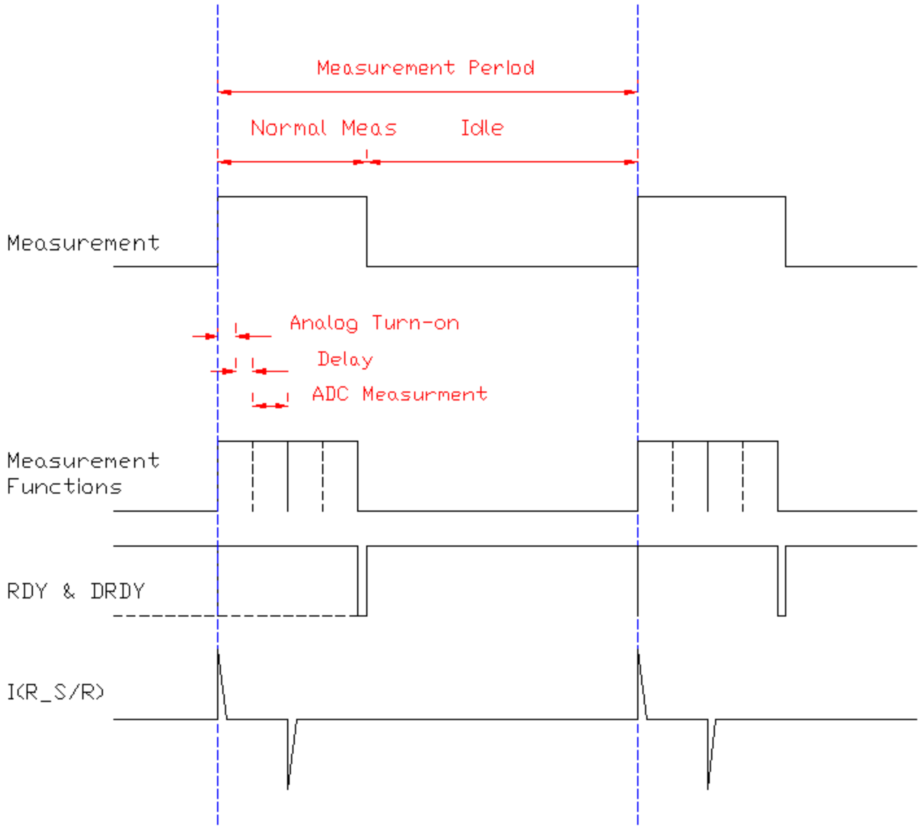
Normal Measurement

The normal measurement is the default measurement configuration. The normal measurement flow is shown in the diagram below.



Normal Measurement Flow Diagram

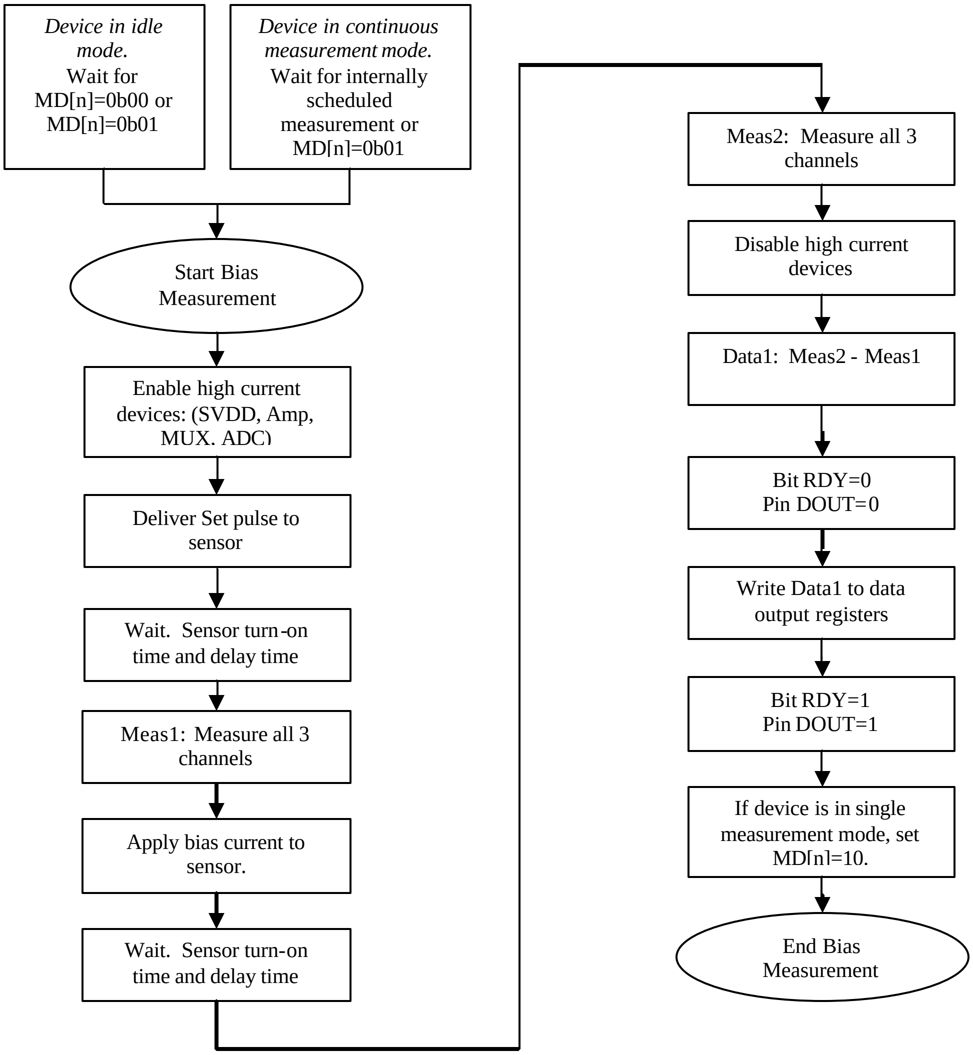
The timing diagram for the normal measurement is shown below. "Normal Meas" defines the timing of the Normal Measurement Flow Diagram below. When the device is in continuous-measurement mode, the time shown as "Idle" defines time the device is in low current state, similar to idle mode. When the device is in single-measurement mode, the time shown as "Idle" defines the time the device is in sleep mode. *Analog Turn-on* time defines the longest of these times: the sensor's turn-on time, the amplifier turn-on time, or the ADC turn-on time. Note that after applying a reset pulse to the sensor, the device shall wait the duration of the sensor's turn-on before making measurements, even though sensor was not powered-down between measurements. I*I(R_S/R)* depicts the current through the sensor strap, $R_{S/R}$.



Normal Measurement Timing

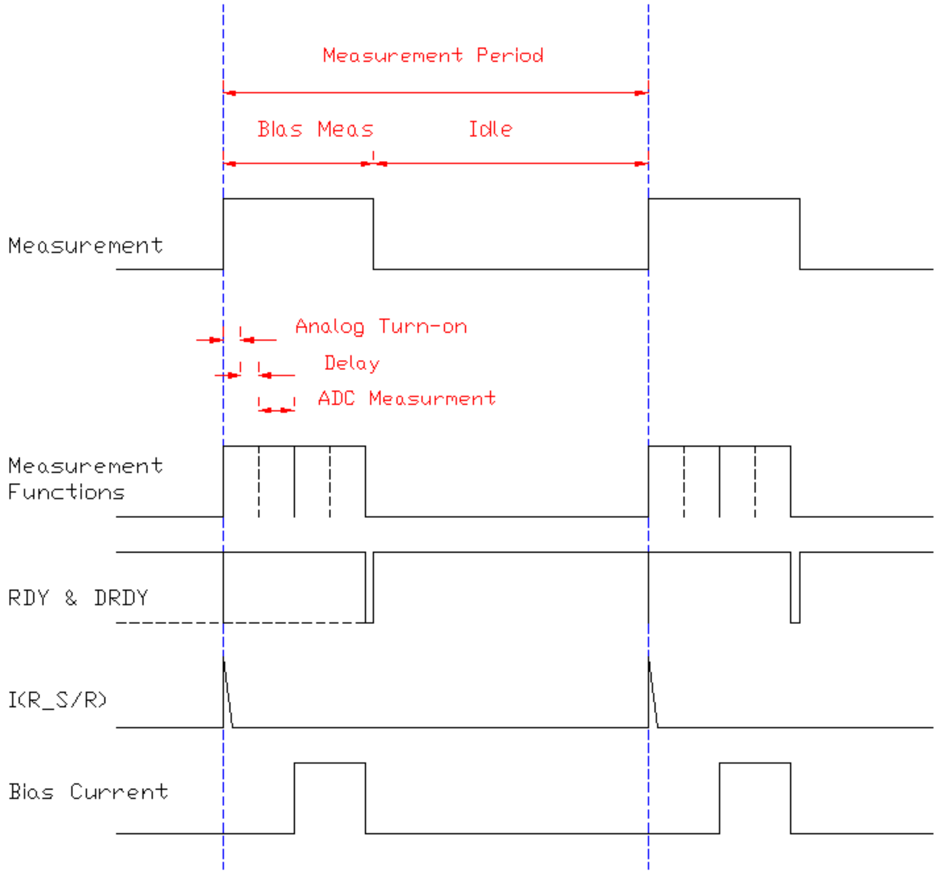
Self-Test Bias Measurement

The self-test bias measurement flow is shown in the diagram below.



Self-Test Bias Measurement Flow Diagram

The timing diagram for both the bias measurement is shown below. “Bias Meas” defines the timing of figure below. When the device is in continuous-measurement mode, the time shown as “Idle” defines time the device is in low current state similar to idle mode. When the device is in single-measurement mode, the time shown as “Idle” defines the time the device is in sleep mode. *Analog Turn-on* time defines the longest of these times: the sensor’s turn-on time, the amplifier turn-on time, or the ADC turn-on time. *I(R_S/R)* depicts the current through the sensor set/reset strap, $R_{S/R}$.



Bias Measurement Timing

REGISTERS

This device is controlled and configured via a number of on-chip registers, which are described in this section. In the following descriptions, *set* implies a logic 1, and *reset* or *clear* implies a logic 0, unless stated otherwise.

Register List

The table below lists the registers and their access. All address locations are 8 bits.

Address Location	Name	Access
00	Configuration Register A	Read/Write
01	Configuration Register B	Read/Write
02	Mode Register	Read/Write
03	Data Output X MSB Register	Read
04	Data Output X LSB Register	Read
05	Data Output Y MSB Register	Read
06	Data Output Y LSB Register	Read
07	Data Output Z MSB Register	Read
08	Data Output Z LSB Register	Read
09	Status Register	Read
10	Identification Register A	Read
11	Identification Register B	Read
12	Identification Register C	Read

Table 5: Register List

Register Access

This section describes the process of reading from and writing to this device. The devices uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit read/write identifier.

To minimize the communication between the master and this device, the address pointer updated automatically without master intervention. This automatic address pointer update has two additional features. First when address 12 or higher is accessed the pointer updates to address 00 and secondly when address 08 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

```
If (address pointer = 08) then address pointer = 03
Else if (address pointer >= 12) then address pointer = 0
Else (address pointer) = (address pointer) + 1
```

The address pointer value itself cannot be read via the I^{2}C bus.
Any attempt to read an invalid address location returns 0's, and any write to an invalid address location or an undefined bit within a valid address location is ignored by this device.

Configuration Register A

The configuration register is used to configure the device for setting the data output rate and measurement configuration. CRA0 through CRA7 indicate bit locations, with *CRA* denoting the bits that are in the configuration register. CRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

CRA7	**CRA6**	**CRA5**	**CRA4**	**CRA3**	**CRA2**	**CRA1**	**CRA0**
(0)	(0)	(0)	DO2 (1)	DO1 (0)	DO0 (0)	MS1 (0)	MS0 (0)

Table 6: Configuration Register A

Location	**Name**	**Description**
CRA7 to CRA5	0	These bits must be cleared for correct operation.
CRA4 to CRA2	DO2 to DO0	Data Output Rate Bits. These bits set the rate at which data is written to all three data output registers.
CRA1 to CRA0	MS1 to MS0	Measurement Configuration Bits. These bits define the measurement flow of the device, specifically whether or not to incorporate an applied bias to the sensor into the measurement.

Table 7: Configuration Register A Bit Designations

The Table below shows minimum output data rates given PVT conditions. All three channels shall be measured within a given data rate.

DO2	**DO1**	**DO0**	**Minimum Data Output Rate (Hz)**
0	0	0	0.5
0	0	1	1
0	1	0	2
0	1	1	5
1	0	0	10 (default)
1	0	1	20
1	1	0	50
1	1	1	Not used

Table 8: Data Output Rates

MS1	MS0	Mode
0	0	Normal measurement configuration (default). In normal measurement configuration the device follows normal measurement flow. Pins BP and BN are left floating and high impedance.
0	1	Positive bias configuration. In positive bias configuration, a positive current is forced across the resistive load on pins BP and BN.
1	0	Negative bias configuration. In negative bias configuration, a negative current is forced across the resistive load on pins BP and BN.
1	1	This configuration is not used.

Table 9: Measurement Modes

Configuration Register B

The configuration register B for setting the device gain and for setting a measurement delay time. CRB0 through CRB7 indicate bit locations, with *CRB* denoting the bits that are in the configuration register. CRB7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

CRB7	CRB6	CRB5	CRB4	CRB3	CRB2	CRB1	CRB0
GN2 (0)	GN1 (0)	GN0 (1)	(0)	DL3 (0)	DL2 (0)	DL1 (0)	DL0 (0)

Table 10: Configuration B Register

Location	Name	Description
CRB7 to CRB5	GN2 to GN0	Gain Configuration Bits. These bits configure the gain for the device. The gain configuration is common for all channels.
CRB4	0	This bit must be cleared for correct operation.
CRB3 to CRB0	DL3 to DL0	Delay Configuration Bits. These bits set the delay time after which pin SVDD and ADC are high before analog to digital conversion begins.

Table 11: Configuration Register B Bit Designations

The table below shows nominal gain settings.

GN2	GN1	GN0	Sensor Input Field Range:	Output Range	LSB (Input Referred)	GN2
0	0	0	Not Recommended			0
0	0	1	Not Recommended			0
0	1	0	Not Recommended			0
0	1	1	Not Recommended			0
1	0	0	±0.7mT	0xF800–0x07FF (-2048–2047)	4.52µV (0.18µT)	1
1	0	1	±0.125mT	0xF800–0x07FF (-2048–2047)	5.19µV (0.21µT)	1
1	1	0	±0.2mT	0xF800–0x07FF (-2048–2047)	6.10µV (0.24µT)	1
1	1	1	±4.0mT	0xF800–0x07FF (-2048–2047)	8.54µV (0.34µT)	1

Table 12: Gain Settings

The table below shows nominal delay times settings. These values may have up to ±50% variation due to PVT.

DL3	DL2	DL1	DL0	Delay Time (ms)
0	0	0	0	0.000 (default)
0	0	0	1	0.333
0	0	1	0	0.667
0	0	1	1	1.000
0	1	0	0	1.333
0	1	0	1	1.667
0	1	1	0	2.000
0	1	1	1	2.333
1	0	0	0	2.667
1	0	0	1	3.000
1	0	1	0	3.333
1	0	1	1	3.667
1	1	0	0	4.000
1	1	0	1	4.333
1	1	1	0	4.667
1	1	1	1	5.000

Table 13: Delay Time

Mode Register

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to select the operating mode of the device. MR0 through MR7 indicate bit locations, with *MR* denoting the bits that are in the mode register. MR7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
(0)	(0)	(0)	(0)	(0)	(0)	MD1 (1)	MD0 (0)

Table 14: Mode Register

Location	Name	Description
MR7 to MR2	0	These bits must be cleared for correct operation.
MR1 to MR0	MD1 to MD0	Mode Select Bits. These bits select the operation mode of this device.

Table 15: Mode Register Bit Designations

MD1	MD0	Mode
0	0	Continuous-Conversion Mode. In continuous-conversion mode, the device continuously performs conversions an places the result in the data register. RDY goes high when new data is placed in all three registers. After a power-on or a write to the mode or configuration register, the first measurement set is available from all three data output registers after a period of $2/f_{DO}$ and subsequent measurements are available at a frequency of f_{DO}, where f_{DO} is the frequency of data output.
0	1	Single-Conversion Mode. When single-conversion mode is selected, device performs a single measurement, sets RDY high and returned to sleep mode. Mode register returns to sleep mode bit values. The measurement remains in the data output register and RDY remains high until the data output register is read or another conversion is performed.
1	0	Idle Mode. Device is placed in idle mode.
1	1	Sleep Mode. Device is placed in sleep mode.

Table 16: Operating Modes

Data Output X Registers A and B

The data output X registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel X. Data output X register A contains the MSB from the measurement result, and data output X register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DXRA0 through DXRA7 and DXRB0 through DXRB7 indicate bit locations, with *DXRA* and *DXRB* denoting the bits that are in the data output X registers. DXRA7 and DXRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DXRA7	**DXRA6**	**DXRA5**	**DXRA4**	**DXRA3**	**DXRA2**	**DXRA1**	**DXRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DXRB7	**DXRB6**	**DXRB5**	**DXRB4**	**DXRB3**	**DXRB2**	**DXRB1**	**DXRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 17: Data Output X Registers A and B

Data Output Y Registers A and B

The data output Y registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Y. Data output Y register A contains the MSB from the measurement result, and data output Y register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DYRA0 through DYRA7 and DYRB0 through DYRB7 indicate bit locations, with *DYRA* and *DYRB* denoting the bits that are in the data output Y registers. DYRA7 and DYRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DYRA7	**DYRA6**	**DYRA5**	**DYRA4**	**DYRA3**	**DYRA2**	**DYRA1**	**DYRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DYRB7	**DYRB6**	**DYRB5**	**DYRB4**	**DYRB3**	**DYRB2**	**DYRB1**	**DYRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 18: Data Output Y Registers A and B

Data Output Z Registers A and B

The data output Z registers are two 8-bit registers, data output register A and data output register B. These registers store the measurement result from channel Z. Data output Z register A contains the MSB from the measurement result, and data output Z register B contains the LSB from the measurement result. The value stored in these two registers is a 16-bit value in 2's complement form, whose range is 0xF800 to 0x07FF. DZRA0 through DZRA7 and DZRB0 through DZRB7 indicate bit locations, with *DZRA* and *DZRB* denoting the bits that are in the data output Z registers. DZRA7 and DZRB7 denote the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

In the event the ADC reading overflows or underflows for the given channel, or if there is a math overflow during the bias measurement, this data register will contain the value -4096 in 2's complement form. This register value will clear when after the next valid measurement is made.

DZRA7	**DZRA6**	**DZRA5**	**DZRA4**	**DZRA3**	**DZRA2**	**DZRA1**	**DZRA0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
DZRB7	**DZRB6**	**DZRB5**	**DZRB4**	**DZRB3**	**DZRB2**	**DZRB1**	**DZRB0**
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 19: Data Output Z Registers A and B

Data Output Register Operation

When one or more of the output registers are read, new data cannot be placed in any of the output data registers until all six data output registers are read. This requirement also impacts DRDY and RDY, which cannot be cleared until new data is placed in all the output registers.

Status Register

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with *SR* denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
(0)	(0)	(0)	(0)	(0)	REN (0)	LOCK (0)	RDY(0)

Table 20: Status Register

Location	Name	Description
SR7 to SR3	0	These bits must be cleared for correct operation.
SR2	REN	Regulator Enabled Bit. This bit is set when the internal voltage regulator is enabled. This bit is cleared when the internal regulator is disabled.
SR1	LOCK	Data output register lock. This bit is set when this some but not all for of the six data output registers have been read. When this bit is set, the six data output registers are locked and any new data will not be placed in these register until on of four conditions are met: one, all six have been read or the mode changed, two, a POR is issued, three, the mode is changed, or four, the measurement is changed.
SR0	RDY	Ready Bit. Set when data is written to all six data registers. Cleared when device initiates a write to the data output registers, when in off mode, and after one or more of the data output registers are written to. When RDY bit is clear it shall remain cleared for a minimum of 5 µs. DRDY pin can be used as an alternative to the status register for monitoring the device for conversion data.

Table 21: Status Register Bit Designations

Identification Register A

The identification register A is used to identify the device. IRA0 through IRA7 indicate bit locations, with *IRA* denoting the bits that are in the identification register A. IRA7 denotes the first bit of the data stream. The number in parenthesis indicates the default value of that bit.

The identification value for this device is stored in this register. This is a read-only register.
Register values. ASCII value *H*

IRA7	IRA6	IRA5	IRA4	IRA3	IRA2	IRA1	IRA0
0	1	0	0	1	0	0	0

Table 22: Identification Register A Default Values

Identification Register B

The identification register B is used to identify the device. IRB0 through IRB7 indicate bit locations, with *IRB* denoting the bits that are in the identification register A. IRB7 denotes the first bit of the data stream.

Register values. ASCII value *4*

IRB7	IRB6	IRB5	IRB4	IRB3	IRB2	IRB1	IRB0
0	0	1	1	0	1	0	0

Table 23: Identification Register B Default Values

Identification Register C

The identification register C is used to identify the device. IRC0 through IRC7 indicate bit locations, with *IRC* denoting the bits that are in the identification register A. IRC7 denotes the first bit of the data stream.

Register values. ASCII value *3*

IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
0	0	1	1	0	0	1	1

Table 24: Identification Register C Default Values

I^{2}C COMMUNICATION PROTOCOL

The HMC5843 communicates via a two-wire I2C bus system as a slave device. The HMC5843 uses a simple protocol with the interface protocol defined by the I2C bus specification, and by this document. The data rate is at the standard-mode 100kbps or 400kbps rates as defined in the I2C Bus Specifications. The bus bit format is an 8-bit Data/Address send and a 1-bit acknowledge bit. The format of the data bytes (payload) shall be case sensitive ASCII characters or binary data to the HMC5843 slave, and binary data returned. Negative binary values will be in two's complement form. The default (factory) HMC5843 7-bit slave address is 0x3C for write operations, or 0x3D for read operations.

The HMC5843 Serial Clock (SCL) and Serial Data (SDA) lines have optional internal pull-up resistors, but require resistive pull-ups (Rp) between the master device (usually a host microprocessor) and the HMC5843. Pull-up resistance values of about 10k ohms are recommended with a nominal 1.8-volt digital supply voltage (DVDD). Other values may be used as defined in the I2C Bus Specifications or with the internal 50k ohm pull-up resistors (SDAP, SCLP) that can be tied to DVDD.

The SCL and SDA lines in this bus specification can be connected to a host of devices. The bus can be a single master to multiple slaves, or it can be a multiple master configuration. All data transfers are initiated by the master device which is responsible for generating the clock signal, and the data transfers are 8 bit long. All devices are addressed by I2C's unique 7 bit address. After each 8-bit transfer, the master device generates a 9 th clock pulse, and releases the SDA line. The receiving device (addressed slave) will pull the SDA line low to acknowledge (ACK) the successful transfer or leave the SDA high to negative acknowledge (NACK).

Per the I2C spec, all transitions in the SDA line must occur when SCL is low. This requirement leads to two unique conditions on the bus associated with the SDA transitions when SCL is high. Master device pulling the SDA line low while the SCL line is high indicates the Start (S) condition, and the Stop (P) condition is when the SDA line is pulled high while the SCL line is high. The I2C protocol also allows for the Restart condition in which the master device issues a second start condition without issuing a stop.

All bus transactions begin with the master device issuing the start sequence followed by the slave address byte. The address byte contains the slave address; the upper 7 bits (bits7-1), and the Least Significant bit (LSb). The LSb of the address byte designates if the operation is a read (LSb=1) or a write (LSb=0). At the 9 th clock pulse, the recieving slave device will issue the ACK (or NACK). Following these bus events, the master will send data bytes for a write operation, or the slave will clock out data with a read operation. All bus transactions are terminated with the master issuing a stop sequence.

I2C bus control can be implemented with either hardware logic or in software. Typical hardware designs will release the SDA and SCL lines as appropriate to allow the slave device to manipulate these lines. In a software implementation, care must be taken to perform these tasks in code.

OPERATIONAL EXAMPLES

The HMC5843 has a fairly quick stabilization time from no voltage to stable and ready for data retrieval. The nominal 5 milli-seconds with the factory default single measurement mode means that the six Bytes of magnetic data registers (DXRA, DXRB, DYRA, DYRB, DZRA, and DZRB) are filled with a valid first measurement.

To change the measurement mode to continuous measurement mode, after the 5 milli-second power-up time send the three bytes:

0x3C 0x02 0x00

This writes the 00 into the second register or mode register to switch from single to continuous measurement mode setting. With the data rate at the factory default of 10Hz updates (100 milli-seconds interval), a 100 milli-second delay should be made by the I2C master before querying the HMC5843 data registers for new measurements. To clock out the new data, send:

0x3D, and clock out DXRA, DXRB, DYRA, DYRB, DZRA, DZRB located in registers 3 through 8. The HMC5843 will automatically re-point back to register 3 for the next 0x3D query, expected 100 milli-seconds or later.

EXTERNAL CAPACITORS

The two external capacitors should be ceramic type construction with low ESR characteristics. Reservoir capacitor C1 is nominally 4.7 micro-farads in capacitance, with the set/reset capacitor C2 nominally 0.22 micro-farads in capacitance. Low ESR characteristics may not be in many smallest size SMT ceramic capacitors (0402), so be prepared to up-size the capacitors to gain Low ESR characteristics.

ORDERING INFORMATION

Ordering Number	Product
HMC5843	3-Axis Digital Compass IC
HMC5843-TR	Tape and Reel 2.5k pieces/reel

Caution
This part is sensitive to damage by electrostatic discharge. Use ESD precautionary procedures when touching, removing or inserting.

CAUTION: ESDS CAT. 1B

FIND OUT MORE

For more information on Honeywell's Magnetic Sensors visit us online at www.honeywell.com/magneticsensors or contact us at 800-323-8295 (763-954-2474 internationally).

The application circuits herein constitute typical usage and interface of Honeywell product. Honeywell does not warranty or assume liability of customer-designed circuits derived from this description or depiction.

Honeywell reserves the right to make changes to improve reliability, function or design. Honeywell does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others.

U.S. Patents 4,441,072, 4,533,872, 4,569,742, 4,681,812, 4,847,584 and 6,529,114 apply to the technology described

Honeywell
12001 Highway 55
Plymouth, MN 55441
Tel: 800-323-8295
www.honeywell.com/magneticsensors

Honeywell

Form #900367
September 2008