TDK Multilayer Ceramic Chip Capacitors

Application Manual

1 Features of TDK multilayer ceramic chip capacitors

The electrical characteristics of multi-layer ceramic chip capacitors are essentially the same as disk-type capacitors since the same ceramic dielectric principles apply. However, to provide large capacitance, the laminated ceramic-chip capacitor can be made with a ceramic dielectric that is much thinner, at 2.5 to 30 micrometers, than the standard disk type capacitor (0.1mm or larger). As a result, the MLC Class II/III, differ in voltage related characteristics, such as DC bias effects, when compared to single layer types.

The laminated ceramic-chip capacitor also has a structure that makes it vastly different from the disk type capacitor in several key areas.

1) Laminate structures of numerous thin layers provide high capacitance in small packages.
2) The structure is completely monolithic which affords superior mechanical strength and high reliability.
3) Precisely-controlled dimensions are critical for accurate, high-speed automated placement.
4) Constructed of ceramic material and metal, MLC chip capacitors are extremely stable, and do not deteriorate, even under extreme environmental conditions.
5) Lack of device polarity and lateral symmetry simplify handling, placement, and inspection.
6) Stray capacitance is kept at a minimum achieving output close to the theoretical model.
7) Surface mount (leadless) components have very low parasitic inductance providing excellent frequency characteristics.

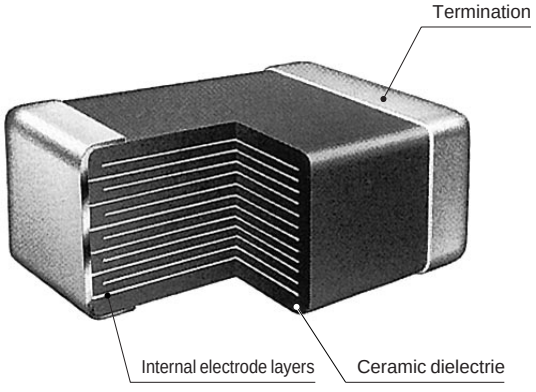
Even with the aforementioned advantages, it is important to recognize the limitations of any ceramic component. MLC chip capacitors mounted directly onto printed circuit boards are subjected to many mechanical and thermal stresses. These adverse conditions may damage the product and alter its characteristics.

Therefore, well-maintained process controls for mounting and soldering surface mount components is necessary. A full understanding of these proper application methods will lead to more reliable products.

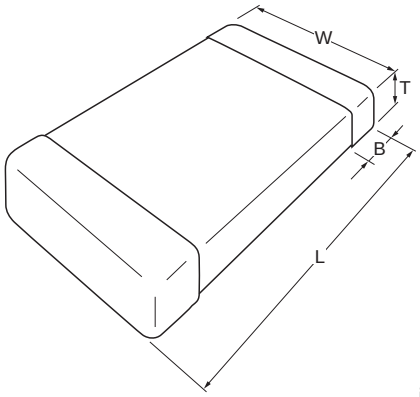
2. Dimensions and construction

2-1 Dimensions and construction

Model of the structure of a laminated ceramic chip capacitor



Dimensions of TDK multilayer ceramic chip capacitors



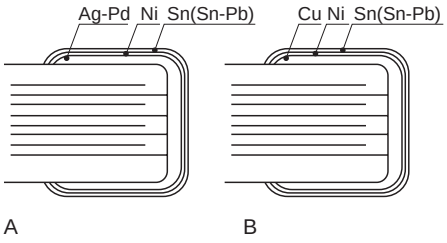
in millimeters

Type	L	W	T	B
C1005	1.0±0.05	0.5±0.05	0.55max.	0.1min.
C1608	1.6±0.1	0.8±0.1	0.9max.	0.2min.
C2012	2.0±0.2	1.25±0.2	1.45max.	0.2min.
C3216	3.2±0.2	1.6±0.2	1.9max.	0.2min.
C3225	3.2±0.4	2.5±0.3	2.8max.	0.2min.
C4532	4.5±0.4	3.2±0.4	3.6max.	0.2min.
C5750	5.7±0.4	5.0±0.4	5max.	0.2min.

For more details, see the product catalog.

2-2 Termination composition

Two kinds of terminations are available. One is composed of Ag-Pd, with electroplated nickel barrier layer with a tin (or tin-lead) layer as the solderable finish (see Fig. A). The other is a copper base with electroplated layers of nickel and tin (or tin-lead) (Fig. B).



A: Ag-Pd-based system (Pd internal electrode)
B: Cu-based system (BME technology)

To prevent the phenomenon of termination leaching, a solder barrier layer of nickel is electroplated on the termination with layer of tin (or tin-lead) that has excellent solderability characteristics. The table below shows the soldering techniques to be used with each type.

Soldering technique by chip shape

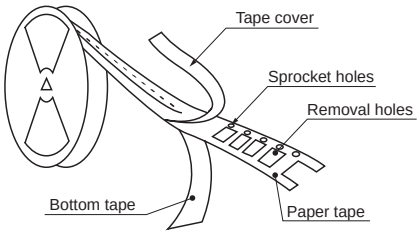
Type	Reflow	Flow	Soldering iron
C1005	○	×	○
C1608	○	○	○
C2012	○	○	○
C3216	○	○	○
C3225	○	×	○
C4532	○	×	○
C5750	○	×	○

○: applicable ×: non-applicable

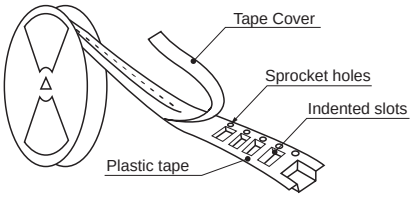
Reel packaging

Taping material

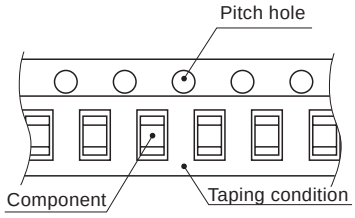
Paper carrier



Embossed tape

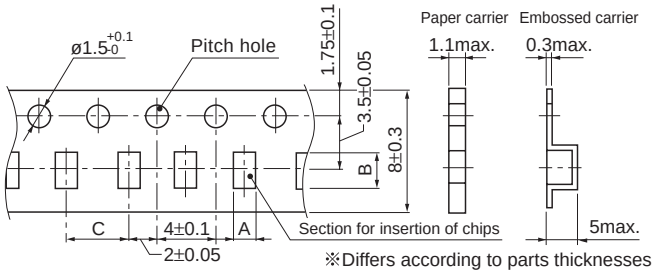


Tape-loading status



Tape dimensions

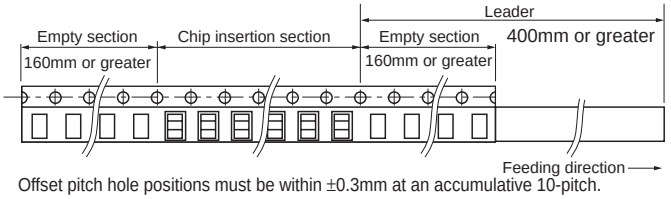
Tape form and dimensions



※Differs according to parts thicknesses

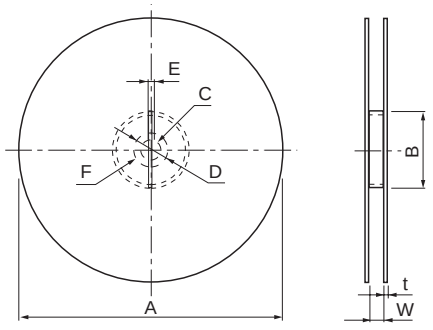
(in millimeters)

Type	A	B	C
C1005	$0.62^{+0.05}_{-0.10}$	$1.15^{+0.05}_{-0.10}$	2±0.05
C1608	1.1±0.2	1.9±0.2	4±0.1
C2012	1.5±0.2	2.3±0.2	4±0.1
C3216	1.9±0.2	3.5±0.2	4±0.1
C3225	2.9±0.2	3.6±0.2	4±0.1
C4532	3.6±0.2	4.9±0.2	8±0.1
C5750	5.4±0.2	6.1±0.2	8±0.1



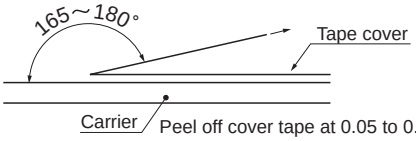
Offset pitch hole positions must be within ±0.3mm at an accumulative 10-pitch.

Reel shape and dimensions



A:ø178±2.0
B:ø60±2.0
C:ø13±0.5
D:ø21±0.8
E:2±0.5
F:R1
W:9±0.3 (3225 and smaller)
W:13±0.3 (4532 and 5750)
t:2±0.5

in millimeters



Peel off cover tape at 0.05 to 0.7N in the direction of the arrow.

Storage
TDK multilayer ceramic chip capacitors will not lose their electrical characteristics in ambient conditions. However, solderability and taping properties may change during extended storage. Therefore, the following precautionary measures are recommended.

Storage environment
The packaging of chip capacitors is designed to have a long shelf life, but in order to minimize the aging of the packaging materials, storage conditions should be at less than 40°C and under 70% relative humidity. Use TDK multilayer ceramic chip capacitors within six months of receiving.

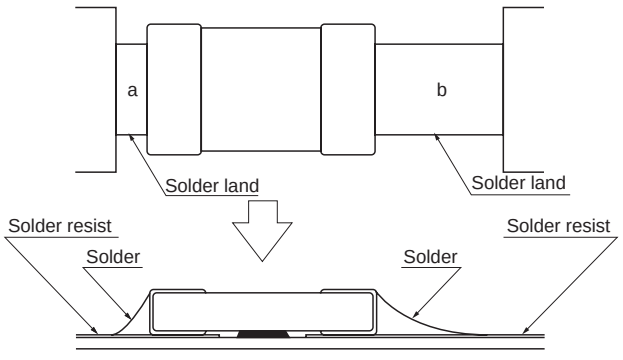
Atmosphere
Chlorine gas or sulfuric acid in the air may adversely affect the solderability of the termination, therefore, avoid exposure to this environment.

Rapid temperature changes.
When removing TDK multilayer ceramic chip capacitors from their storage place,l make sure that they are not subjected to any differences in temperature that would cause moisture condensation.

Surface mount technology
Solder pad design
The solder filet volume will directly affect the strength of the chip capacitor.

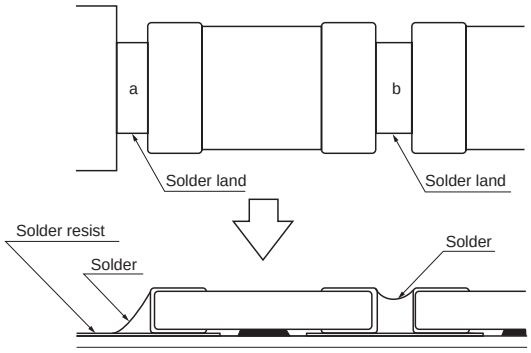
1) The larger the amount of solder used on TDK multilayer ceramic chip capacitors, the greater the stress on the capacitors which results in a weakened condition. Solder land dimensions shall be designed to ensure that appropriate solder amounts are used.
2) Avoid using common solder land for multiple terminations and provide individual solder land for each termination.

Foot print size and solder amount
Component span



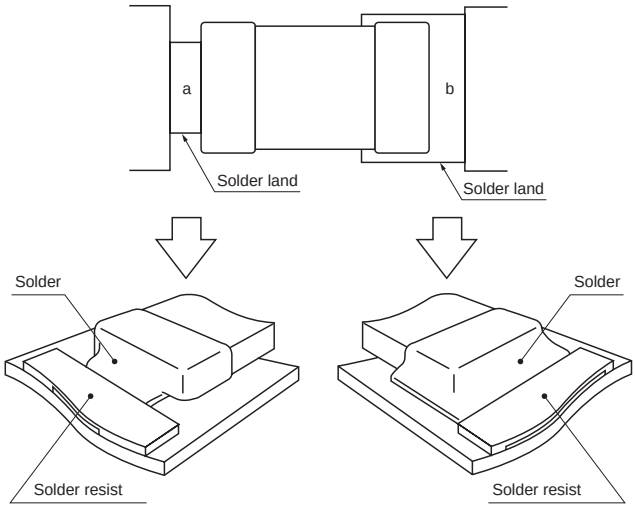
a : Solder quantity is appropriate
b : Solder resist is too far away from the chip termination allowing too much soldering space.

Distance between adjacent terminations



a : Solder quantity is appropriate
b : Chip capacitor is too close the adjacent chip capacitor

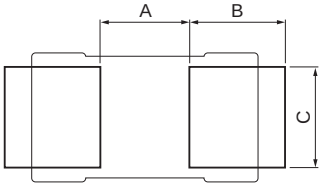
Land width



a : Solder quantity is appropriate
b : Excessive solder when lands are too wide.

Example of recommend land shape and dimensions
1) Land dimensions
Since there are differences between the appropriate solder volume, depending on the soldering method selected, we recommend the land shape and dimensions shown below.

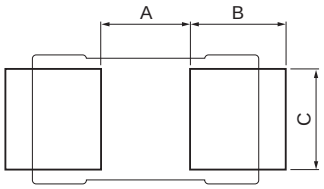
Recommend land pattern for reflow use



(in millimeters)

Type	A	B	C
C1005	0.3 to 0.5	0.35 to 0.45	0.4 to 0.6
C1608	0.6 to 0.8	0.6 to 0.8	0.6 to 0.8
C2012	0.9 to 1.2	0.7 to 0.9	0.9 to 1.2
C3216	2 to 2.4	1 to 1.2	1.1 to 1.6
C3225	2 to 2.4	1 to 1.2	1.9 to 2.5
C4532	3.1 to 3.7	1.2 to 1.4	2.4 to 3.2
C5750	4.1 to 4.8	1.2 to 1.4	4.0 to 5.0

Land pattern recommended for flow use



(in millimeters)

Type	A	B	C
C1608	0.7 to 1	0.8 to 1	0.6 to 0.8
C2012	1 to 1.3	1 to 1.2	0.8 to 1.1
C3216	2.1 to 2.5	1.1 to 1.3	1 to 1.3

2) Why land dimensions differ in reflow and flow uses (points to observe)
Dimension A: Reason that reflow < flow
In flow use, component is held temporarily in place by a glue dot, so the sizes are a little bit larger in flow than in reflow to prevent the adhesive from flowing out onto the lands.
Dimension B: Reason that reflow < flow
In flow use the B dimensions are made larger to prevent defects from lack of solder during spray soldering.
Dimension C: Reason that reflow > flow
The C dimension is reduced in flow use to cut down on the amount of solder buildup and to minimize direct flex stress on the circuit board.

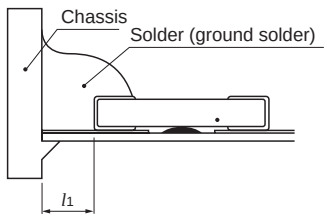
3) Land dimensions of micro-chips (type 1005 and 1608)
Extremely small MLC chip capacitors increase the rate of generation of the tombstone effect in reflow soldering. To prevent the tombstone effect, reduce land dimensions to decrease the amount of solder buildup.

Placement on the circuit board

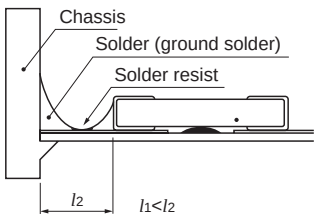
1) Example of placement to be avoided and layout recommendations (processing of land divisions)

Example 1: Soldering to chassis

Locations to be avoided

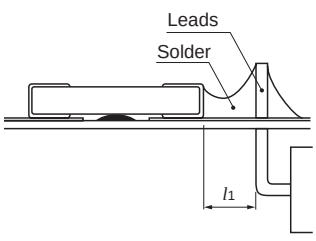


Example of improvement

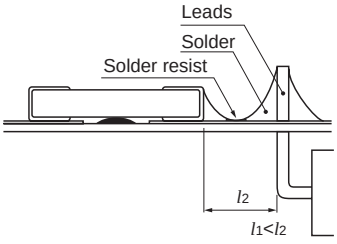


Example 2: Use of common solder land with PTH components

Locations to be avoided

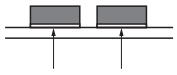


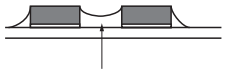
Example of improvement



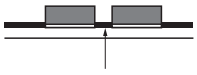
Example 3: Common land use with other SMD

Locations to be avoided





Example of improvement



2) Important points in designing land patterns
Solder buildup will be in excess if more than one TDK MLC chip capacitor is placed on the same land or a capacitor shares a land with some other part. Caution must be used when more than one MLC chip capacitor shares the same land because that narrows the space between chips, makes it easier for some sections not to get soldered, and may require repairs with a soldering iron.
The above diagram of an example of improvement shows that using solder resist processing to provide a land for each chip improves the level of soldering reliability.

Adhesive

Otherwise, there is a danger of deterioration in chip characteristics. Check these elements in the prototype stage, before mass production, and if there are any questions as to details, please contact TDK.

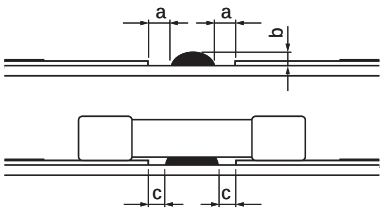
Methods of use and basic conditions required of adhesives

Please consider the following requirement when selecting adhesives.
1) High adherent strength so the components will not drop off or skew during mounting or while handling.
2) Adhesive strength must not deteriorate when subjected to the high heat of soldering.
3) Long shelf life
4) Rapid curing
5) Non-corrosive
6) Non-conductive
7) Non-toxic

Printing/dispensing

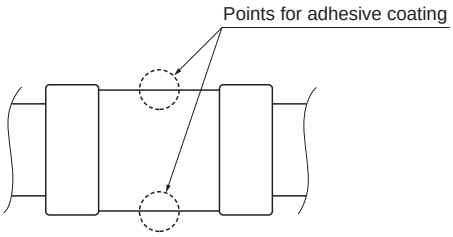
(1) When TDK MLC chip capacitors are glued to a circuit board with adhesive, all elements such as land pattern dimensions, type of adhesive, quantity of adhesive coating, curing temperature and curing time must be compatible. Applying too much adhesive coating presents the danger of the coating flowing into the land patterns and causing soldering to be defective. As a guide for optimum application, see the next page, which shows the amount and shape of coating for C2012 and C3216 types. Adequately investigate the amount and shape of coating for other types before using them.

Recommended conditions for adhesives quantities
(example of C2012 and C3216)



a:0.2mm min. b:70～100μm c:No contact with pattern

2) We recommend the following coating patterns when using adhesives that combine UV and heat curing.



To promote effective UV curing, coat at 2points that are away from the center of mounting position and hold the chip in position with adheisive from the sides.

Curing of adhesive

To prevent the terminal electrodes oxidizing, keep the curing conditions at within 2 minutes and less than 160°C.
Caution: Certain types of adhesives may reduce in insulation resistance. The differences in coefficients of thermal expansion (CTE) between the adhesives and the TDK multilayer ceramic chip capacitors may cause the chip to develop cracks. Use caution when applying adhesives because either too much or too little can cause problems.

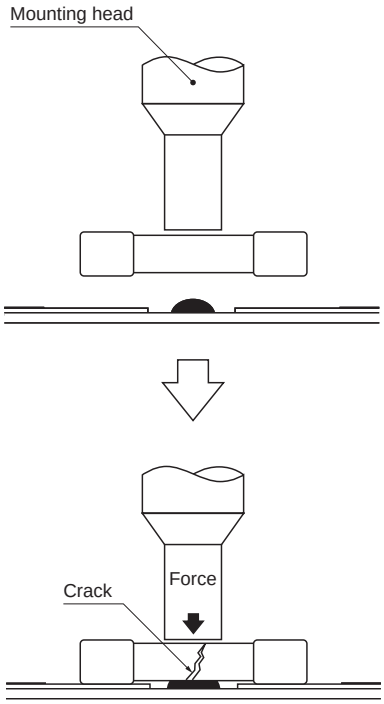
Mounting

When installing TDK multilayer ceramic chip capacitors on circuit boards make sure that excessive force is not applied to the capacitors. Make sure that the periodic maintenance of installer equipment is performed regularly.

Pressure on installation head

1) The stronger the pressure on the installation head, the more stable the installation, but if a pressure greater than necessary is applied, the TDK multilayer ceramic chip capacitors may crack.
2) If the drop point of the suction nozzle is too low, excessive forces will be applied to the chip during installation and that may cause breaks. Realign the circuit board slide and adjust the bottom dead center over the circuit board.

Mounting



Mounting head pressure

The amount of mounting pressure applied to a TDK MLC chip capacitor will differ according to the shape of the mounting nozzle. If the tip diameter is 1.8mm, the usual amount of mounting force is 3000 to 8000 erg. If the head is smaller and the same amount of mounting force is applied, an increase in shock energy per square millimeter of (eg/mm^2) will be such that caution must be used when handling extremely small chips like the C1005 and C1608 types.

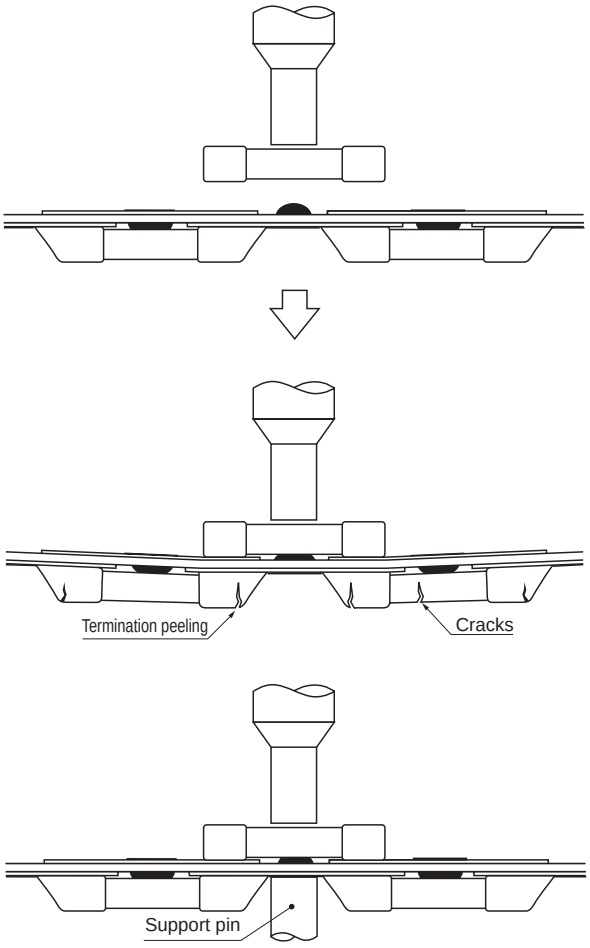
Maintenance and inspection of installers

When the centering jaw is worn, excessive localized shock may be loaded on the TDK MLC chip capacitor during positioning and cracking may occur. To prevent problems like this from occurring, carefully monitor the centering jaw and ensure that periodic maintenance and inspection is performed.

Torsion stress on printed circuit boards during double sided mounting

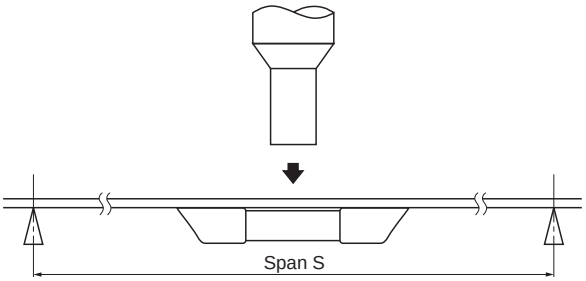
1) After soldering both surfaces of the dual-sided circuit board and then performing installation, on one of the surfaces, if pressure from the installation head causes the circuit board to bend, this will apply a large amount of mechanical stress to the TDK multilayer ceramic chip capacitors that have been already soldered on the opposite side. To prevent this, we recommend the installation of support pins for the back surface of the circuit board. (see the model diagram on the next page.)

Model of cracks generated on a dual-surface mounted board



2) Even if the shock energy is the same, the smaller the span of the circuit board (S in diagram below) the greater the shock applied to the TDK MLC chip capacitor and the higher the rate of crack occurrence. Therefore, when installing support pins, set their positions so that there will be as little shock energy as possible.

Magnitude of stress and location of support pins



Vibrating parts feeder

If the parts feeder is subjected to vibrations for long periods of time, the TDK multilayer ceramic chip capacitors may have their terminal electrodes warn because of contact friction with the interior walls of the parts feeder. This may lead to a degradation in solderability. Moreover, termination material may adhere to the surface of the component, resulting in a degradation of insulation resistance.
Controlled quantities of chip capacitors should be used in the feeder at one time.

Requirements for selecting flux

Recommended flux
The more active the flux, the better the soldering finish, but the materials that are added for cleanliness and making flux more active may reduce the insulation performance of TDK multilayer ceramic chip capacitors. To prevent this from happening, we recommend rosin flux with low activity (containing 0.2% or less chlorine).

Flux types

1) It is recommended that mildly-activated rosin flux used. There are flat and lustrous types.
2) Water soluble flux: These are made from activators and organic compounds that dissolve in water, and that have superior soldering properties in comparison with rosin fluxes.

Flux control

1) coating quantity
   Amount of flux coated differs according to the specific gravity of the flux. Make adequate checks prior to use.
2) Periodic replacement
   The moisture absorption and oxidation properties of flux result in the degradation of solder characteristics. TDK recommends replacement of all solder after it has been in use for two to four weeks.

Cautions in using flux

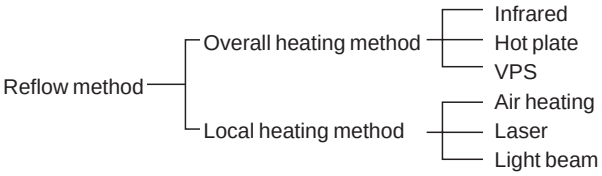
Flux is one of the more important elements affecting the performance of TDK multilayer ceramic chip capacitors. Before selecting and using flux, check the items shown below for the best flux.
1) Use flux that has a chlorine content of 0.1wt% or less. Do not use strong flux. Use of flux with large amounts of chlorine compounds added for activation or strong oxide flux will lead to large amounts of dross after soldering, which may invite a lowering of chip surface insulation and corrosion of terminal electrodes.
2) When soldering, keep the amount of flux coating minimized. Coat with flux when flow soldering to improve soldering characteristics but if large amounts of flux are used at this time it will result in the occurrence of flux gas which presents the danger of impeding soldering properties. We recommend the use of the foam method for limiting the amount of flux coating.
3) When using water soluble flux, clean thoroughly. The dross from water soluble flux has the property of melting when exposed to moisture, so in high humidity conditions, insulation resistance will be lowered by dross that adheres to the chip surface and that will have adverse effects on reliability. Therefore, when using water soluble flux, make sure that the capabilities of the cleaning method and cleaning equipment are well-maintained.

Soldering

Because the TDK multilayer ceramic chip capacitors will be in direct contact with molten solder during soldering, there will be stresses caused by the rapid rise in heat, and there will also be the danger of such things as flux residue and the dissolution of terminal electrode materials. Therefore, the most important point for the soldering process when installing on the circuit board is that attention be given to the following items when assigning conditions.

Reflow soldering

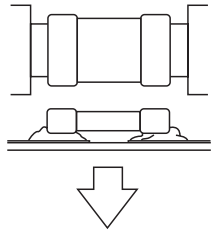
The reflow soldering method places the components on dispensed solder amounts on the printed circuit board. The chips are then attached by using heat to melt the solder. The method of heating for melting the solder may be the overall heating method or the local heating method.



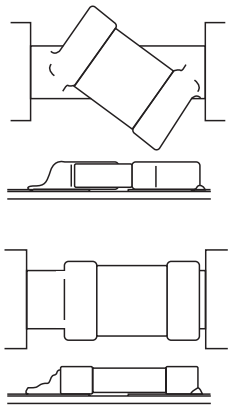
With this method, adhesives usually are used to temporarily hold the TDK MLC chip capacitors in place. This prevents skewing and tombstoning effects. Also if there is a rapid temperature curve in heat treatment, there is a danger of thermal cracks appearing in all of the chips, so we recommend the soldering conditions shown below (temperature profile).

Skewing

Before soldering



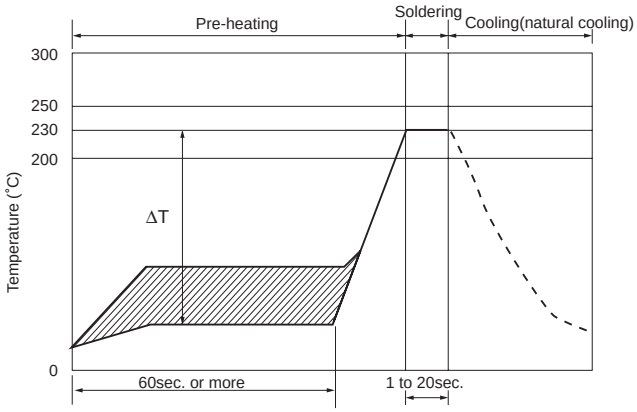
After soldering



Recommended soldering profile for reflow method

If there is a rapid increase in heat on the molten solder temperature, tombstoning effects may be more common. If there is a rapid temperature change during the soldering operation, thermal cracks may be more common.

Generally recommended temperature conditions for reflow soldering



Soldering method	Change in temperature(˚C)
C3216 and under	ΔT≦190
C3225 and over	ΔT≦130

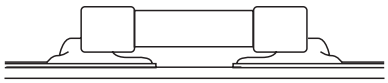
Important points in selecting cream solder

1) Compatible with consistent printing or dispensing volume on PC pad dimensions.
2) The solder surface area must not spread more than necessary in the reflow preheating process after printing or dispensing.
3) Adequate solderability.
4) The flux residue must be minimized and solder balls must be eliminated.
5) Flux residue must not adversely affect the circuit or other electronic parts.
6) Must have an adhesion that allows parts mounting in stable state with high reliability and no change in contact resistance.

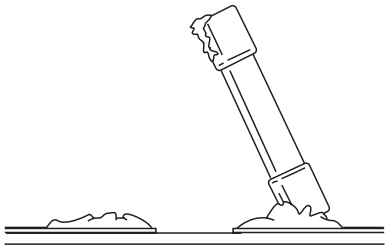
The tombstone effect (Tombstone effect)

TDK multilayer ceramic chip capacitors are small and lightweight, and the tombstone effect, the standing up of capacitors that occurs during reflow soldering, must be addressed. This effect can be reduced by employing such measures as reducing land dimensions, applying adequate preheat, optimizing solder volume, ensuring accurate placement, and providing equal heating to both terminations during soldering.

The tombstone effect (drawbridge effect)
Before soldering



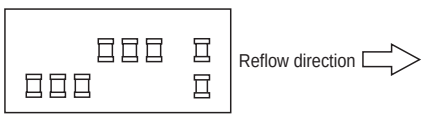
After soldering



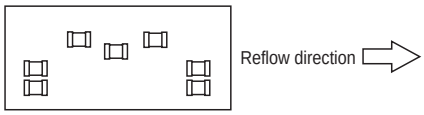
Recommended steps to prevent the tombstone effect

1) Accurate chip placement: Give consideration to reducing any offset in position with relation to the PC board pattern. The tombstone effect occurs more frequently when the direction of chip position offset is the same as the reflow direction (direction of forward circuit board movement).
2) Orientation of component: Give consideration when designing P.C. board pattern to ensure the direction of chip mounting (lengthwise direction) at right angles to the reflow direction.

Position in which the tombstone effect rate is low
(both terminal electrode temperatures are balanced)



Position in which the occurrence of the tombstone effect is high
(temperature of both terminal electrodes easily gets out of balance).

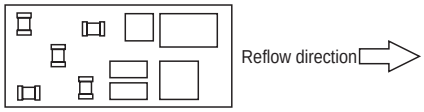


3) Relation between placement and parts with large heat capacity

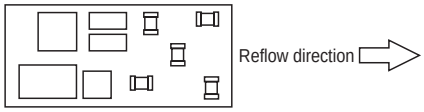
a: Reflow direction and circuit board direction

When installing parts with a large heat capacity on the same circuit board as the TDK multilayer ceramic chip capacitors. Orient the circuit board so that the parts with high heat capacity go into the reflow furnace first and that will help to suppress the rate of the tombstone effect occurrence.

Circuit board direction in which the rate of the tombstone effect occurrence is low (reduced difference in temperature between both terminal electrodes)

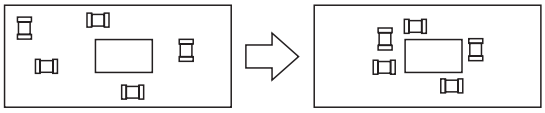


Circuit board direction in which the rate of the tombstone effect occurrence is high (imbalance in temperatures between both terminal electrodes).



b: Distance between parts with large heat capacity

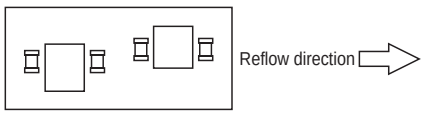
To reduce the rate of tombstone effect occurrence, design the patterns so that the parts with large heat capacity are as close as possible to the TDK multilayer ceramic chip capacitors.



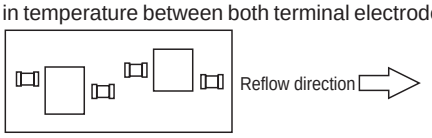
c: Relation in positions between parts with large heat capacity

The occurrence of the tombstone effect can be held down by placing the TDK multilayer ceramic chip capacitors in proximity with the sides of the parts with large heat capacity. At this time, too, place the capacitors as close as possible to the parts with large heat capacity and make sure that the chip orientation is at right angles to the reflow direction.

Position in which the tombstone effect is low (small difference in temperature between both terminal electrodes)



Position in which the tombstone effect is high (imbalance easily occurring in temperature between both terminal electrodes)



4) P.C. pad dimension area

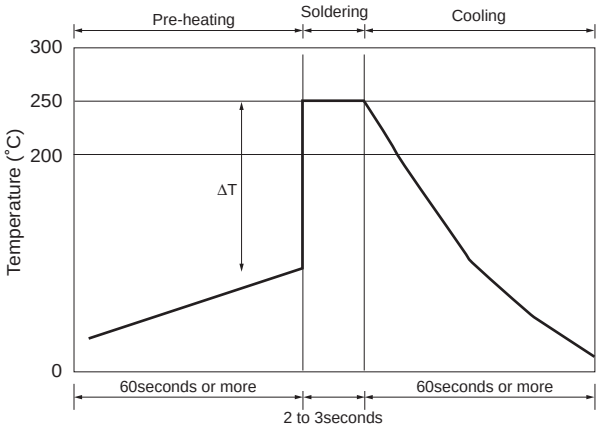
Design the pad dimensions so that the land area is as small as possible and that each land is positioned such that it receives a uniform quantity of solder.

Flow soldering

The flow soldering method involves first temporarily gluing the TDK multilayer ceramic chip capacitors with adhesives in the appropriate positions on the printed circuit board, then coats it with flux and dips it into a preheated molten solder bath.
The TDK multilayer ceramic chip capacitors tested with solder at 230 to 250°C so that adequate measures must be taken to prevent thermal cracks.
Caution: If TDK multilayer ceramic chip capacitors are used that exceed the range of delivery specifications given or specifications in the catalog, cracks may occur within the chips and that presents a danger of reduced reliability. Rapid temperature changes and local heating during soldering are also causes of cracks. Please refer to the soldering methods below for optimum soldering benefits. (temperature profile)

Recommended flow soldering temperature conditions

Recommended temperatures for flow soldering



Soldering method	Change in temperature(°C)
C3216 and under	ΔT≦150

Cautions when setting preheat temperatures

When setting preheat temperatures, we recommend as preheat conditions high temperatures which can pass the following points for test circuit boards

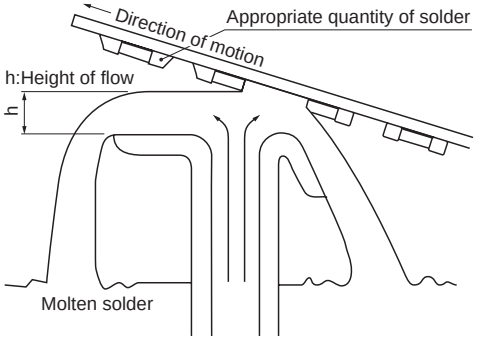
1) Check points when preheat temperature is too low
   a:Flux flows too easily
   b:Possibility of thermal cracks
2) Check points when preheat temperature is too high
   a: Flux deteriorates and reoxidizes even when oxide film is removed. (especially at temperatures of 160°C and above)
   b: Too large a warp in circuit board
   c: Loss of reliability in chips and other parts

Cautions in spray soldering

In the flow method, a pump is constantly spraying molten solder so that if there is a fluctuation in the quantity of solder supplied over unit time, there is a danger of unsoldered locations or bridges occurring. There is a of soldering defects caused by flux gas. To avoid this danger, pay attention to the following points when selecting the spray equipment and setting the spray height .

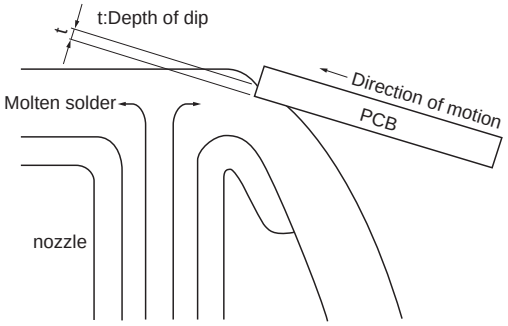
1) Height of spraying in the single wave method (distance from spray nozzle to solder surface)
   a: When the h value in the diagram below increases (that is there is a large flow in unit time and the flow speed is fast), the surface pressure on the circuit board is governed by force in the horizontal direction and the flatness of the solder surface is impaired, and that increases the rate of occurrence of solder defects.
   b: when the h value is low, the surface pressure on the circuit board is governed by force in the vertical direction and the flow of solder is uniformly maintained.
   Recommend value: we recommend an h value of 5mm or less.

Setting spray height h in the single wave method

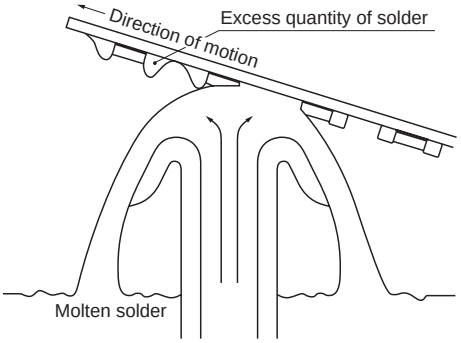


2) Depth of dip in single wave method
   a: If the t value in the diagram below is too large, the rate of occurrence of bridges increases.
   b: If the t value is too low, there rate of occurrence of unsolder sections increases.
   Recommended t value: Recommend an appropriate t value of 0.5 to 1 mm.

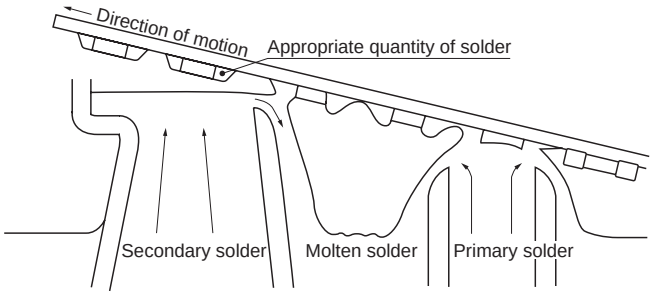
Setting of dip depth t in the single wave method



Examples of conditions to avoid: When dip depth t is too high.



3) Solder dip depth in the double wave method
Setting dip depth t in the double wave method



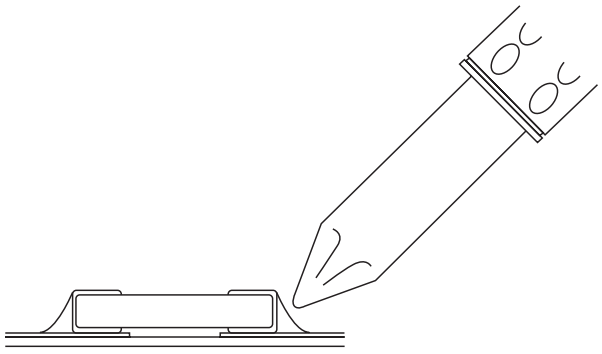
Important points
Primary solder: Greater immersion (prevents non soldered portions)
Second solder: Dip is shallower (draws in excess solder and prevents solder bridges)

Soldering by solder iron

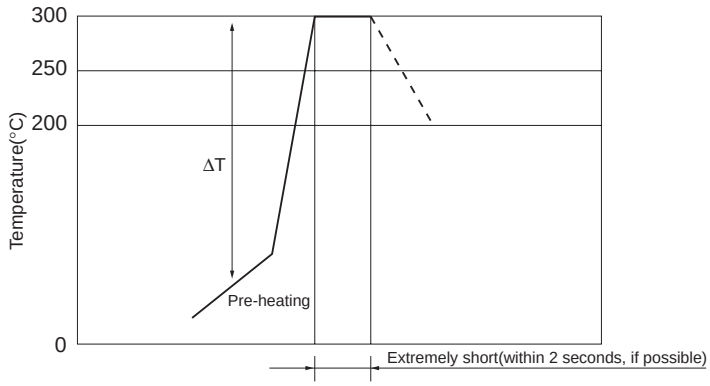
Special attention must be given to the handling and temperature of the soldering iron and the shape of the soldering iron. This is because it is easy for the soldering iron to come into direct contact with the terminal electrodes on the TDK multilayer ceramic chip causing multiple cracking opportunities.
Make sure that the soldering iron does not come into contact with the ceramic dielectric, only the terminations.

How to apply the soldering iron
Recommended conditions for soldering iron

Rated (W)	Soldering iron temperature (°C)	Soldering iron shape (mm)
20max.	300max.	⌀3.0max.



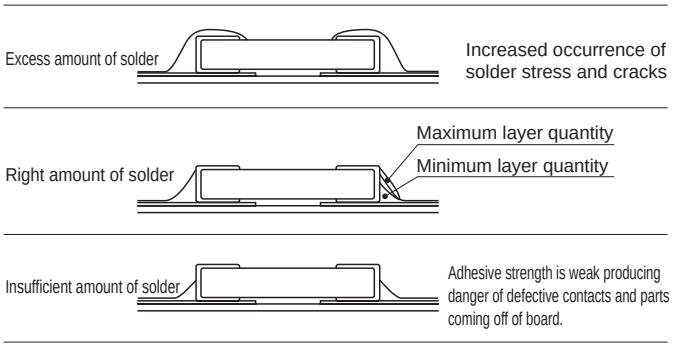
Recommended conditions for soldering iron temperatures



Soldering method	Change in temperature(°C)
C3216 and under	ΔT ≦190
C3225 and over	ΔT ≦130

Solder amount

Too much or too little solder may cause serious consequences for circuit reliability such as cracks from solder stress and parts falling off the circuit board. Check the diagram and make sure to provide the right amount of solder.



Cooling

We recommend natural cooling in the air, but if the parts will be dipped in solvent for cleaning purposes, the temperature difference T should be 100°C or less.

Cleaning

Selection of cleaning fluid

When using rosin flux, cleaning is not usually necessary. When using active flux, the cleaning fluid will separate the chlorine component from the flux and that will have a bad effect on devices. Always use new cleaning fluid for cleaning.

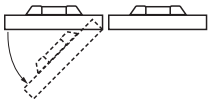
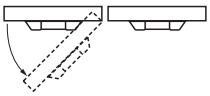
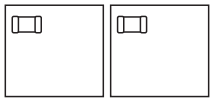
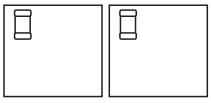
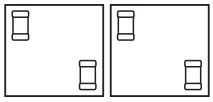
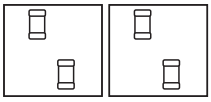
Ultrasonic cleaning

If the ultrasonic energy output is too high during ultrasound cleaning that will affect the adhesion of terminal electrodes so we recommend the following conditions for ultrasound cleaning:
Frequency: 28kHz Output: 20W// cleaning time: 5 min. or less

Cautions in removing from double-sided circuit board

Double-sided circuit boards are singulated into separate unit circuit boards, but if excess flex stress is placed on the circuit boards at that time, cracks may occur in TDK multilayer ceramic chip capacitors. Use the diagram below to ensure that stress suppression during board separation is adequate.

Relationship between chip position and flex stress during board separation

Point	Locations to avoid	Recommended locations
Direction in which chip mounting surface is bent.	 Hold chip mounting surface upward and bend upward	 Holding chip mounting surface downward and bending downward.
Chip orientation	 Set vertically in relationship to slit	 Set horizontally in relationship to slit
Distance from slit	 Installing close to slit	 Installing in center of circuit board units

Cautions when resin coating

After installing the TDK multilayer ceramic chip capacitors on the circuit board, resin may be coated on the device-mounting surface for the purposes of preventing damage from moisture and dust, or when potting, follow the items below in selecting the resin.

1) Take full precautions to ensure that the curing process or the natural drying state is not one in which decomposing gases or reactive gases are present. Being placed in such environments may cause the destruction of the chips because the metals that are part of the TDK MLC chip capacitor structure will react (such as the hydrogen absorption effect of palladium) with the gas.

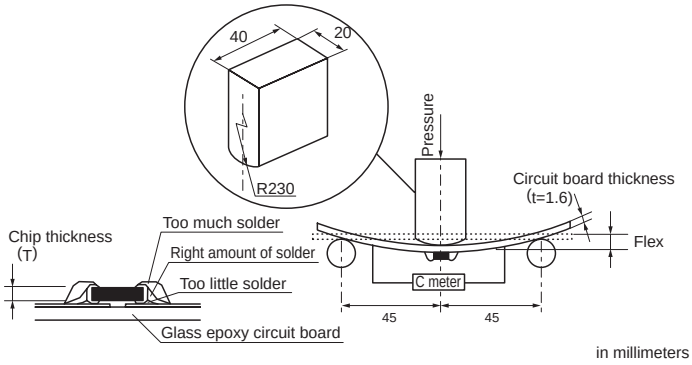
2) The producing of large amounts of stress (this trend is generally pronounced in hard polymer resins) by the thermal expansion and contraction of the resin in the curing process may destroy the TDK multilayer ceramic chip capacitors. Soft polymers should be used as an under coating.

Effects and conditions of other operations

The stress on TDK multilayer ceramic chip capacitors when they are installed will differ according to solder quantity, board material and other conditions, below is shown examples of data for all conditions of stress that occurs to TDK multilayer ceramic chip capacitors. Please use this to improve circuit reliability.

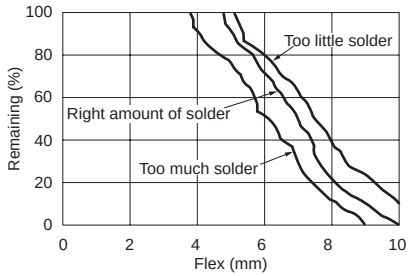
Solder amount and flex strength

Test method

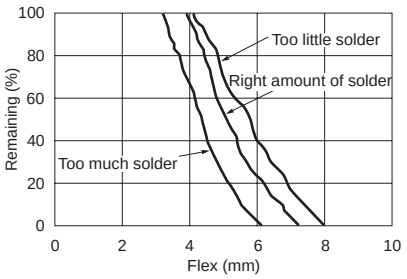


in millimeters

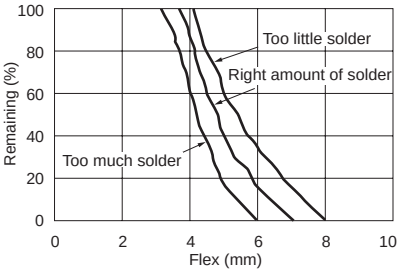
Relation between solder amount and flex strength (C1005X7R1C103K)



Relation between solder amount and flex strength (C1608X7R1C103K)

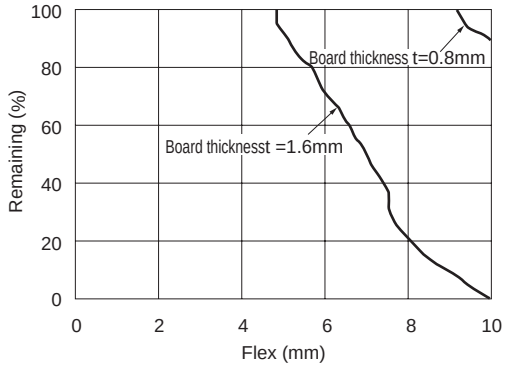


Relation between solder amount and flex strength (C2012X7R1H103K)

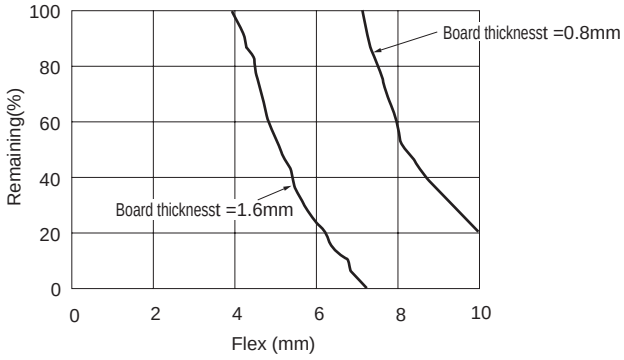


Printed circuit board thickness and flex strength

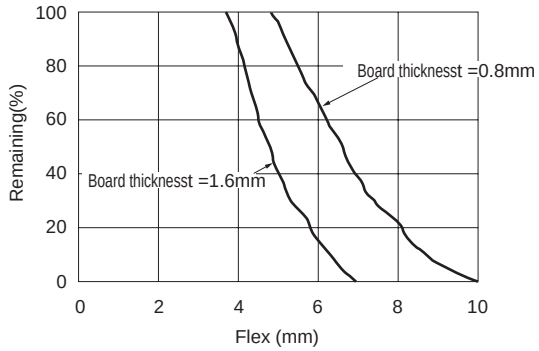
Relation between board thickness and flex strength (C1005X7R1C103K)



Relation between board thickness and flex strength (C1608X7R1C103K)

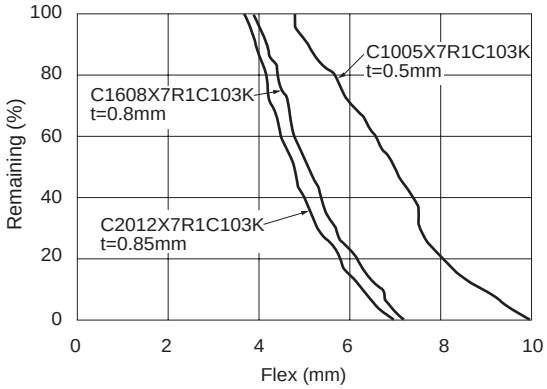


Relation between board thickness and flex strength (C2012X7R1H103K)

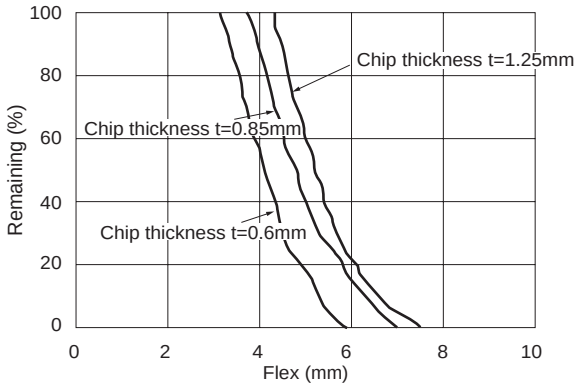


Chip shape and flex strength

Relation between chip shape and flex strength



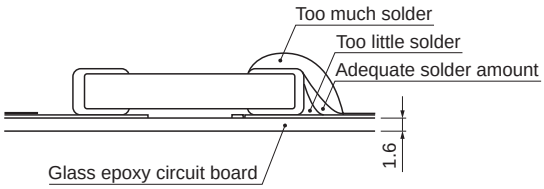
Relation between chip thickness and flex strength (C2012X7R1H103)



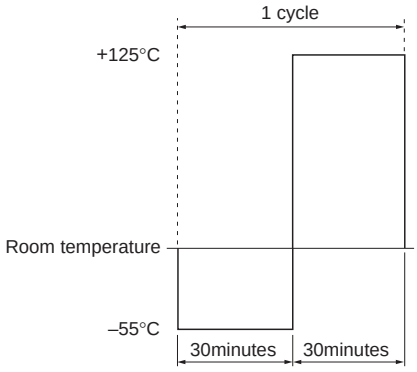
Solder quantity and heat shock

Land dimensions and printed circuit boards used are determined by JIS C6429.

Test conditions (assigning solder amount)



Test conditions (thermal shock)

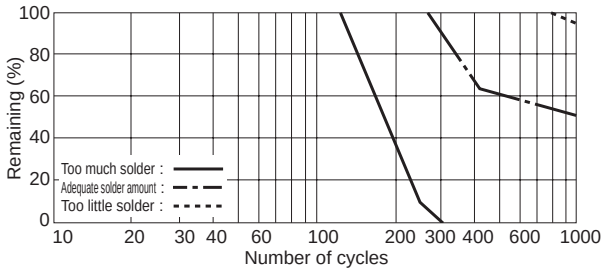


Failure criteria

Determine to be defective if any one of the following condition is not satisfied.

Capacitance change Δ C/C	±7.5%max.
Dielectric dissipation factor tan δ	0.025max.
Insulation resistance IR	10000MΩ min.
External appearance	No damage

Relationship between solder amount and resistance to thermal shock (C2012X7R1H102K)

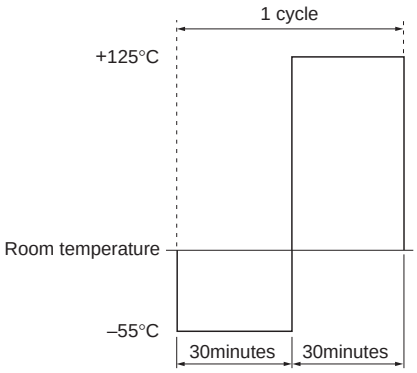


Circuit board material and heat shock

Rate of thermal expansion and circuit board material

Material	Rate of thermal expansion (mm/°C)
Glass epoxy	1.4×10^{-5}
Paper phenol	2.2×10^{-5}
Composite	2.4×10^{-5}
Alumina	6.5×10^{-5}

Test conditions (thermal shock)

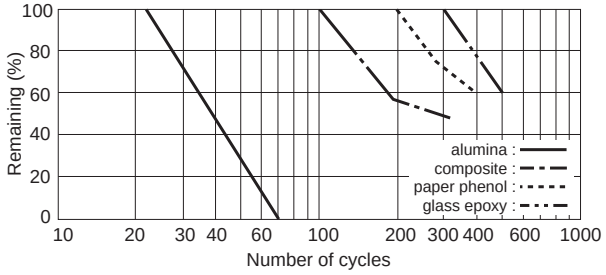


Standards for decision on defects

Determine to be defective if any one of the following condition is not satisfied.

Capacitance change Δ C/C	±7.5%max.
Dielectric dissipation factor tan δ	0.025max.
Insulation resistance IR	10000MΩ min.
External appearance	No damage

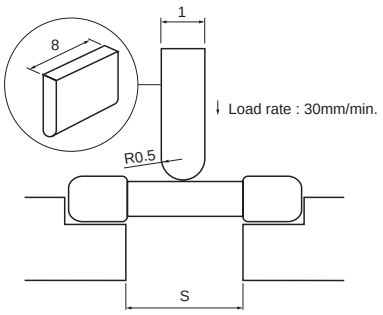
Relationship between circuit board material and thermal shock resistance (C2012X7R1H102K)



Chip break strength

Test method

Conduct tests using tools shown below



S:1.4mm(type 2012)

in millimeters

Chip break strength (Type C2012)