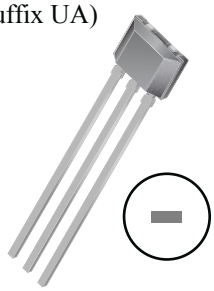
Chopper-Stabilized, Two Wire Hall-Effect Switches

Features and Benefits

- High speed, 4-phase chopper stabilization
- Low switchpoint drift throughout temperature range
- Low sensitivity to thermal and mechanical stresses
- On-chip protection
  - Supply transient protection
  - Reverse battery protection
  - On-board voltage regulator
  - 3.0 to 24 V operation
- Solid-state reliability
- Robust EMC and ESD performance
- Industry leading ISO 7637-2 performance through use of proprietary, 40-V clamping structures

Packages

3-pin ultramini SIP
1.5 mm × 4 mm × 3 mm
(suffix UA)



3-pin SOT23-W
2 mm × 3 mm × 1 mm
(suffix LH)

Approximate scale

Description

The A1152, A1153, A1155, and A1156 comprise a family of two-wire, unipolar, Hall-effect switches, which are factory-trimmed to optimize magnetic switchpoint accuracy. These devices are produced on the Allegro® advanced BiCMOS wafer fabrication process, which implements a patented high frequency, 4-phase, chopper-stabilization technique. This technique achieves magnetic stability over the full operating temperature range, and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh application environments.

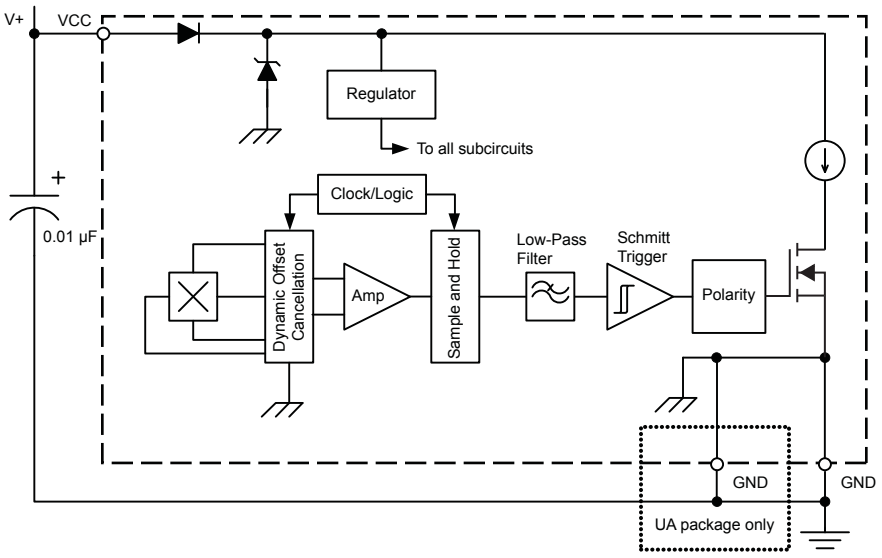
The A115x family has a number of automotive applications. These include sensing seat track position, seat belt buckle presence, hood/trunk latching, and shift selector position.

Two-wire unipolar switches are particularly advantageous in cost-sensitive applications because they require one less wire for operation versus the more traditional open-collector output switches. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition.

Continued on the next page…

Engineering samples available on a limited basis. Contact your local sales or applications support office for additional information.

Functional Block Diagram



Description (continued)

All family members are offered in two package styles. The LH is a SOT-23W style, miniature, low profile package for surface-mount applications. The UA is a 3-pin, ultra-mini, single inline package (SIP) for through-hole mounting. Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

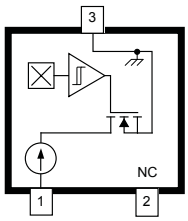
Part Number	Packing[1]	Package	Output (I_{CC}) in South Polarity Field	Supply Current at $I_{CC(L)}$ (mA)	Magnetic Operate Point, B_{OP} (G)
A1152LLHLX-T	13-in. reel, 10 000 pieces/reel	3-pin SOT23W surface mount	Low	5 to 6.9	50 to 110
A1152LUA-T[2]	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1153LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	High		
A1153LUA-T[2]	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1155LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	Low	5 to 6.9	20 to 60
A1155LUA-T[2]	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1156LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	High		
A1156LUA-T[2]	Bulk, 500 pieces/bag	3-pin SIP through hole			

[1]Contact Allegro® for additional packing options.
[2]Contact factory for availability.

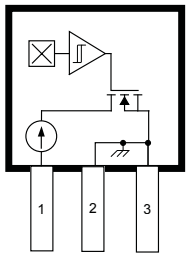
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Magnetic Flux Density	B		Unlimited	G
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagrams



LH Package



UA Package

Terminal List Table

Number	Name		Function
	LH package	UA package	
1	VCC	VCC	Connects power supply to chip
2	NC	GND	LH package: no connection UA package: ground terminal
3	GND	GND	Ground terminal

ELECTRICAL CHARACTERISTICS Valid at T_A = –40°C to 150°C, $T_J < T_J(max)$, C_{BYP} = 0.01 µF, through operating supply voltage range; unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{CC}	Operating, $T_J \leq$ 165 °C		3.0	–	24	V
Supply Current	$I_{CC(L)}$	A1152, A1155	$B > B_{OP}$	5	–	6.9	mA
		A1153, A1156	$B < B_{RP}$				
	$I_{CC(H)}$	A1152, A1155	$B < B_{RP}$	12	–	17	mA
		A1153, A1156	$B > B_{OP}$				
Supply Zener Clamp Voltage	$V_{Z(sup)}$	$I_{CC(L)}(max)$ + 3 mA, T_A = 25°C		28	–	–	V
Supply Zener Clamp Current	$I_{Z(sup)}$	$V_{Z(sup)}$ = 28 V		–	–	$I_{CC(L)}(max)$ + 3 mA	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –18 V		–	–	–1.6	mA
Output Slew Rate[2]	di/dt	No bypass capacitor, capacitance of probe C_S = 20 pF		–	90	–	mA/µs
Chopping Frequency	f_c			–	700	–	kHz
Power-Up Time[3,4]	t_{on}			–	–	25	µs
Power-Up State[3,5,6]	POS	$t_{on} < t_{on}(max)$, V_{CC} slew rate > 25 mV/µs		–	$I_{CC(H)}$	–	–

[1]V_{CC} represents the generated voltage between the VCC pin and the GND pin.
[2]Measured without bypass capacitor between VCC and GND. Use of a bypass capacitor results in slower current change.
[3]Power-Up Time is measured without and with bypass capacitor of 0.01 µF, $B > B_{OP}$ + 10 G. Adding a larger bypass capacitor would cause longer Power-Up Time.
[4]Guaranteed by characterization and design.
[5]Power-Up State as defined is true only with a V_{CC} slew rate of 25 mV/µs or greater.
[6]For $t > t_{on}$ and $B_{RP} < B < B_{OP}$, Power-Up State is not defined.

MAGNETIC CHARACTERISTICS[1] Valid at T_A = –40°C to 150°C, $T_J < T_J$ (max); unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit[2]
Magnetic Operating Point	B_{OP}	A1152, A1153	50	–	110	G
		A1155, A1156	20	–	60	G
Magnetic Release Point	B_{RP}	A1152, A1153	45	–	105	G
		A1155, A1156	10	–	55	G
Hysteresis	B_{HYS}		5	–	30	G

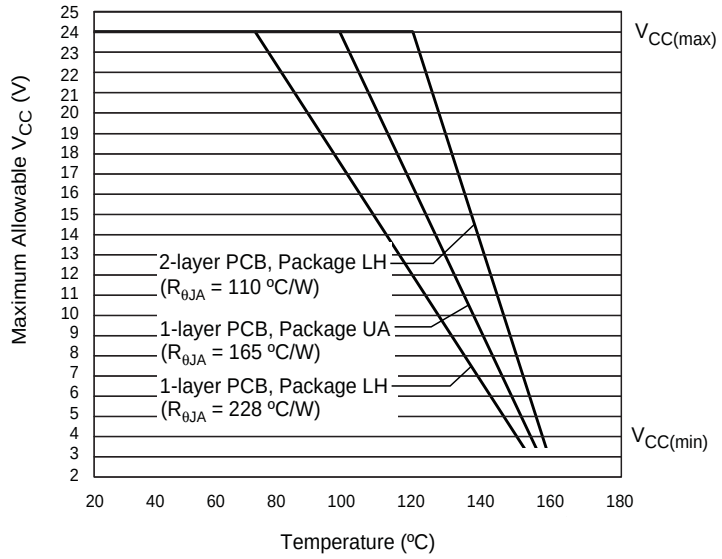
[1]Relative values of B use the algebraic convention, where positive values indicate south magnetic polarity, and negative values indicate north magnetic polarity; therefore greater B values indicate a stronger south polarity field (or a weaker north polarity field, if present).
[2] 1 G (gauss) = 0.1 mT (millitesla).

Thermal Characteristics may require derating at maximum conditions, see application information

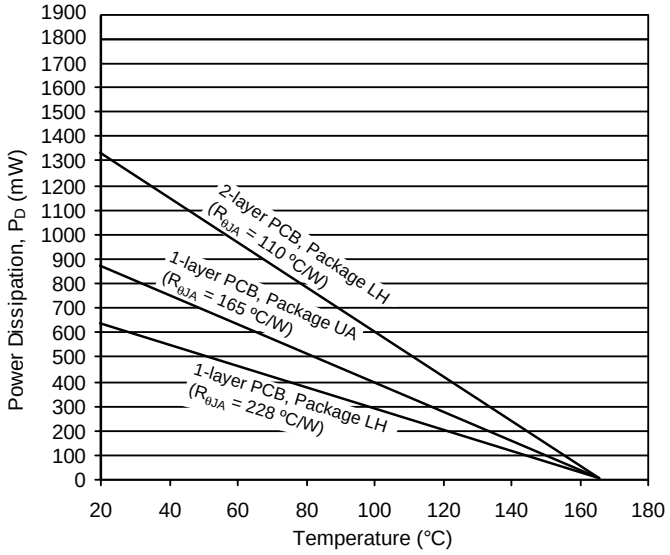
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on 4-layer PCB based on JEDEC standard	228	°C/W
		Package LH, on 2-layer PCB with 0.463 in.^{2} of copper area each side	110	°C/W
		Package UA, on 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on the Allegro website

Power Derating Curve

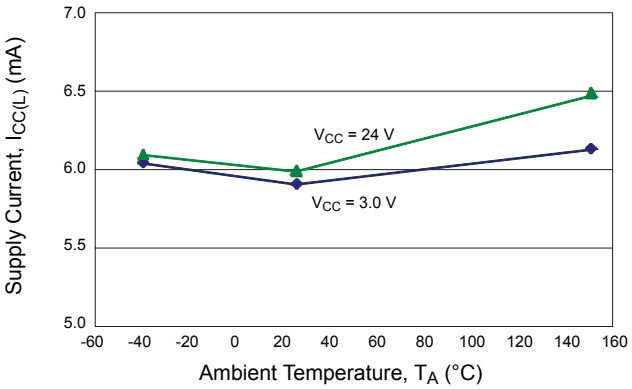


Power Dissipation versus Ambient Temperature

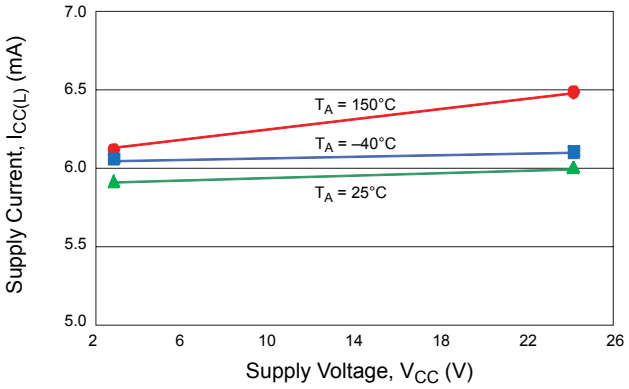


Characteristic Performance

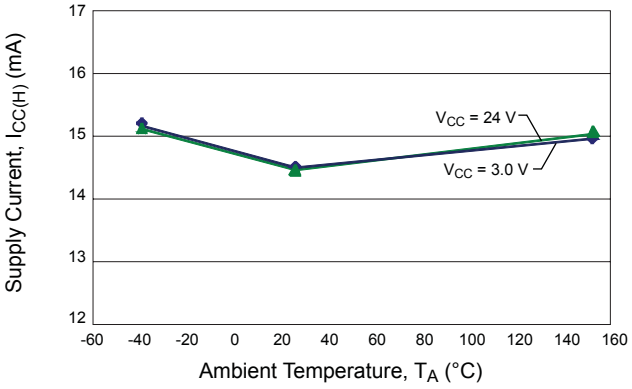
A1152/A1153/A1155/A1156
Average Supply Current (Low) versus Temperature



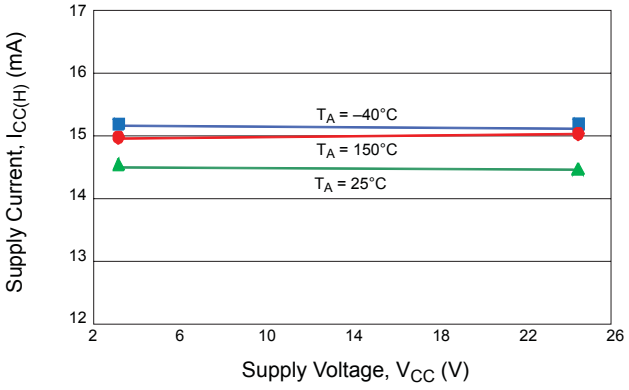
A1152/A1153/A1155/A1156
Average Supply Current (Low) versus Supply Voltage



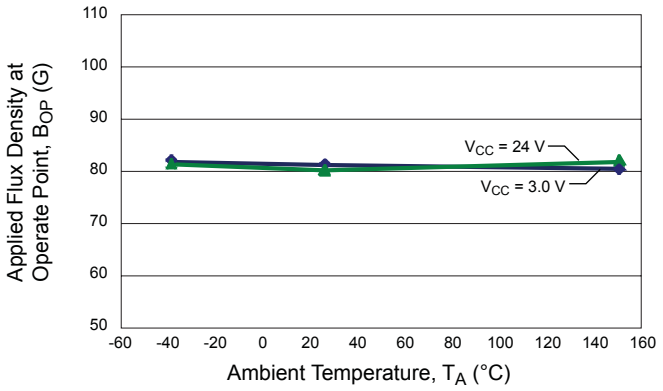
A1152/A1153/A1155/A1156
Average Supply Current (High) versus Temperature



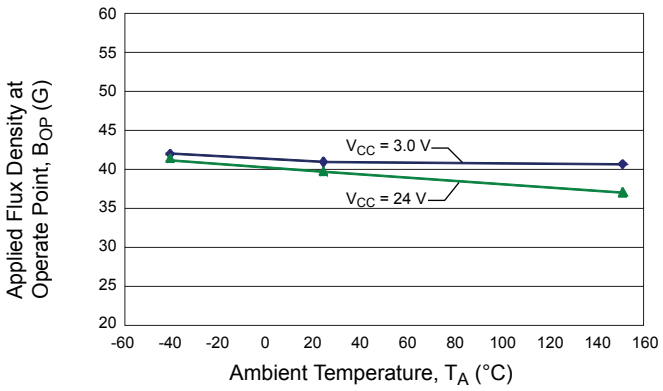
A1152/A1153/A1155/A1156
Average Supply Current (High) versus Supply Voltage



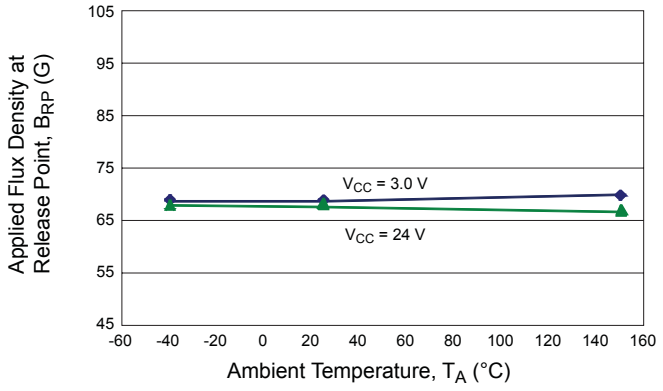
A1152/A1153
Average Operate Point versus Temperature



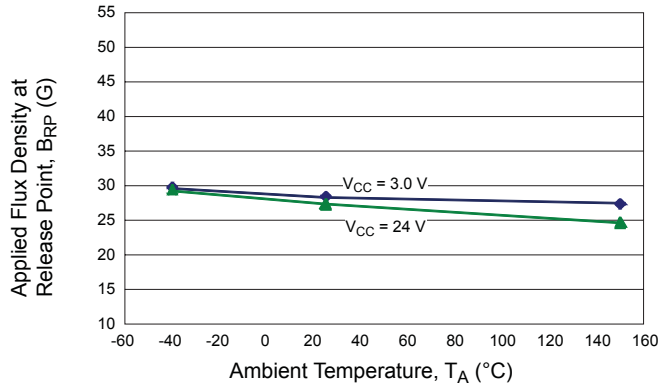
A1155/A1156
Average Operate Point versus Temperature



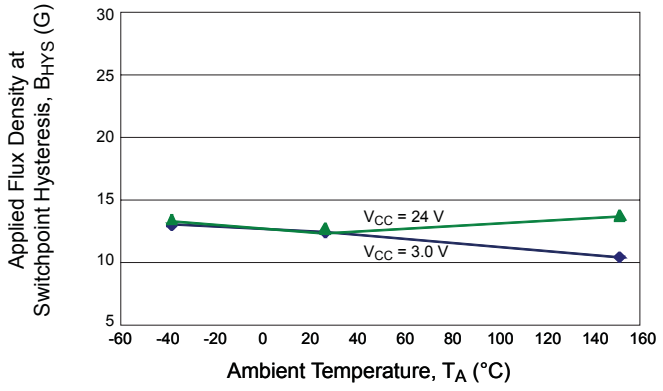
A1152/A1153
Average Release Point versus Temperature



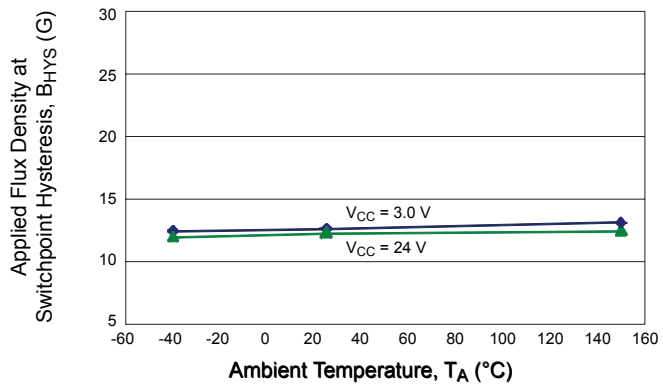
A1155/A1156
Average Release Point versus Temperature



A1152/A1153
Average Switchpoint Hysteresis versus Temperature



A1155/A1156
Average Switchpoint Hysteresis versus Temperature

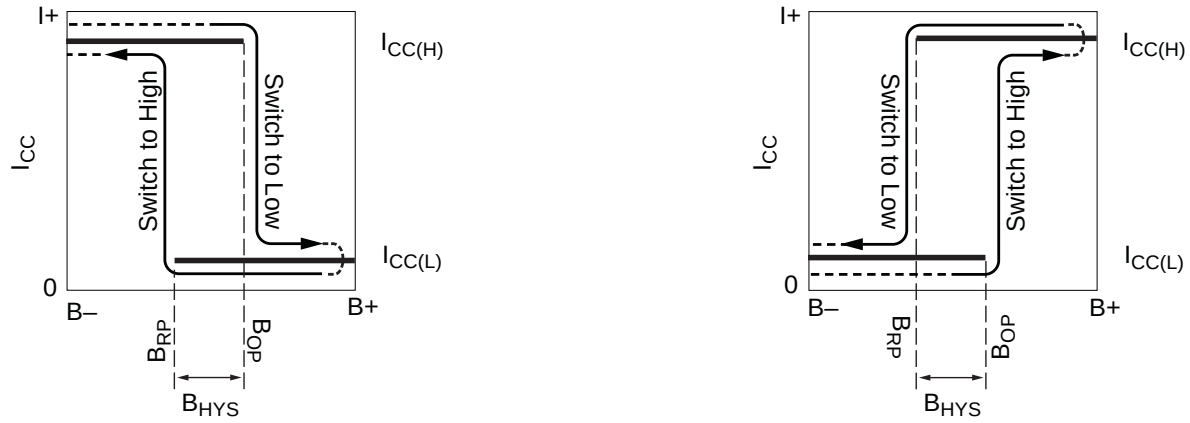


Functional Description

The A1152 and A1155 output, I_{CC}, switches low after the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes high. This is shown in figure 1, panel A.

In the case of the reverse output polarity, as in the A1153 and A1156, the device output switches high after the magnetic field at the Hall sensor IC exceeds the operate point threshold, B_{OP}. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes low (panel B).

The difference between the magnetic operate and release points is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.



(A) Hysteresis curve for A1152, and A1155

(B) Hysteresis curve for A1153 and A1156

Figure 1. Alternative switching behaviors are available in the A115x device family. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

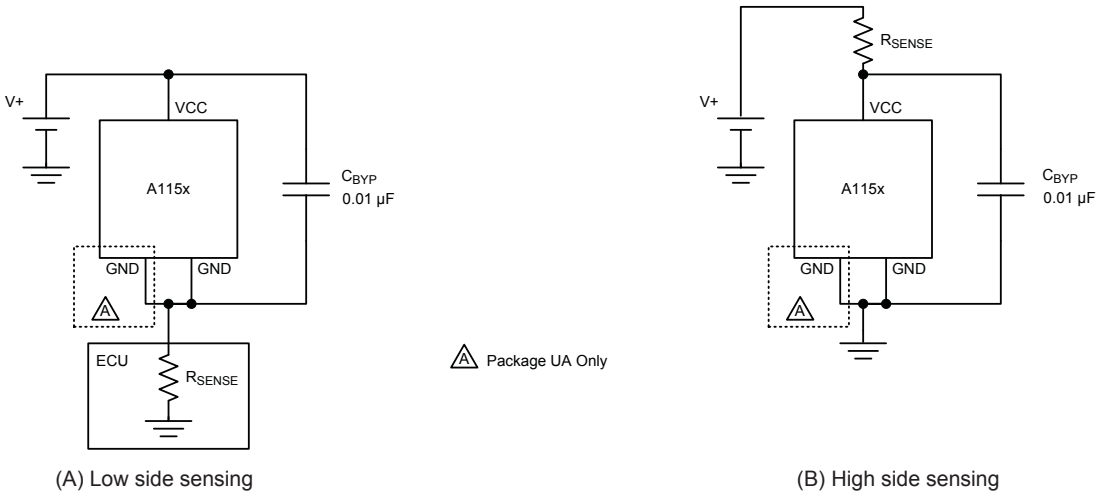


Figure 2. Typical application circuits

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor IC. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 350 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency. This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

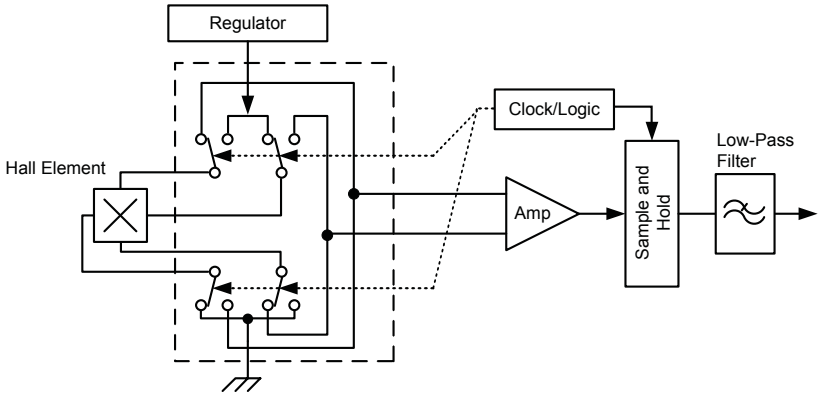


Figure 3. Chopper stabilization circuit (Dynamic Quadrature Offset Cancellation)

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4 mA, and $R_{\theta JA}$ = 140 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4\ mA = 48\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48\ mW \times 140\ °C/W = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UA, using a low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=165 °C/W, T_J(max) = 165°C, V_{CC}(max) = 24 V, and I_{CC}(max) = 17 mA.

Calculate the maximum allowable power level, P_D(max). First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 165\ °C/W = 91\ mW$$

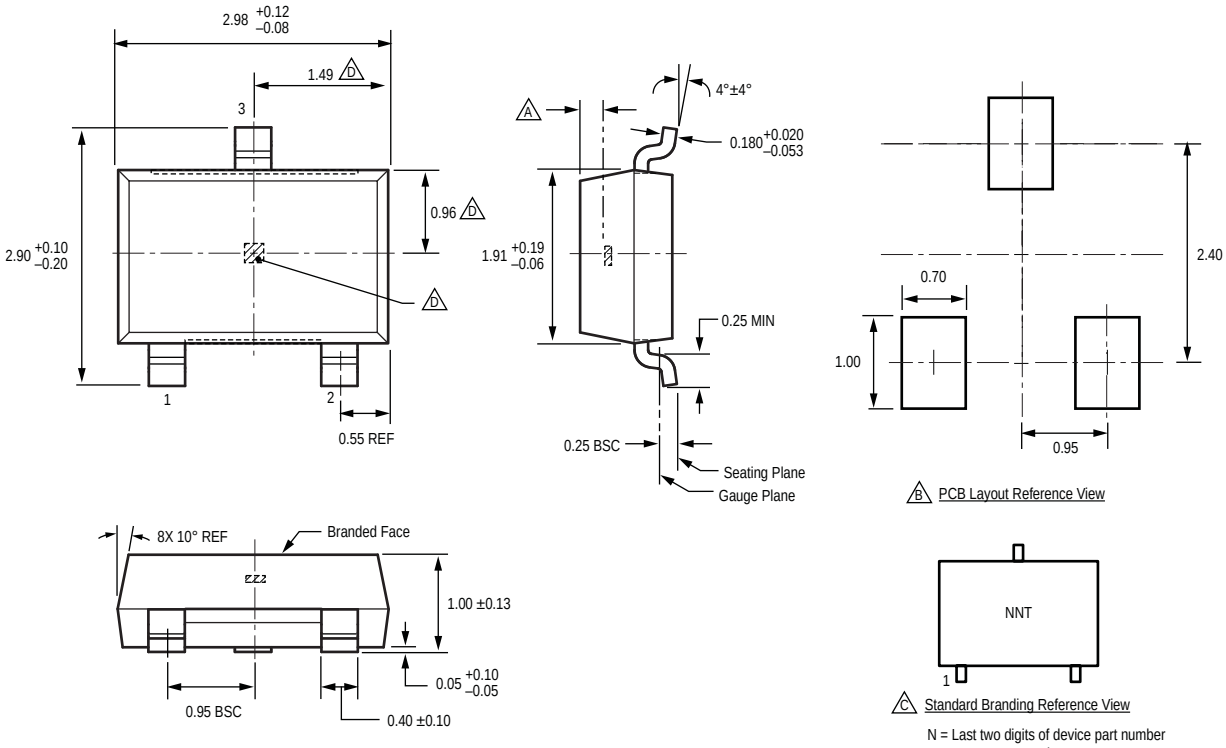
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC}(max) = 91\ mW \div 17\ mA = 5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to V_{CC}(max). If $V_{CC(est)} \leq V_{CC}$(max), then reliable operation between $V_{CC(est)}$ and V_{CC}(max) requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC}$(max), then operation between $V_{CC(est)}$ and V_{CC}(max) is reliable under these conditions.

Package LH, 3-Pin SOT23W



N = Last two digits of device part number
T = Temperature code

For Reference Only; not for tooling use (reference DWG-2840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

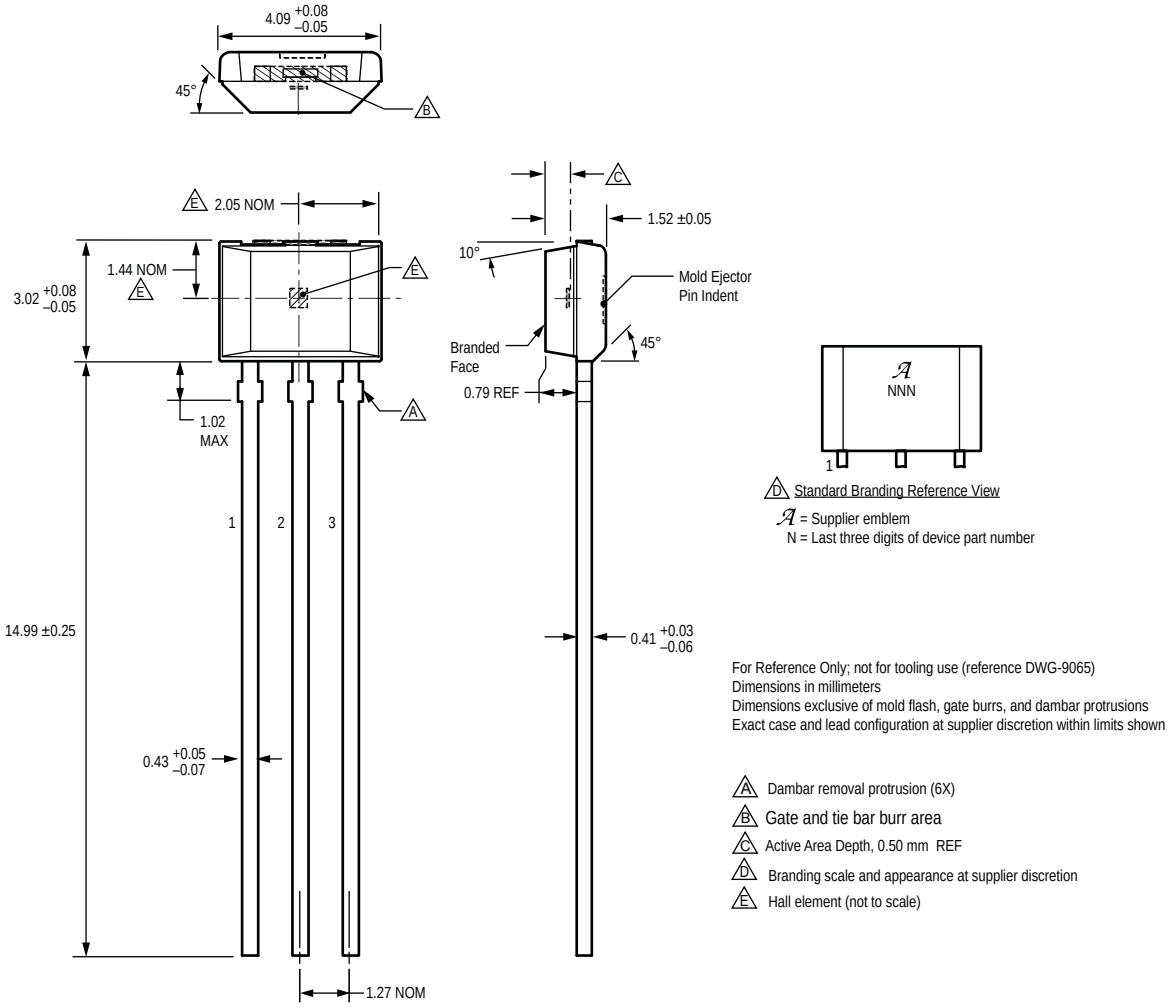
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Package UA, 3-Pin SIP



For Reference Only; not for tooling use (reference DWG-9065)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate and tie bar burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element (not to scale)

For the latest version of this document, visit our website:

www.allegromicro.com