AS5245

Programmable 360° Magnetic Angle Encoder with Absolute SSI and PWM Output

1 General Description

The AS5245 is a contactless magnetic angle encoder for accurate measurement up to 360° and includes two AS5145 devices in a punched stacked leadframe.

It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.0879° = 4096 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal.

An internal voltage regulator allows operation of the AS5245 from 3.3V or 5.0V supplies.

The AS5245 is fully automotive qualified to AEC-Q100, grade 0.
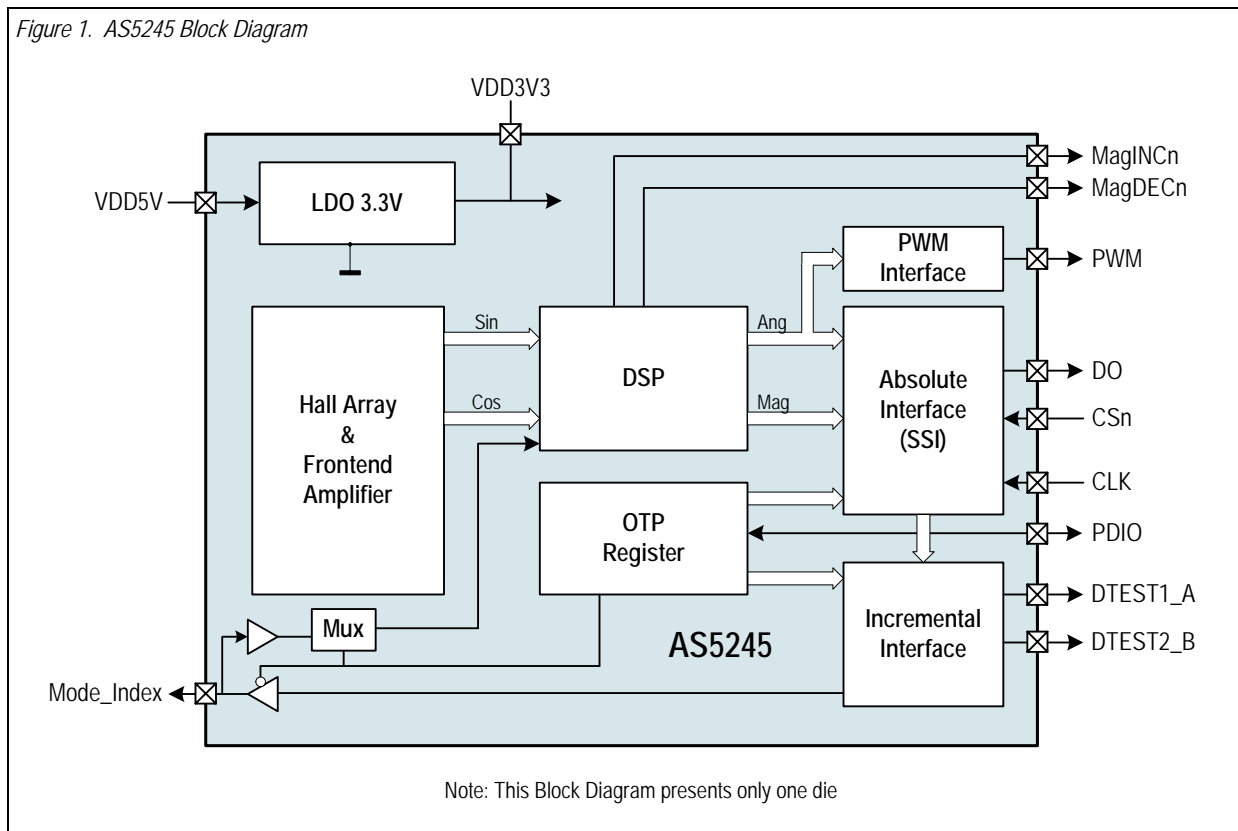
2 Key Features

- Contactless high resolution rotational position encoding over a full turn of 360°

- Two digital 12-bit absolute outputs

- Quadrature A/B (10- or 12-bit) and Index output signal

- User programmable zero position

- Failure detection mode for magnet placement monitoring and loss of power supply

- "Red-Yellow-Green" indicators display placement of magnet in Z-axis

- Tolerant to magnet misalignment and air gap variations

- Wide temperature range: - 40°C to +150°C

- Unique Chip Identifier

- Fully automotive qualified to AEC-Q100, grade 0

- Small package: QFN 32 LD (7x7)

3 Applications

The AS5245 is ideal for applications with an angular travel range from a few degrees up to a full turn of 360°. The device is suitable for Automotive applications like Throttle position sensors, Gas/brake pedal position sensing, Headlight position control, Contactless rotary position sensing, Front panel rotary switches and Replacement of potentiometer.
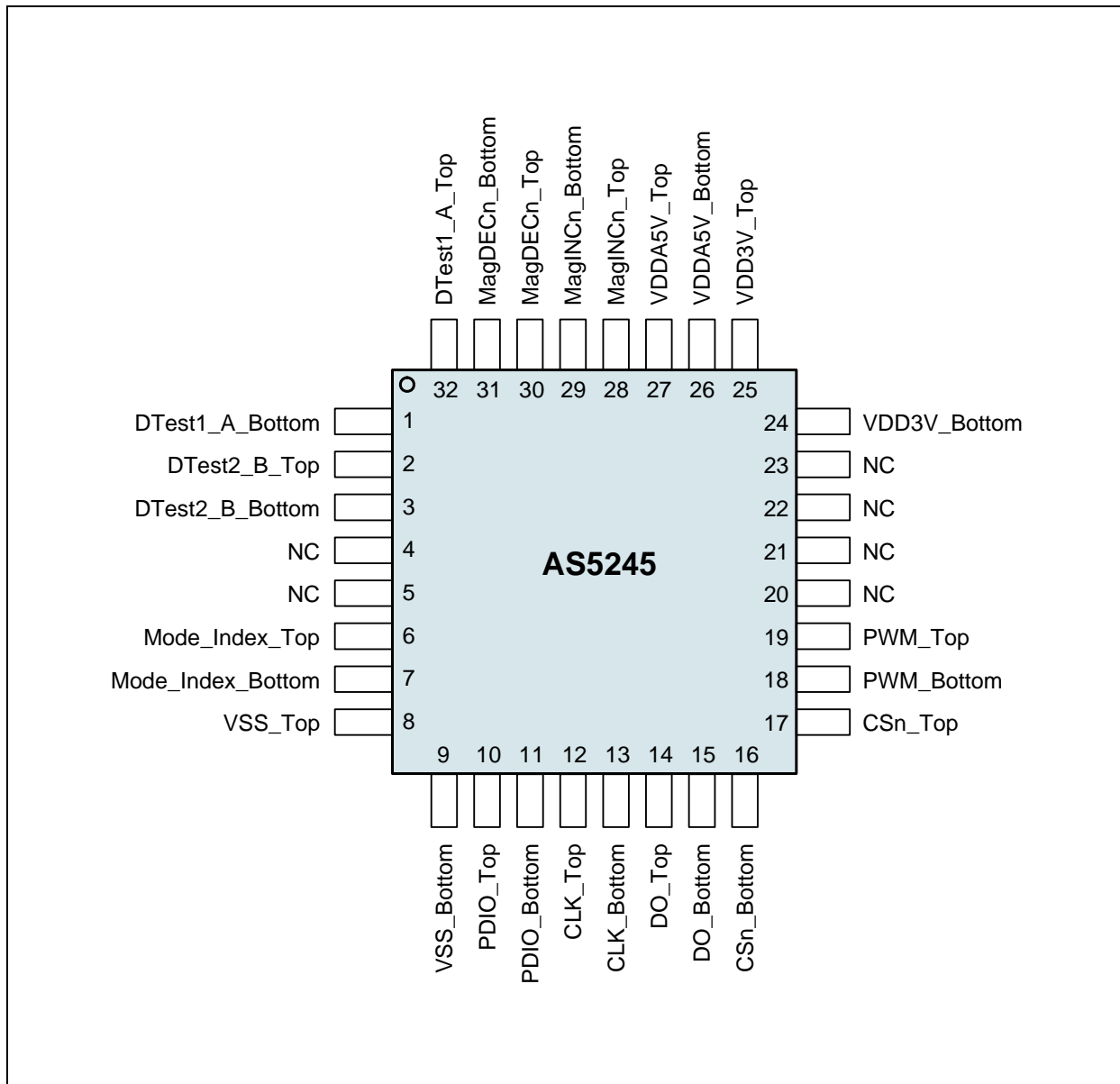

Figure 1. AS5245 Block Diagram

Note: This Block Diagram presents only one die

Contents

4 Pin Assignments

Figure 2. Pin Assignments (Top View)

4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
DTest1_A	1, 32	Digital output	Test output in default mode
DTest2_B	2, 3	Digital output	Test output in default mode
NC	4, 5	-	For internal use. Must be left unconnected
Mode_Index	6, 7	Digital I/O pull-down	Select between slow (open, low: VSS) and fast (high) mode. Internal pull-down resistor. Hard wired connection to VDD or GND recommended.
VSS	8, 9	Supply pin	Negative Supply Voltage (GND)
PDIO	10, 11	Digital input pull-down	**OTP Programming Input and Data Input for Daisy Chain mode.** Internal pull-down resistor (74kΩ). Should be connected to VSS if programming is not used.
CLK	12, 13	Digital input, Schmitt-trigger input	**Clock Input** of Synchronous Serial Interface; Schmitt-Trigger input
DO	14, 15	Digital output / tri-state	**Data Output** of Synchronous Serial Interface
CSn	16, 17	Digital input pull-up, Schmitt-trigger input	**Chip Select.** Active low. Schmitt-Trigger input, internal pull-up resistor (50kΩ)
PWM	18, 19	Digital output	**Pulse Width Modulation**
NC	20, 21	-	For internal use. Must be left unconnected
NC	22, 23	-	For internal use. Must be left unconnected
VDD3V3	24, 25	Supply pin	3V-Regulator Output for internal core, regulated from VDD5V. Connect to VDD5V for 3V supply voltage. Do not load externally.
VDD5V	26, 27	Supply pin	Positive Supply Voltage, 3.0V to 5.5V
MagINCn	28, 29	Digital output open drain	**Magnet Field Magnitude Increase.** Active low. Indicates a distance reduction between the magnet and the device surface.
MagDECn	30, 31	Digital output open drain	**Magnet Field Magnitude Decrease.** Active low. Indicates a distance increase between the device and the magnet.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
DC supply voltage at pin VDD5V	-0.3	7	V	
DC supply voltage at pin VDD3V3	-0.3	5	V	
Input pin voltage	-0.3	7	V	Pins Prog, MagINCn, MagDECn, CLK, CSn
Input current (latchup immunity)	-100	100	mA	Norm: EIA/JESD78 Class II Level A
Electrostatic discharge		±2	kV	Norm: JESD22-A114E
Storage temperature	-55	+150	ºC	
Body temperature (Lead-free package)		260	ºC	t=20 to 40s, Norm: IPC/JEDEC J-Std-020C Lead finish 100% Sn "matte tin"
Humidity non-condensing	5	85	%	
Ambient temperature	-40	150	ºC	

6 Electrical Characteristics

T_{AMB} = -40 to +150ºC, $V_{DD}5V$ = 3.0-3.6V (3V operation) VDD5V = 4.5-5.5V (5V operation) unless otherwise noted.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating Conditions						
T_{AMB}	Ambient temperature		-40		+150	ºC
I_{supp}	Supply current	**(one die only)**		16	21	mA
$V_{DD}5V$	Supply voltage at pin $V_{DD}5V$	5V Operation	4.5	5.0	5.5	V
$V_{DD}3V3$	Voltage regulator output voltage at pin $V_{DD}3V3$		3.0	3.3	3.6	
$V_{DD}5V$	Supply voltage at pin $V_{DD}5V$	3.3V Operation (pin $V_{DD}5V$ and $V_{DD}3V3$ connected)	3.0	3.3	3.6	V
$V_{DD}3V3$	Supply voltage at pin $V_{DD}3V3$		3.0	3.3	3.6	
V_{ON}	Power-on reset thresholds On voltage; 300mV typ. hysteresis	DC supply voltage 3.3V ($V_{DD}3V3$)	1.37	2.2	2.9	V
V_{OFF}	Power-on reset thresholds Off voltage; 300mV typ. hysteresis		1.08	1.9	2.6	
Programming Conditions						
V_{PROG}	Programming voltage	Voltage applied during programming	3.3		3.6	V
$V_{ProgOff}$	Programming voltage off level	Line must be discharged to this level	0		1	V
I_{PROG}	Programming current	Current during programming			100	mA
$R_{programmed}$	Programmed fuse resistance (log 1)	10µA maximum current@100mV	100k		∞	Ω
$R_{unprogrammed}$	Unprogrammed fuse resistance (log 0)	2mA maximum current@100mV	50		100	Ω
DC Characteristics CMOS Schmitt-Trigger Inputs: CLK, CSn (CSn = Internal Pull-up)						
V_{IH}	High level input voltage	Normal operation	0.7 * $V_{DD}5V$			V
V_{IL}	Low level input voltage				0.3 * $V_{DD}5V$	V
V_{Ion}- V_{Ioff}	Schmitt Trigger hysteresis		1			V
I_{LEAK}	Input leakage current	CLK only	-1		1	µA
I_{iL}	Pull-up low level input current	CSn only, $V_{DD}5V$: 5.0V	-30		-100	
DC Characteristics CMOS / Program Input: PDIO						
V_{IH}	High level input voltage		0.7 * $V_{DD}5V$		$V_{DD}5V$	V
V_{PROG}	High level input voltage	During programming, Either with 3.3V or 5V supply	3.3		3.6	V
V_{IL}	Low level input voltage				0.3 * $V_{DD}5V$	V
I_{iL}	High level input current	$V_{DD}5V$: 5.5V	30		100	µA
DC Characteristics CMOS Output Open Drain: MagINCn, MagDECn						
I_{OZ}	Open drain leakage current				1	µA
V_{OL}	Low level output voltage				V_{SS} +0.4	V

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_O	Output current	$V_{DD}5V$: 4.5V			4	mA
		$V_{DD}5V$: 3V			2	
DC Characteristics CMOS Output: PWM						
V_{OH}	High level output voltage		$V_{DD}5V-0.5$			V
V_{OL}	Low level output voltage				$V_{SS}+0.4$	V
I_O	Output current	$V_{DD}5V$: 4.5V			4	mA
		$V_{DD}5V$: 3V			2	
DC Characteristics CMOS Output: A, B, Index						
V_{OH}	High level output voltage		$V_{DD}5V-0.5$			V
V_{OL}	Low level output voltage				$V_{SS}+0.4$	V
I_O	Output current	$V_{DD}5V$: 4.5V			4	mA
		$V_{DD}5V$: 3V			2	
DC Characteristics Tri-state CMOS Output: DO						
V_{OH}	High level output voltage		$V_{DD}5V-0.5$			V
V_{OL}	Low level output voltage				$V_{SS}+0.4$	V
I_O	Output current	$V_{DD}5V$: 4.5V			4	mA
		$V_{DD}5V$: 3V			2	
I_{OZ}	Tri-state leakage current				1	µA

6.1 System Specifications

T_{AMB} = -40 to +150ºC, $V_{DD}5V$ = 3.0 to 3.6V (3V operation) VDD5V = 4.5 to 5.5V (5V operation) unless otherwise noted.

Table 4. Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
RES	Resolution	0.088 deg			12	bit
INL_{opt}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} =25ºC.			±0.5	deg
INL_{temp}	Integral non-linearity (optimum)	Maximum error with respect to the best line fit. Centered magnet without calibration, T_{AMB} = -40 to +150ºC			±0.9	deg
INL	Integral non-linearity	Best line fit = (Err_{max} − Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, T_{AMB} = -40 to +150ºC			±1.4	deg
DNL	Differential non-linearity	12bit, no missing codes			±0.044	deg
TN	Transition noise	1 sigma, fast mode (MODE = 1)			0.06	Deg RMS
		1 sigma, slow mode (MODE = 0 or open)			0.03	

Table 4. *Input Specification*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PwrUp}	Power-up time	Fast mode (Mode = 1); Until status bit OCF = 1			20	ms
		Slow mode (Mode = 0 or open); Until OCF = 1			80	
t_{delay}	System propagation delay absolute output : delay of ADC, DSP and absolute interface	Fast mode (MODE = 1)			96	µs
		Slow mode (MODE = 0 or open)			384	
f_S	Internal sampling rate for absolute output:	T_{AMB} = 25ºC, slow mode (MODE=0 or open)	2.48	2.61	2.74	kHz
		T_{AMB} = -40 to +150ºC, slow mode (MODE=0 or open)	2.35	2.61	2.87	
f_S	Internal sampling rate for absolute output	T_{AMB} = 25ºC, fast mode (MODE = 1)	9.90	10.42	10.94	kHz
		T_{AMB} = -40 to +150ºC, fast mode (MODE=1)	9.38	10.42	11.46	
CLK/SEL	Read-out frequency	Maximum clock frequency to read out serial data			1	MHz

Figure 3. *Integral and Differential Non-Linearity Example*

Integral Non-Linearity (INL) is the maximum deviation between actual position and indicated position.

Differential Non-Linearity (DNL) is the maximum deviation of the step length from one position to the next.

Transition Noise (TN) is the repeatability of an indicated position.

7 Timing Characteristics

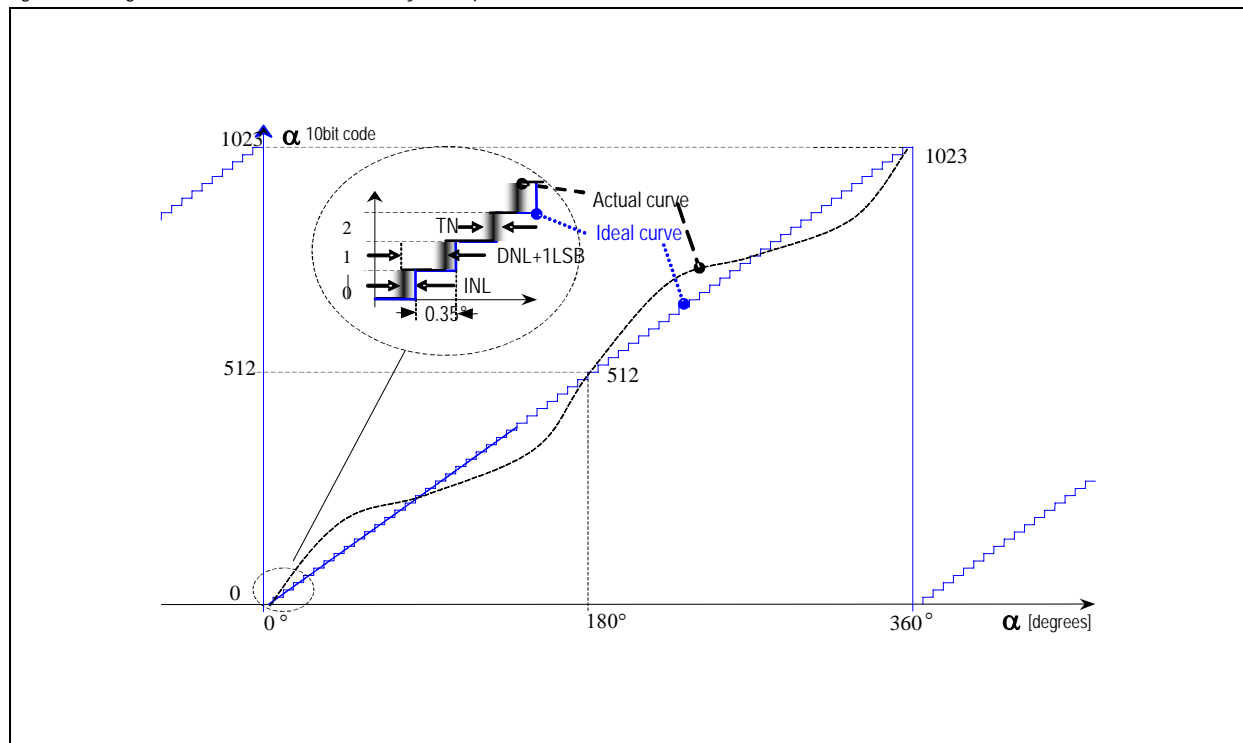T_{AMB}= -40 to +150ºC, VDD5V= 3.0 to 3.6V (3V operation) VDD5V= 4.5 to 5.5V (5V operation), unless otherwise noted.

Table 5. Timing Characteristics

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
Synchronous Serial Interface (SSI)						
$t_{DOactive}$	Data output activated (logic high)	Time between falling edge of CSn and data output activated			100	ns
t_{CLKFE}	First data shifted to output register	Time between falling edge of CSn and first falling edge of CLK	500			ns
$T_{CLK/2}$	Start of data output	Rising edge of CLK shifts out one bit at a time	500			ns
$t_{DOvalid}$	Data output valid	Time between rising edge of CLK and data output valid			413	ns
$t_{DOtristate}$	Data output tri-state	After the last bit DO changes back to "tri-state"			100	ns
t_{CSn}	Pulse width of CSn	CSn =high; To initiate read-out of next angular position	500			ns
f_{CLK}	Read-out frequency	Clock frequency to read out serial data	>0		1	MHz
Pulse Width Modulation Output						
f_{PWM}	PWM frequency	Signal period = 4098µs ±10% at T_{AMB} = -40 to +150ºC	220	244	268	Hz
PW_{MIN}	Minimum pulse width	Position 0d; angle 0 degree	0.90	1	1.10	µs
PW_{MAX}	Maximum pulse width	Position 4098d; angle 359.91 degrees	3686	4096	4506	µs
Programming Conditions						
t_{PROG}	Programming time per bit	Time to prog. a singe fuse bit	10		20	µs
t_{CHARGE}	Refresh time per bit	Time to charge the cap after t_{PROG}	1			µs
f_{LOAD}	LOAD frequency	Data can be loaded at n x 2µs			500	kHz
f_{READ}	READ frequency	Read the data from the latch			2.5	MHz
f_{WRITE}	WRITE frequency	Write the data to the latch			2.5	MHz

8 Detailed Description

The AS5245 is manufactured in a CMOS standard process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip. The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5245 provides accurate high-resolution absolute angular position information. For this purpose, a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals. The DSP is also used to provide digital information at the outputs MagINCn and MagDECn that indicate movements of the used magnet towards or away from the device's surface. A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information (see Figure 16).

The AS5245 senses the orientation of the magnetic field and calculates a 12-bit binary code. This code can be accessed via. a Synchronous Serial Interface (SSI). In addition, an absolute angular representation is given by a Pulse Width Modulated signal at pin 12 (PWM). This PWM signal output also allows the generation of a direct proportional analog voltage, by using an external Low-Pass-Filter. The AS5245 is tolerant to magnet misalignment and magnetic stray fields due to differential measurement technique and Hall sensor conditioning circuitry.

Figure 4. Typical Arrangement of AS5245 and Magnet
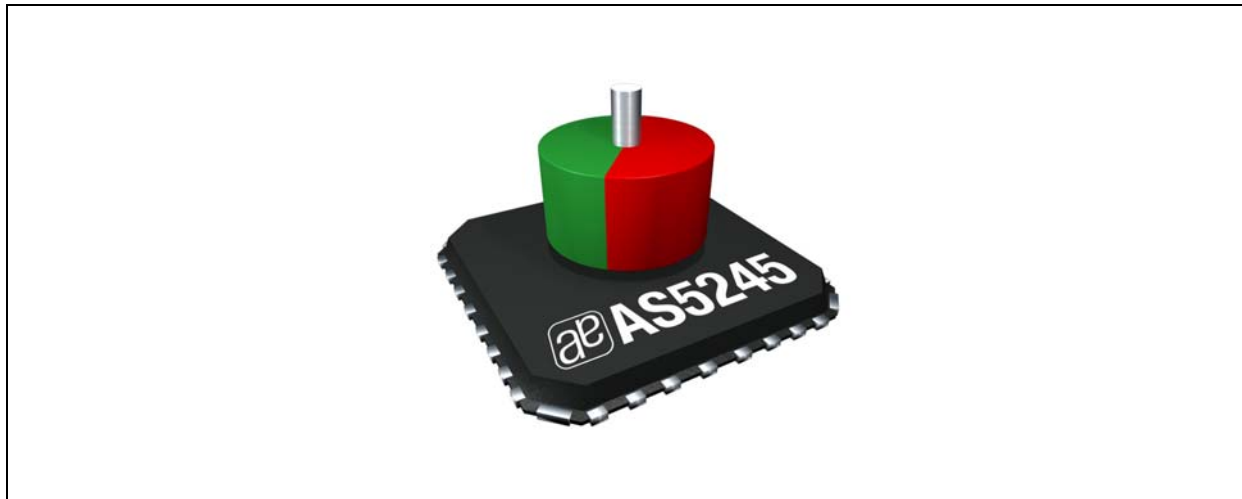
8.1 Mode_Index Pin

The Mode_Index pin activates or deactivates an internal filter that is used to reduce the analog output noise. Activating the filter (Mode pin = LOW or open) provides a reduced output noise of 0.03º rms. At the same time, the output delay is increased to 384µs. This mode is recommended for high precision, low speed applications.

Deactivating the filter (Mode pin = HIGH) reduces the output delay to 96µs and provides an output noise of 0.06º rms. This mode is recommended for higher speed applications.

Setting up the Mode pin affects the following parameters:

Table 6. Slow and Fast Mode Parameters

Parameter	Slow Mode (mode=low or open)	Fast Mode (mode=high, V_{DD}=5V)
Sampling rate	2.61 kHz (384 µs)	10.42 kHz (96µs)
Transition noise (1 sigma)	$\leq 0.03º$ rms	$\leq 0.06º$ rms
Output delay	384µs	96µs
Maximum speed @ 4096 samples/rev	38 rpm	153 rpm
Maximum speed @ 1024 samples/rev	153 rpm	610 rpm
Maximum speed @ 256 samples/rev	610 rpm	2441 rpm
Maximum speed @ 64 samples/rev	2441 rpm	9766 rpm

Note: A change of the Mode during operation is not allowed. The setup must be constant during power up and during operation.

8.2 Synchronous Serial Interface (SSI)

Figure 5. Synchronous Serial Interface with Absolute Angular Position Data
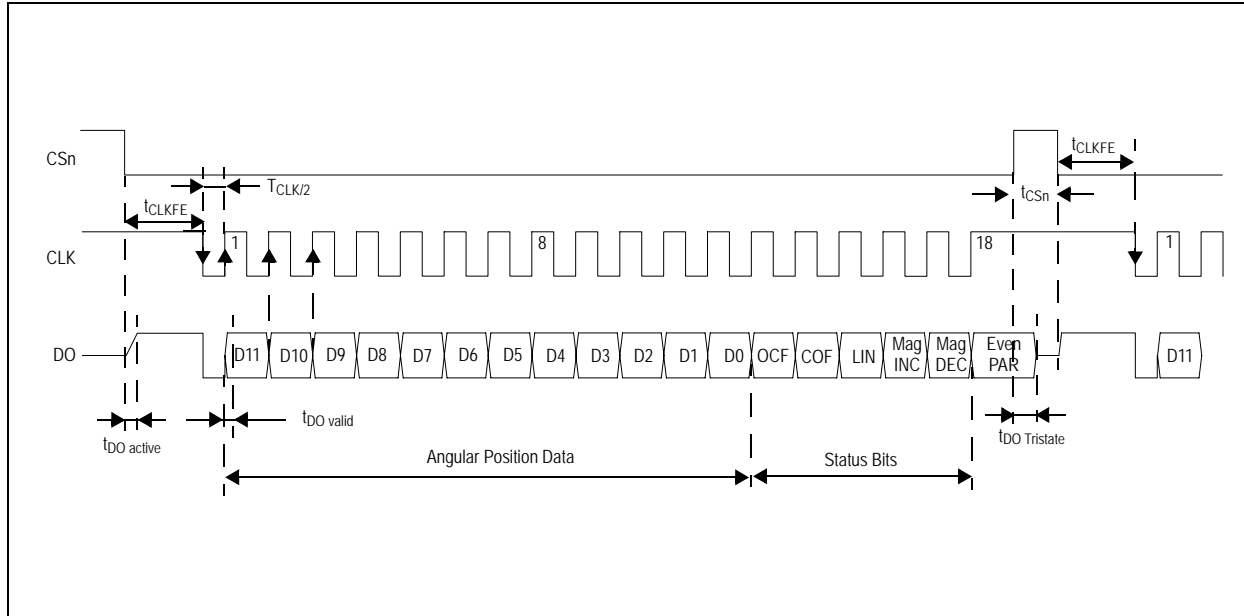
If CSn changes to logic low, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated.

■ After a minimum time $t_{CLK\ FE}$, data is latched into the output shift register with the first falling edge of CLK.

■ Each subsequent rising CLK edge shifts out one bit of data.

■ The serial word contains 18 bits, the first 12 bits are the angular information D[11:0], the subsequent 6 bits contain system information, about the validity of data such as OCF, COF, LIN, Parity and Magnetic Field status (increase/decrease).

■ A subsequent measurement is initiated by a "high" pulse at CSn with a minimum duration of t_{CSn}.

8.2.1 Serial Data Contents

D11:D0 – Absolute angular position data (MSB is clocked out first).

OCF – (Offset Compensation Finished). Logic high indicates the finished Offset Compensation Algorithm.

COF – (Cordic Overflow). Logic high indicates an out of range error in the CORDIC part. When this bit is set, the data at D9:D0 is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

LIN – (Linearity Alarm). Logic high indicates that the input field generates a critical output linearity. When this bit is set, the data at D9:D0 may still be used, but can contain invalid data. This warning may be resolved by bringing the magnet within the X-Y-Z tolerance limits.

Even Parity – Bit for transmission error detection of bits 1…17 (D11…D0, OCF, COF, LIN, MagINC, MagDEC). Placing the magnet above the chip, angular values increase in clockwise direction by default.

Data D11:D0 is valid, when the status bits have the following configurations:

Table 7. Status Bit Outputs

OCF	COF	LIN	Mag INC	Mag DEC	Parity
1	0	0	0	0	Even checksum of bits 1:15
			0	1	
			1	0	
			1	1	

Note: MagInc=MagDec=1 is only recommended in YELLOW mode (see Table 8)

8.2.2 Z-axis Range Indication (Push Button Feature, Red/Yellow/Green Indicator)

The AS5245 provides several options of detecting movement and distance of the magnet in the Z-direction. Signal indicators MagINCn and MagDECn are available both as hardware pins (pins #1 and 2) and as status bits in the serial data stream (see Figure 5). Additionally, an OTP programming option is available with bit MagCompEn that enables additional features:

In the default state, the status bits MagINC, MagDec and pins MagINCn, MagDECn have the following function:

Table 8. Magnetic Field Strength Red-Yellow-Green Indicator (OTP option)

Status Bits			Hardware Pins		OPT: Mag CompEn = 1 (Red-Yellow-Green Programming Option)
Mag INC	Mag DEC	LIN	Mag INCn	Mag DECn	Description
0	0	0	Off	Off	No distance change Magnetic input field OK (GREEN range, ~45…75mT)
1	1	0	On	Off	YELLOW range: magnetic field is ~ 25…45mT or ~75…135mT. The AS5245 may still be operated in this range, but with slightly reduced accuracy.
1	1	1	On	On	RED range: magnetic field is ~<25mT or >~135mT. It is still possible to operate the AS5245 in the red range, but not recommended.
All other combinations			n/a	n/a	Not available

Note: Pin 1 (MagINCn) and pin 2 (MagDECn) are active low via. open drain output and require an external pull-up resistor. If the magnetic field is in range, both outputs are turned off.

The two pins may also be combined with a single pull-up resistor. In this case, the signal is high when the magnetic field is in range. It is low in all other cases (see Table 8).

8.2.3 Incremental Mode

The AS5245 has an internal interpolator block. This function is used if the input magnetic field is too fast and a code position is missing. In this case an interpolation is done.

With the OTP bits OutputMd0 and OutputMd1 a specific mode can be selected. For the available pre-programmed incremental versions (10bit and 12bit), these bits are set during test at austriamicrosystems. These settings are permanent and can not be recovered.

A change of the incremental mode (WRITE command) during operation could cause problems. A power-on-reset in between is recommended. During operation in incremental mode it is recommended setting CSn = High, to disable the SSI-Interface.

Table 9. Incremental Resolution

| Mode	Description	Output Md1	Output Md0	Resolution	DTest1_A and DTest2_B Pulses	Index Width
Default mode	AS5245 function **DTEST1_A** and **DTEST2_B** are not used. The **Mode_Index** pin is used for selection of the decimation rate (low speed/high speed).	0	0			
10 bit Incremental mode (low DNL)	**DTEST1_A** and **DTEST2_B** are used as **A** and **B** signal. In this mode the **Mode_Index** Pin is switched from input to output and will be the **Index** Pin. The decimation rate is set to 64 (fast mode) and cannot be changed from external.	0	1	10	256	1/3 LSB
12 bit Incremental mode (high DNL)		1	0	12	1024	
Sync mode	In this mode a control signal is switched to **DTEST1_A** and **DTEST2_B**.	1	1			

Figure 6. Incremental Output
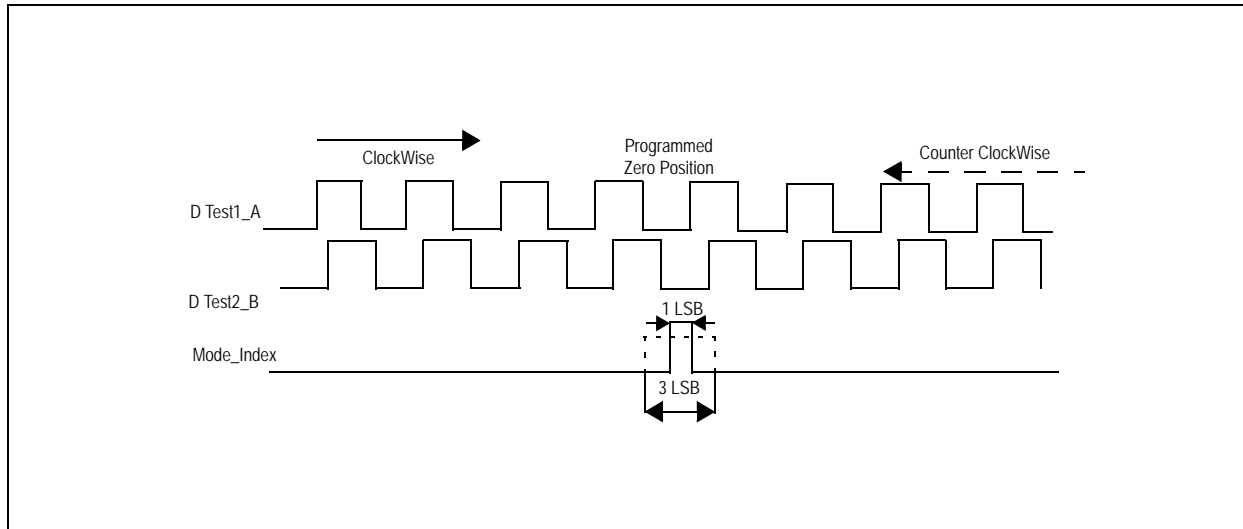
The hysteresis trimming is done at the final test (factory trimming) and set to 4 LSB, related to a 12 bit number.

Incremental Output Hysteresis. To avoid flickering incremental outputs at a stationary magnet position, a hysteresis is introduced. In case of a rotational direction change, the incremental outputs have a hysteresis of 4 LSB. Regardless of the programmed incremental resolution, the hysteresis of 4 LSB always corresponds to the highest resolution of 12 bit. In absolute terms, the hysteresis is set to 0.35 degrees for all resolutions. For constant rotational directions, every magnet position change is indicated at the incremental outputs (see Figure 7). For example, if the magnet turns clockwise from position "x+3" to "x+4", the incremental output would also indicate this position accordingly. A change of the magnet's rotational direction back to position "x+3" means that the incremental output still remains unchanged for the duration of 4 LSB, until position "x+2"is reached. Following this direction, the incremental outputs will again be updated with every change of the magnet position.

Figure 7. Hysteresis Window for Incremental Outputs
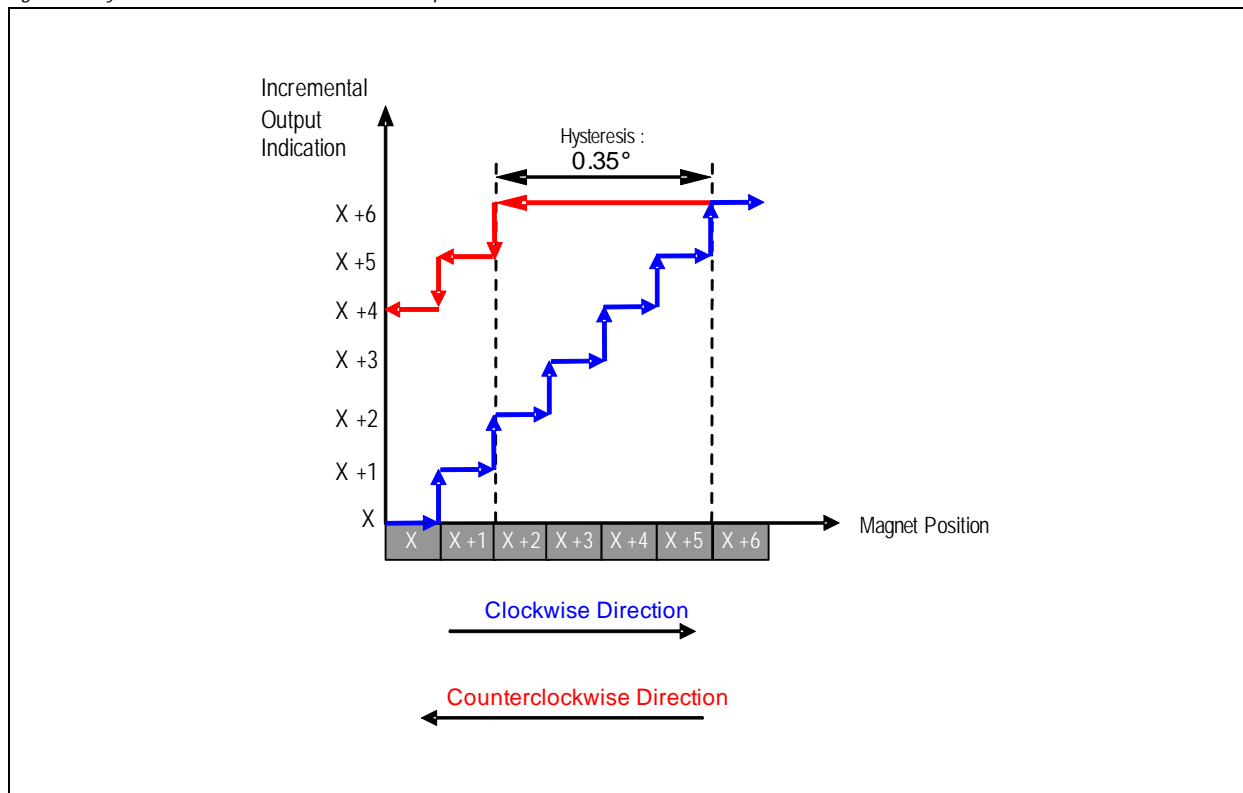
Incremental Output Validity. During power on the incremental output is kept stable high until the offset compensation is finished and the CSn is low (internal Pull Up) the first time. In quadrature mode A = B = Index = high indicates an invalid output. If the interpolator recognizes a difference larger than 128 steps between two samples, it holds the last valid state. The interpolator synchronizes up again with the next valid difference. This avoids undefined output burst, e.g. if no magnet is present.

8.2.4 Sync Mode

This mode is used to synchronize the external electronic with the AS5245. In this mode, two signals are provided at the pins DTEST1_A and DTEST2_B. By setting of Md0=1 and Md1=1 in the OTP register, the Sync mode will be activated.

Figure 8. DTest1_A and DTest2_B
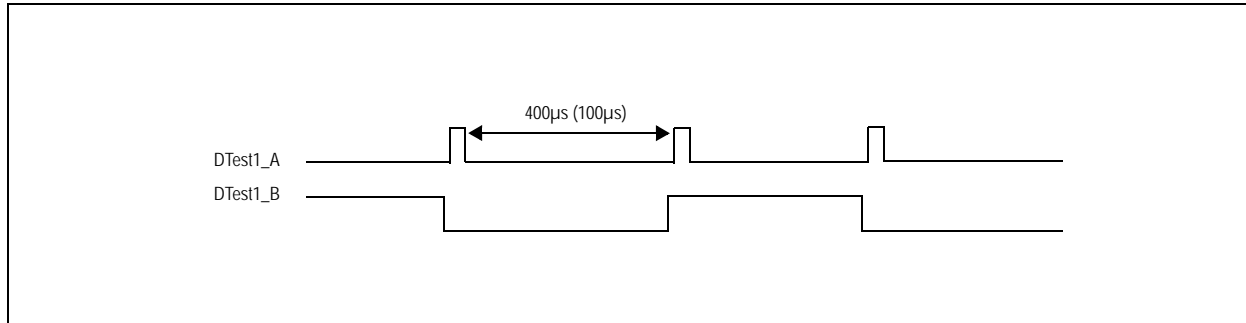
Every rising edge at DTEST1_A indicates that new data in the device is available. With this signal it is possible to trigger an external customer Microcontroller (interrupt) and start the SSI readout. DTEST2_B indicates the phase of available data.

8.2.5 Sine/Cosine Mode

This mode can be enabled by setting the OTP Factory-bit FS2. If this mode is activated, the 16 bit sinus and 16 bit cosines digital data of both channels will be switched out. Due to the high resolution of 16 bits of the data stream, an accurate calculation can be done externally. In this mode, the open drain outputs of DTEST1_A and DTEST2_B are switched to push-pull mode. At Pin MagDECn the clock impulse, at Pin MagINCn the Enable pulse will be switched out. The pin PWM indicates, which phase of signal is being presented. The mode is not available in the default mode.

8.2.6 Daisy Chain Mode

The Daisy Chain mode allows connection of several AS5245s in series, while still keeping just one digital input for data transfer (see "Data IN" in Figure 9). This mode is accomplished by connecting the data output (DO; pin 9) to the data input (PDIO; pin 8) of the subsequent device. The serial data of all connected devices is read from the DO pin of the first device in the chain. The length of the serial bit stream increases with every connected device, it is n * (18+1) bits: n= number of devices. E.g. 38 bit for two devices, 57 bit for three devices, etc.

The last data bit of the first device (Parity) is followed by a dummy bit and the first data bit of the second device (D11), etc. (see Figure 10).

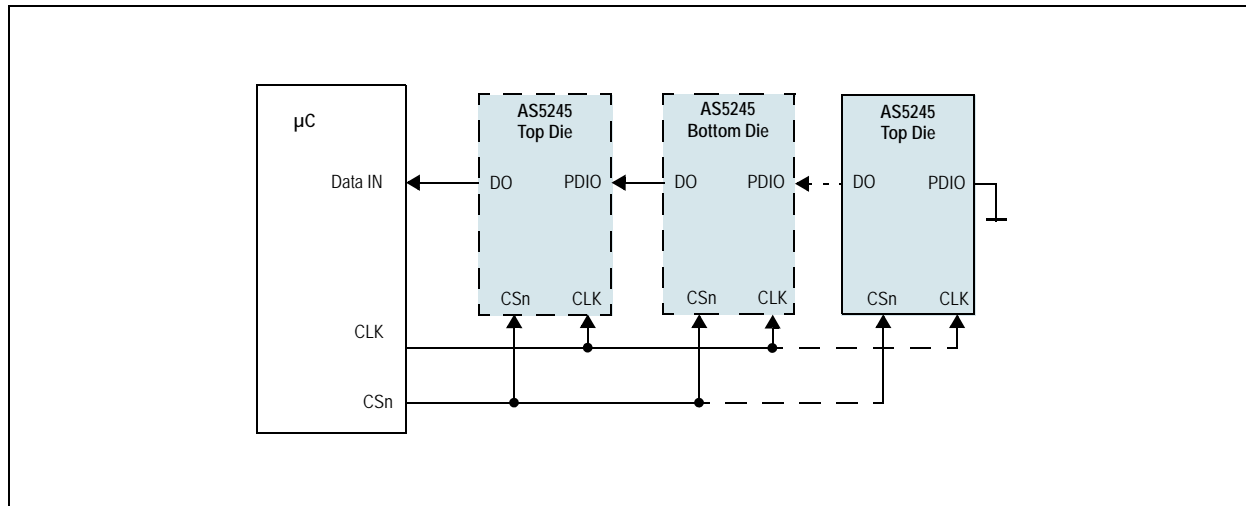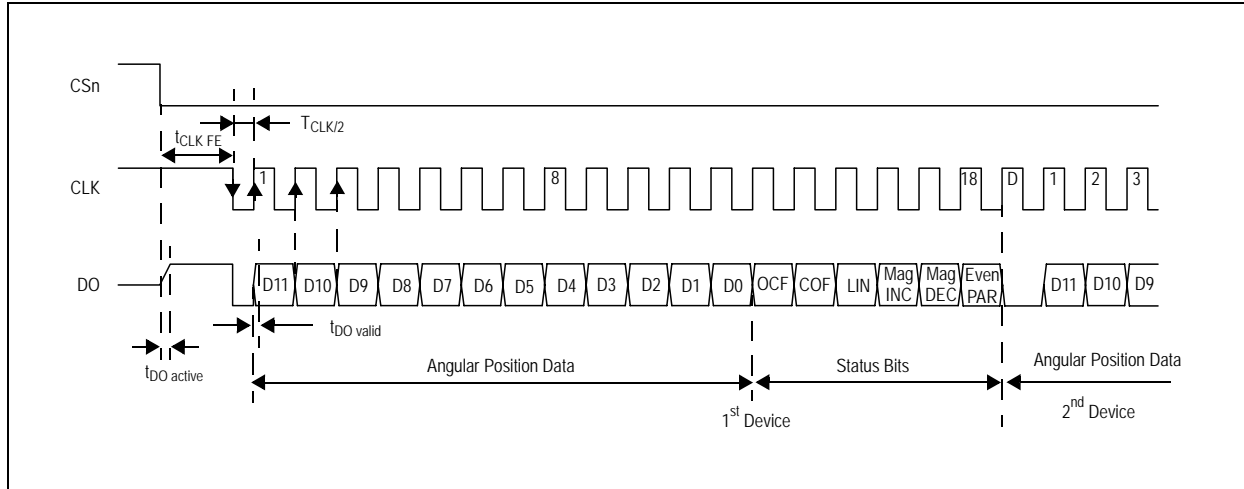*Figure 9. Daisy Chain Hardware Configuration*

Figure 10. Daisy Chain Mode Data Transfer

8.3 Pulse Width Modulation (PWM) Output

The AS5245 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. For angle position 0 to 4094:

$$Position = \frac{t_{on} \cdot 4098}{(t_{on} + t_{off})} - 1 \qquad \text{(EQ 1)}$$

Examples:

1. An angle position of 180º will generate a pulse width ton = 2049μs and a pause toFF of 2049 μs resulting in Position = 2048 after the calculation: 2049 * 4098 / (2049 + 2049) -1 = 2048

2. An angle position of 359.8º will generate a pulse width ton = 4095μs and a pause toFF of 3 μs resulting in Position = 4094 after the calculation: 4095 * 4098 / (4095 + 3) -1 = 4094

Exception:

1. An angle position of 359.9º will generate a pulse width ton = 4097μs and a pause toFF of 1 μs resulting in Position = 4096 after the calculation: 4097 * 4098 / (4097 + 1) -1 = 4096

The PWM frequency is internally trimmed to an accuracy of ±5% (±10% over full temperature range). This tolerance can be cancelled by measuring the complete duty cycle as shown above.

Figure 11. PWM Output Signal
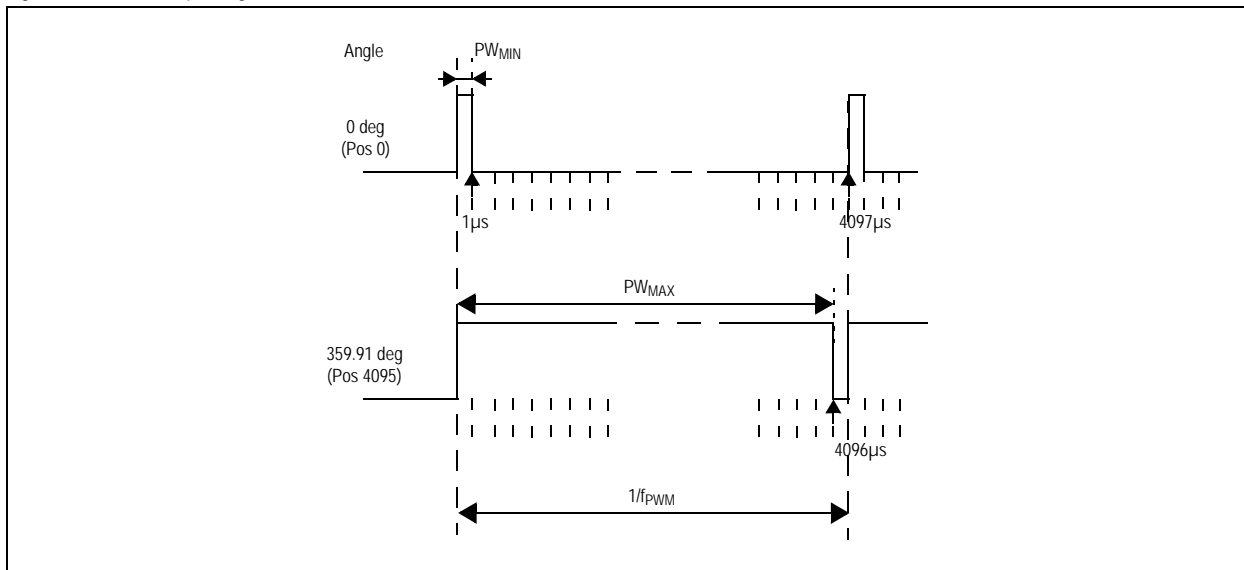
8.3.1 Changing the PWM Frequency

The PWM frequency of the AS5245 can be divided by two by setting a bit (PWMhalfEN) in the OTP register (see Programming the AS5245 on page 17). With PWMhalfEN = 0, the PWM timing is as shown in Table 10:

Table 10. PWM Signal Parameters (Default mode)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	244	Hz	Signal period: 4097µs
PW_{MIN}	MIN pulse width	1	µs	- Position 0d - Angle 0 deg
PW_{MAX}	MAX pulse width	4096	µs	- Position 4095d - Angle 359,91 deg

When PWMhalfEN = 1, the PWM timing is as shown in Table 11:

Table 11. PWM Signal Parameters with Half Frequency (OTP option)

Symbol	Parameter	Typ	Unit	Note
f_{PWM}	PWM frequency	122	Hz	- Position 0d - Angle 0 deg
PW_{MIN}	MIN pulse width	2	µs	- Position 4095d - Angle 359,91 deg
PW_{MAX}	MAX pulse width	8192	µs	- Position 0d - Angle 0 deg

8.4 Analog Output

An analog output can be generated by averaging the PWM signal, using an external active or passive low pass filter. The analog output voltage is proportional to the angle: 0º= 0V; 360º = VDD5V.

Using this method, the AS5245 can be used as direct replacement of potentiometers.

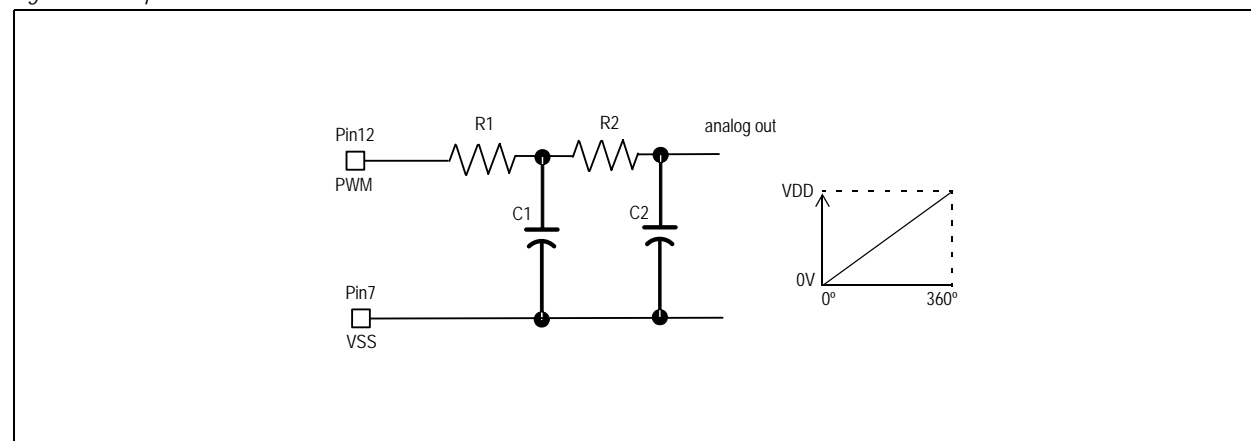*Figure 12. Simple 2nd Order Passive RC Low Pass Filter*

Figure 12 shows an example of a simple passive low pass filter to generate the analog output.

$$R1,R2 \geq 4k7 \qquad C1,C2 \geq 1\mu F / 6V \qquad\qquad (EQ\ 2)$$

R1 should be greater than or equal to 4k7 to avoid loading of the PWM output. Larger values of Rx and Cx will provide better filtering and less ripple, but will also slow down the response time.

9 Application Information

The benefits of AS5245 are as follows:

- Complete system-on-chip

- Angle measurement with programmable range up to 360º

- High reliability due to non-contact magnetic sensing

- Ideal for applications in harsh environments

- Robust system, tolerant to magnet misalignment, airgap variations, temperature variations and external magnetic fields

- No calibration required

- Building of redundancy systems with plausibility checks

9.1 Programming the AS5245

After power-on, programming the AS5245 is enabled with the rising edge of CSn with PDIO = high and CLK = low.

The AS5245 programming is a one-time programming (OTP) method, based on poly silicon fuses. The advantage of this method is that a programming voltage of only 3.3V to 3.6V is required for programming.

The OTP consists of 52 bits, of which 21 bits are available for user programming. The remaining 31 bits contain factory settings and a unique chip identifier (Chip-ID).

A single OTP cell can be programmed only once. Per default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, as long as only unprogrammed "0"-bits are programmed to "1".

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command at any time. This setting will be cleared and overwritten with the hard programmed OTP settings at each power-up sequence or by a LOAD operation. Use application note AN514X_10 to get more information about the programming options.

The OTP memory can be accessed in the following ways:

- **Load Operation:** The Load operation reads the OTP fuses and loads the contents into the OTP register. A Load operation is automatically executed after each power-on-reset.

- **Write Operation:** The Write operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another Write or Load operation.

- **Read Operation:** The Read operation reads the contents of the OTP register, for example to verify a Write command or to read the OTP memory after a Load command.

- **Program Operation:** The Program operation writes the contents of the OTP register permanently into the OTP ROM.

- **Analog Readback Operation:** The Analog Readback operation allows a quantifiable verification of the programming. For each programmed or unprogrammed bit, there is a representative analog value (in essence, a resistor value) that is read to verify whether a bit has been successfully programmed or not.

9.1.1 Zero Position Programming

Zero position programming is an OTP option that simplifies assembly of a system, as the magnet does not need to be manually adjusted to the mechanical zero position. Once the assembly is completed, the mechanical and electrical zero positions can be matched by software. Any position within a full turn can be defined as the permanent new zero position.

For zero position programming, the magnet is turned to the mechanical zero position (e.g. the "off"-position of a rotary switch) and the actual angular value is read.

This value is written into the OTP register bits Z35:Z46.

Note: The zero position value may also be modified before programming, e.g. to program an electrical zero position that is 180º (half turn) from the mechanical zero position, just add 2048 to the value read at the mechanical zero position and program the new value into the OTP register.

9.1.2 OTP Memory Assignment

Table 12. OTP Bit Assignment

Bit	Symbol	Function	
	mbit1	Factory Bit 1	
51	PWMhalfEN_Index width	PMW frequency Index pulse width	Customer Section
50	MagCompEn	Alarm mode	Customer Section
49	pwmDIS	Disable PWM	Customer Section
48	Output Md0	Default, 10 bit inc, 12 bit inc	Customer Section
47	Output Md1	Sync mode	Customer Section
46	Z0	12 bit Zero Position	Customer Section
:	:	12 bit Zero Position	Customer Section
35	Z11	12 bit Zero Position	Customer Section
34	CCW	Direction	Customer Section
33	RA0	Redundancy Address	Customer Section
:	:	Redundancy Address	Customer Section
29	RA4	Redundancy Address	Customer Section
28	FS 0	Factory Bit	Factory Section
27	FS 1	Factory Bit	Factory Section
26	FS 2	Factory Bit	Factory Section
25	FS 3	Factory Bit	Factory Section
24	FS 4	Factory Bit	Factory Section
23	FS 5	Factory Bit	Factory Section
:	:	Factory Bit	Factory Section
20	FS 9	Factory Bit	Factory Section
17	ChipID0	18 bit Chip ID	ID Section
16	ChipID1	18 bit Chip ID	ID Section
:	:	18 bit Chip ID	ID Section
0	ChipID17	18 bit Chip ID	ID Section
	mbit0	Factory Bit 0	

9.1.3 User Selectable Settings

The AS5245 allows programming of the following user selectable options:

- **PWMhalfEN_Indexwidth**: Setting this bit, the PWM pulse will be divided by 2, in case of quadrature incremental mode A/B/Index setting of Index impulse width from 1 LSB to 3LSB.
- **MagCompEN:** The green/yellow mode can be enabled by setting of this bit.
- **Output Md0:** Setting this bit enables sync- or 10bit incremental mode (see Table 9). It is already set by Austriamicrosystems.
- **Output Md1:** Setting this bit enables sync- or 12bit incremental mode (see Table 9)
- **Z [11:0]:** Programmable Zero / Index Position
- **CCW:** Counter Clockwise Bit
   ccw=0 – angular value increases in clockwise direction
   ccw=1 – angular value increases in counterclockwise direction
- **RA [4:0]:** Redundant Address: an OTP bit location addressed by this address is always set to "1" independent of the corresponding original OTP bit setting

9.1.4 OTP Default Setting

The AS5245 can also be operated without programming. The default, un-programmed setting is:

- **Output Md0, Output MD1:** 00= Default mode
- **Z0 to Z11:** 00 = no programmed zero position
- **CCW:** 0 = clockwise operation
- **RA4 to RA0:** 0 = no OTP bit is selected
- **MagCompEN: 1** = The green / yellow mode is enabled.

9.1.5 Redundancy

For a better programming reliability, a redundancy is implemented. This function can be used in cases where the programming of one bit fails. With an address RA(4:0), one bit can be selected and programmed.

Table 13. Redundancy Addressing

Address	PWMhalfEN_Indexwidth	MagCompEN	pwmDIS	Output Md0	Output Md1	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	Z9	Z10	Z11	CCW
00000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00001	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00010	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00011	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00100	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00101	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
00110	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
00111	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
01000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
01001	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
01010	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
01011	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
01100	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
01101	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
01110	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
01111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
10000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
10001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
10010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
10101	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

9.1.6 Redundant Programming Option

In addition to the regular programming, a redundant programming option is available. This option allows that one selectable OTP bit can be set to "1" (programmed state) by writing the location of that bit into a 5-bit address decoder. This address can be stored in bits RA4…RA0 in the OTP user settings.

Example: setting RA4…0 to "00001" will select bit 51 = PWhalfEN_Indexwidth, "00010" selects bit 50 = MagCompEN, "10010" selects bit 34 =CCW, etc.

9.2 Alignment Mode

The alignment mode simplifies centering the magnet over the center of the chip to gain maximum accuracy.

Alignment mode can be enabled with the falling edge of CSn while PDIO = logic high (see Figure 13). The Data bits D11-D0 of the SSI change to a 12-bit displacement amplitude output. A high value indicates large X or Y displacement, but also higher absolute magnetic field strength. The magnet is properly aligned, when the difference between highest and lowest value over one full turn is at a minimum.

Under normal conditions, a properly aligned magnet will result in a reading of less than 128 over a full turn.
The MagINCn and MagDECn indicators will be = 1 when the alignment mode reading is < 128. At the same time, both hardware pins MagINCn (#1) and MagDECn (#2) will be pulled to VSS. A properly aligned magnet will therefore produce a MagINCn = MagDECn = 1 signal throughout a full 360° turn of the magnet.

Stronger magnets or short gaps between magnet and IC may show values larger than 128. These magnets are still properly aligned as long as the difference between highest and lowest value over one full turn is at a minimum.

The Alignment mode can be reset to normal operation by a power-on-reset (disconnect / re-connect power supply) or by a falling edge on CSn with PDIO = low.
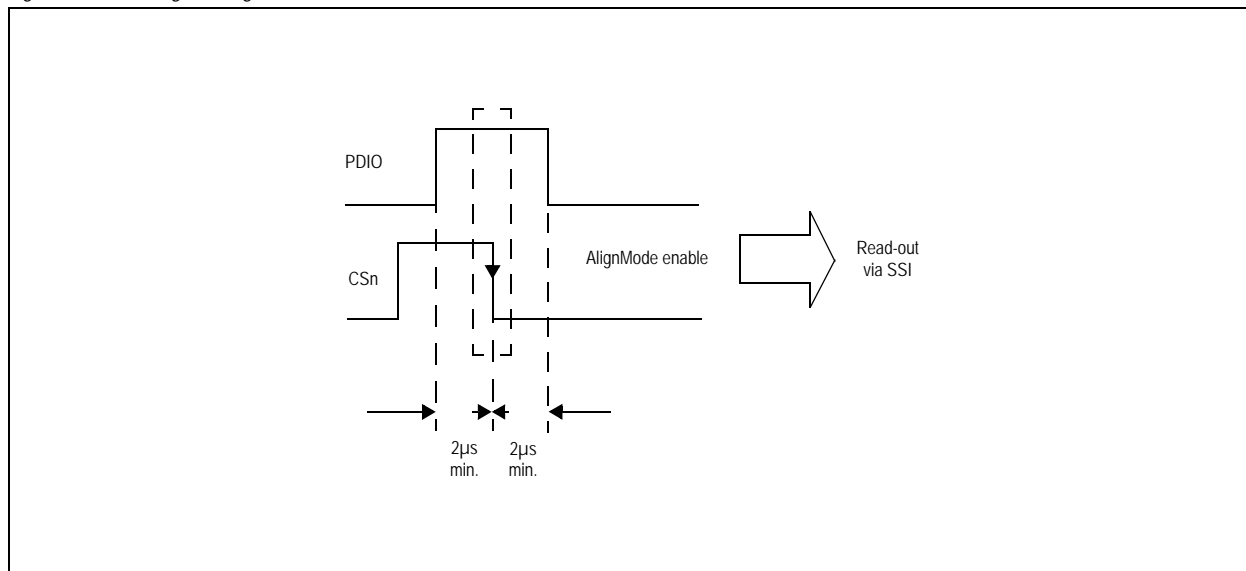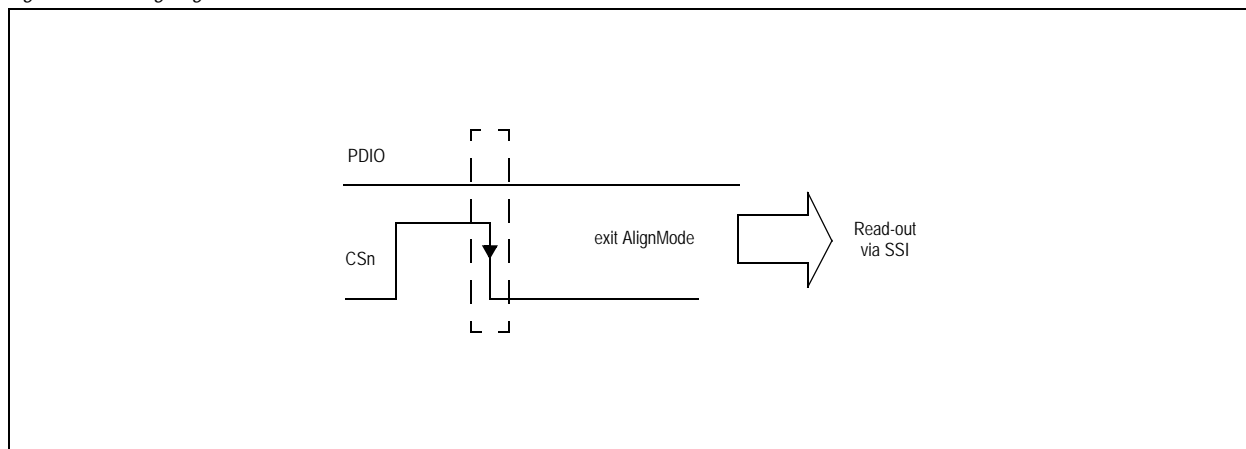
Figure 13. Enabling the Alignment Mode

Figure 14. Exiting Alignment Mode

9.3   3.3V / 5V Operation

The AS5245 operates either at 3.3V ±10% or at 5V ±10%. This is made possible by an internal 3.3V Low-Dropout (LDO) Voltage regulator. The internal supply voltage is always taken from the output of the LDO, meaning that the internal blocks are always operating at 3.3V.

For 3.3V operation, the LDO must be bypassed by connecting VDD3V3 with VDD5V (see Figure 15).

For 5V operation, the 5V supply is connected to pin VDD5V, while VDD3V3 (LDO output) must be buffered by a 1...10µF capacitor, which is supposed to be placed close to the supply pin (see Figure 15).

Note: The VDD3V3 output is intended for internal use only. It must not be loaded with an external load.

The output voltage of the digital interface I/O's corresponds to the voltage at pin VDD5V, as the I/O buffers are supplied from this pin.

*Figure 15.   Connections for 5V / 3.3V Supply Voltages*
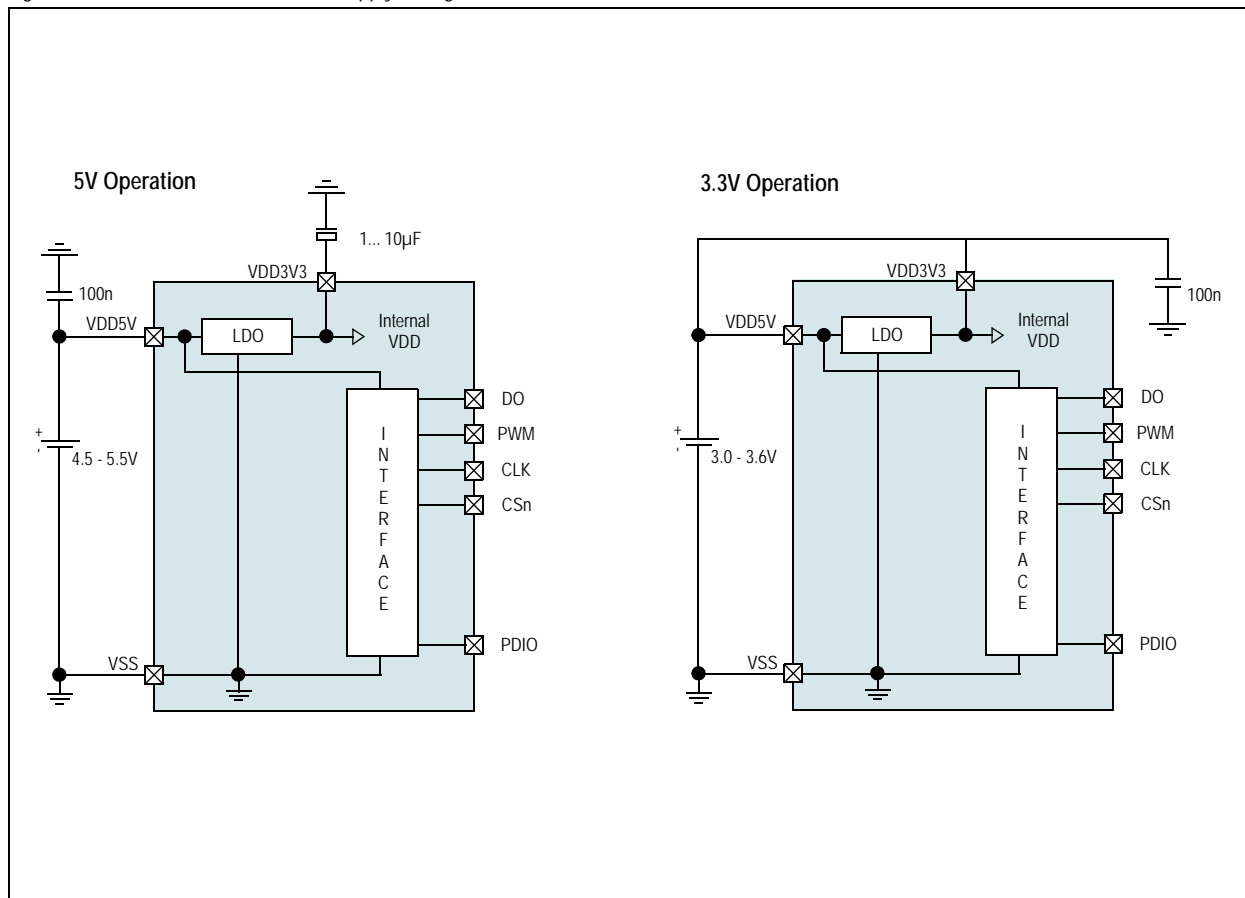
A buffer capacitor of 100nF is recommended in both cases close to pin VDD5V. Note that pin VDD3V3 must always be buffered by a capacitor. It must not be left floating, as this may cause an instable internal 3.3V supply voltage, which may lead to larger than normal jitter of the measured angle.

9.4 Choosing the Proper Magnet

Typically, the magnet should be 6mm in diameter and $\geq$ 2.5mm in height. Magnetic materials such as rare earth AlNiCo/SmCo5 or NdFeB are recommended. The magnetic field strength perpendicular to the die surface has to be in the range of ±45mT…±75mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic field B_V at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±45mT…±75mT (see Figure 16).

Figure 16. Typical Magnet (6x3mm) and Magnetic Field Distribution
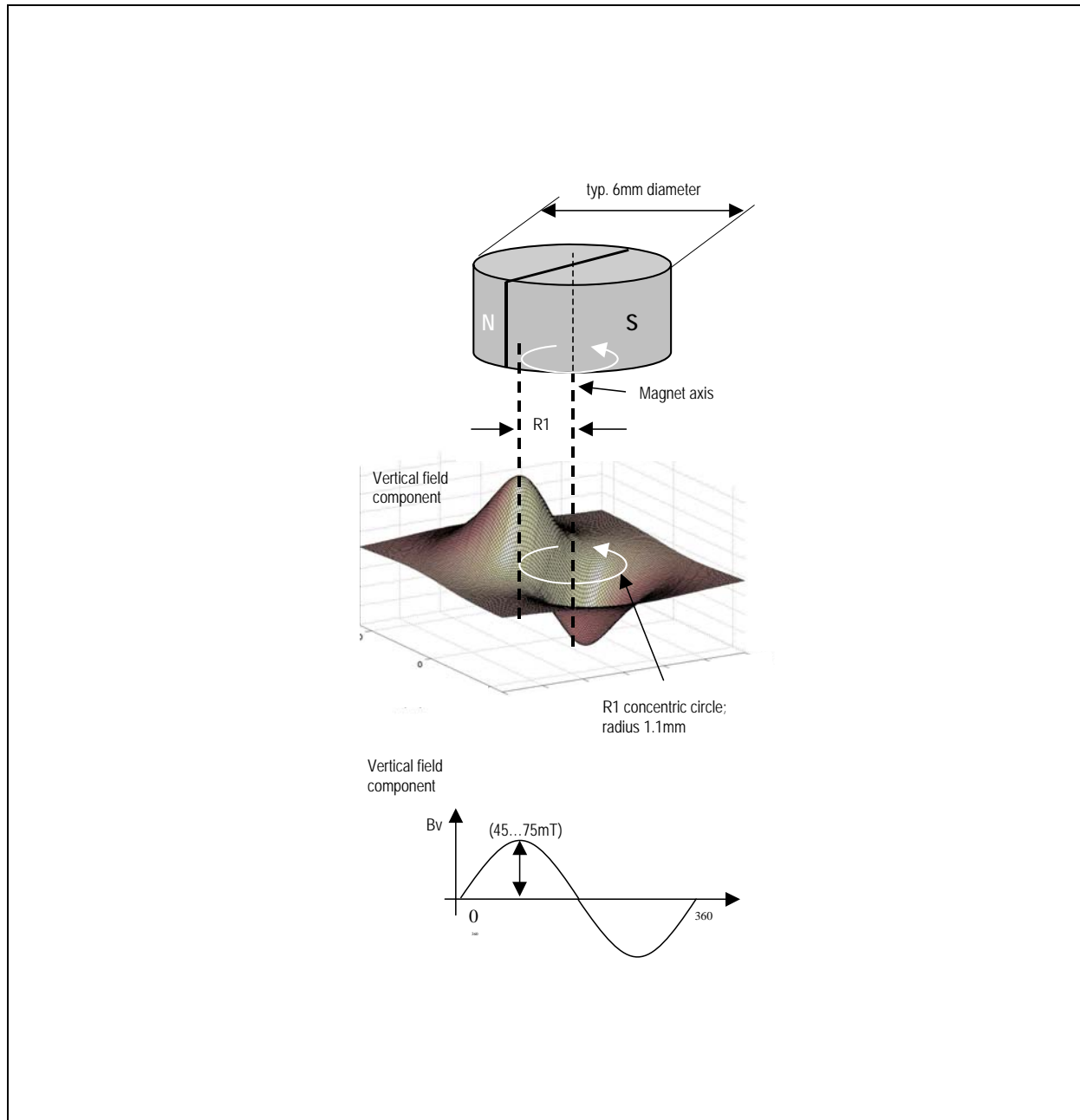
9.5 Failure Diagnostics

The AS5245 also offers several diagnostic and failure detection features, which are discussed in detail further in the document.

9.5.1 Magnetic Field Strength Diagnosis

By Software: The MagINC and MagDEC status bits will both be high when the magnetic field is out of range.

By Hardware: Pins #1 (MagINCn) and #2 (MagDECn) are open-drain outputs and will both be turned on (= low with external pull-up resistor) when the magnetic field is out of range. If only one of the outputs are low, the magnet is either moving towards the chip (MagINCn) or away from the chip (MagDECn).

9.5.2 Power Supply Failure Detection

By Software: If the power supply to the AS5245 is interrupted, the digital data read by the SSI will be all "0"s. Data is only valid, when bit OCF is high, hence a data stream with all "0"s is invalid. To ensure adequate low levels in the failure case, a pull-down resistor (~10kΩ) should be added between pin DIO and VSS at the receiving side.

By Hardware: The MagINCn and MagDECn pins are open drain outputs and require external pull-up resistors. In normal operation, these pins are high ohmic and the outputs are high (see Table 8). In a failure case, either when the magnetic field is out of range of the power supply is missing, these outputs will become low. To ensure adequate low levels in case of a broken power supply to the AS5245, the pull-up resistors (~10kΩ) from each pin must be connected to the positive supply at pin 16 (VDD5V).

By Hardware, PWM Output: The PWM output is a constant stream of pulses with 1kHz repetition frequency. In case of power loss, these pulses are missing.

9.6 Angular Output Tolerances

9.6.1 Accuracy

Accuracy is defined as the error between measured angle and actual angle. It is influenced by several factors:

- The non-linearity of the analog-digital converters,
- Internal gain and mismatch errors,
- Non-linearity due to misalignment of the magnet.

As a sum of all these errors, the accuracy with centered magnet = $(Err_{max} - Err_{min})/2$ is specified as better than ±0.5 degrees @ 25ºC (see Figure 19).

Misalignment of the magnet further reduces the accuracy. Figure 18 shows an example of a 3D-graph displaying non-linearity over XY-misalignment. The center of the square XY-area corresponds to a centered magnet (see dot in the center of the graph). The X- and Y- axis extends to a misalignment of ±1mm in both directions. The total misalignment area of the graph covers a square of 2x2 mm (79x79mil) with a step size of 100µm.

For each misalignment step, the measurement as shown in Figure 19 is repeated and the accuracy $(Err_{max} - Err_{min})/2$ (e.g. 0.25º in Figure 19) is entered as the Z-axis in the 3D-graph.

Figure 17. Example of Linearity Error Over XY Misalignment
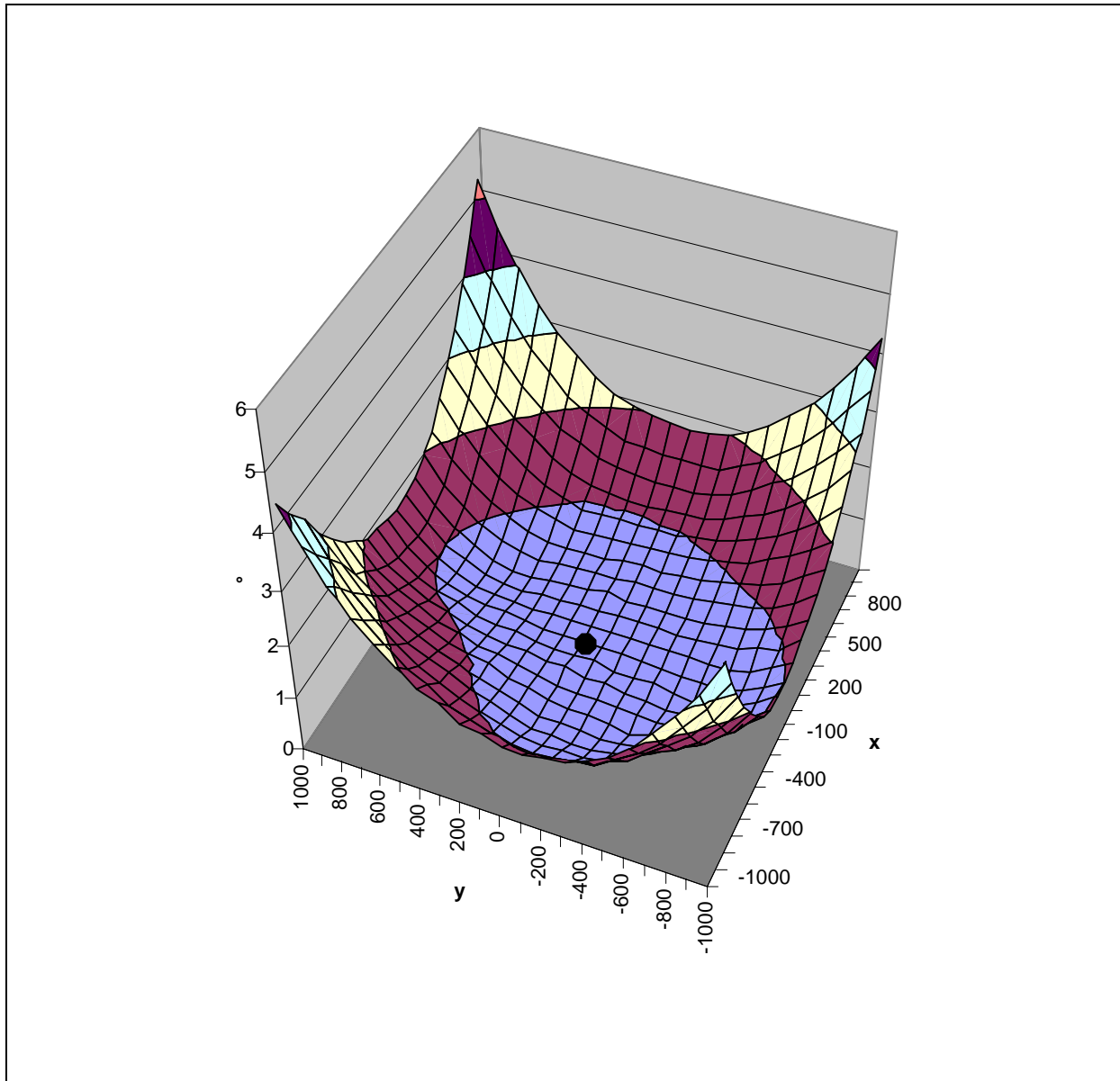
The maximum non-linearity error on this example is better than ±1 degree (inner circle) over a misalignment radius of ~0.7mm. For volume production, the placement tolerance of the IC within the package (±0.235mm) must also be taken into account. The total nonlinearity error over process tolerances, temperature and a misalignment circle radius of 0.25mm is specified better than ±1.4 degrees. The magnet used for this measurement was a cylindrical NdFeB (Bomatec® BMN-35H) magnet with 6mm diameter and 2.5mm in height.

Figure 18.   *Example of Linearity Error Over 360°*
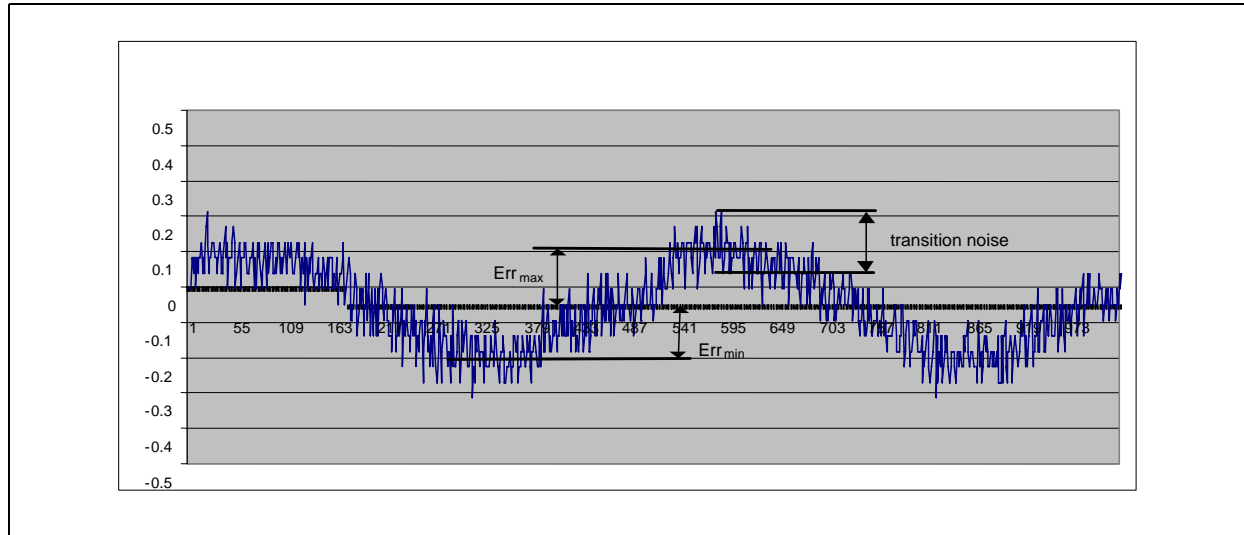
9.6.2   Transition Noise

Transition noise is defined as the jitter in the transition between two steps. Due to the nature of the measurement principle (Hall sensors + Preamplifier + ADC), there is always a certain degree of noise involved. This transition noise voltage results in an angular transition noise at the outputs. It is specified as 0.06 degrees rms (1 sigma)[1] in fast mode (pin MODE = high) and 0.03 degrees rms (1 sigma) in slow mode (pin MODE = low or open). This is the repeatability of an indicated angle at a given mechanical position. The transition noise has different implications on the type of output that is used:

■ **Absolute Output**; **SSI Interface:** The transition noise of the absolute output can be reduced by the user by implementing averaging of readings. An averaging of 4 readings will reduce the transition noise by 6dB or 50%, e.g. from 0.03° rms to 0.015° rms (1 sigma) in slow mode.

■ **PWM Interface:** If the PWM interface is used as an analog output by adding a low pass filter, the transition noise can be reduced by lowering the cutoff frequency of the filter. If the PWM interface is used as a digital interface with a counter at the receiving side, the transition noise may again be reduced by averaging of readings.

■ **Incremental Mode:** In incremental mode, the transition noise influences the period, width and phase shift of the output signals A, B and Index. However, the algorithm used to generate the incremental outputs guarantees no missing or additional pulses even at high speeds (up to 30.000 rpm and higher).

9.6.3   High Speed Operation

Sampling Rate. The AS5245 samples the angular value at a rate of 2.61k (slow mode) or 10.42k (fast mode, selectable by pin MODE) samples per second. Consequently, the absolute outputs are updated each 384µs (96µs in fast mode). At a stationary position of the magnet, the sampling rate creates no additional error.

Absolute Mode. At a sampling rate of 2.6kHz/10.4kHz, the number of samples (n) per turn for a magnet rotating at high speed can be calculated by,

$$n_{slowmode} = \frac{60}{rpm \cdot (384)\mu s} \qquad\qquad (EQ\ 3)$$

$$n_{fastmode} = \frac{60}{rmp \cdot 96\mu s} \qquad\qquad (EQ\ 4)$$

The upper speed limit in slow mode is ~6.000rpm and ~30.000rpm in fast mode. The only restriction at high speed is that there will be fewer samples per revolution as the speed increases (see Table 6). Regardless of the rotational speed, the absolute angular value is always sampled at the highest resolution of 12 bit.

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1.   Statistically, 1 sigma represents 68.27% of readings; 3 sigma represents 99.73% of readings.

Incremental Mode. Incremental encoders are usually required to produce no missing pulses up to several thousand rpms. Therefore, the AS5245 has a built-in interpolator, which ensures that there are no missing pulses at the incremental outputs for rotational speeds of up to 30.000 rpm, even at the highest resolution of 10 bits (512 pulses per revolution).

9.6.4 Propagation Delays

The propagation delay is the delay between the time that the sample is taken until it is converted and available as angular data. This delay is 96μs in fast mode and 384μs in slow mode.

Using the SSI interface for absolute data transmission, an additional delay must be considered, caused by the asynchronous sampling (0 … 1/fsample) and the time it takes the external control unit to read and process the angular data from the chip (maximum clock rate = 1MHz, number of bits per reading = 18).

Angular Error Caused by Propagation Delay. A rotating magnet will cause an angular error caused by the output propagation delay. This error increases linearly with speed:

$$e_{sampling} = rpm * 6 * prop.delay$$

(EQ 5)

Where:
esampling = angular error [º]
rpm = rotating speed [rpm]
prop.delay = propagation delay [seconds]

Note: Since the propagation delay is known, it can be automatically compensated by the control unit processing the data from the AS5245.

9.6.5 Internal Timing Tolerance

The AS5245 does not require an external ceramic resonator or quartz. All internal clock timings for the AS5245 are generated by an on-chip RC oscillator. This oscillator is factory trimmed to ±5% accuracy at room temperature (±10% over full temperature range). This tolerance influences the ADC sampling rate and the pulse width of the PWM output:

- **Absolute Output**; **SSI Interface:** A new angular value is updated every 96μs (typ) in fast mode and every 384μs (typ) in slow mode.

- **PWM Output:** A new angular value is updated every 400μs (typ). The PWM pulse timings t$_{ON}$ and t$_{OFF}$ also have the same tolerance as the internal oscillator. If only the PWM pulse width t$_{ON}$ is used to measure the angle, the resulting value also has this timing tolerance. However, this tolerance can be cancelled by measuring both t$_{ON}$ and t$_{OFF}$ and calculating the angle from the duty cycle (see Pulse Width Modulation (PWM) Output on page 15).

- **Incremental Mode:** In incremental mode, the transition noise influences the period, width and phase shift of the output signals A, B and Index. However, the algorithm used to generate the incremental outputs guarantees no missing or additional pulses even at high speeds (up to 30.000 rpm and higher).

$$Position = \frac{t_{on} \cdot 4097}{(t_{on} + t_{off})} - 1$$

(EQ 6)

9.6.6 Temperature

Magnetic Temperature Coefficient. One of the major benefits of the AS5245 compared to linear Hall sensors is that it is much less sensitive to temperature. While linear Hall sensors require a compensation of the magnet's temperature coefficients, the AS5245 automatically compensates for the varying magnetic field strength over temperature. The magnet's temperature drift does not need to be considered, as the AS5245 operates with magnetic field strengths from ±45…±75mT.

Example:

A NdFeB magnet has a field strength of 75mT @ -40ºC and a temperature coefficient of -0.12% per Kelvin. The temperature change is from -40º to +125º = 165K.The magnetic field change is: 165 x -0.12% = -19.8%, which corresponds to 75mT at -40ºC and 60mT at 125ºC.

The AS5245 can compensate for this temperature related field strength change automatically, no user adjustment is required.

9.6.7 Accuracy over Temperature

The influence of temperature in the absolute accuracy is very low. While the accuracy is less than or equal to ±0.5º at room temperature, it may increase to less then or equal to ±0.9º due to increasing noise at high temperatures.

Timing Tolerance over Temperature. The internal RC oscillator is factory trimmed to ±5%. Over temperature, this tolerance may increase to ±10%. Generally, the timing tolerance has no influence in the accuracy or resolution of the system, as it is used mainly for internal clock generation. The only concern to the user is the width of the PWM output pulse, which relates directly to the timing tolerance of the internal oscillator. This influence, however, can be cancelled by measuring the complete PWM duty cycle instead of just the PWM pulse.

9.7   AS5245 Differences to AS5045

All parameters are according to AS5045 data sheet except for the parameters shown below:

Table 14. Difference Between AS5245 and AS5045

Building Block	AS5245	AS5045
Resolution	12bits, 0.088º/step.	12bits, 0.088º/step.
Ambient temperature range	-40ºC to +150ºC	-40ºC to +125ºC
Data length	read: 18bits (12bits data + 6 bits status) OTP write: 18 bits (12bits zero position + 6 bits mode selection)	read: 18bits (12bits data + 6 bits status) OTP write: 18 bits (12bits zero position + 6 bits mode selection)
Pins 1 and 2	MagINCn, MagDECn: same feature as AS5045, additional OTP option for red-yellow-green magnetic range	MagINCn, MagDECn
Incremental encoder	Pin3 (DTest1_A); Pin 4 (DTest2_B); Pin 6 (Mode_Index) 2x1024 ppr (12-bit) 2x256 ppr low-jitter (10-bit)	Not used Pin 3: not used Pin 4:not used
Pin 6	MODE_Index pin selects fast or slow mode in the default configuration. In case of incremental mode, the fast mode is selected and the pin is configured as output.	MODE_Index pin selects fast or slow mode in the default configuration.
Pin 12	PWM output: frequency selectable by OTP: 1µs / step, 4096 steps per revolution, f=244Hz 2µs/ step, 4096 steps per revolution, f=122Hz	PWM output: frequency selectable by OTP: 1µs / step, 4096 steps per revolution, f=244Hz 2µs/ step, 4096 steps per revolution, f=122Hz
Sampling frequency	selectable by MODE input pin: 2.5kHz, 10,4kHz	selectable by MODE input pin: 2.5kHz, 10,4kHz
Propagation delay	384µs (slow mode)	384µs (slow mode)
	96µs (fast mode)	96µs (fast mode)
Transition noise (rms; 1sigma)	0.03 degrees maximum (slow mode)	0.03 degrees maximum (slow mode)
	0.06 degrees maximum (fast mode)	0.06 degrees maximum (fast mode)
OTP programming options	PPTRIM; programming voltage 3.3V – 3.6V <70ºC; 3.5V – 3.6V >70ºC; 52-bit serial data protocol; CSn, PDIO and CLK	EasyZap; programming voltage 7.3V – 7.5V; Csn; Prog and CLK; 16-bit (32-bit) serial data protocol;

10 Package Drawings and Markings

The device is available in a QFN 32 (7mm x 7mm) package.
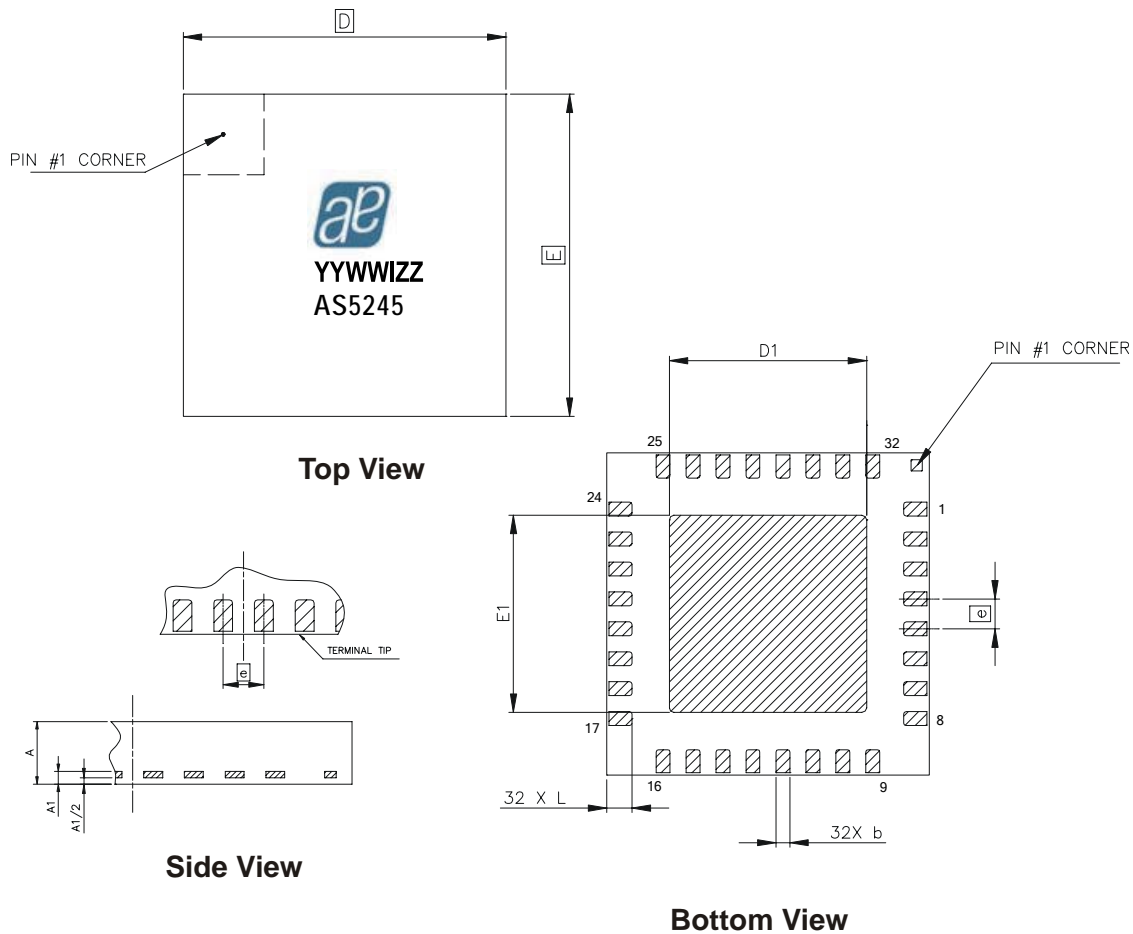
Figure 19. Package Drawings

Top View

Side View

Bottom View

Table 15. Package Dimensions

Symbol	mm			inch		
	Min	Typ	Max	Min	Typ	Max
D	7 BSC			0.28 BSC		
E	7 BSC			0.28 BSC		
D1	4.18	4.28	4.38	0.165	0.169	0.172
E1	4.18	4.28	4.38	0.165	0.169	0.172
L	0.45	0.55	0.65	0.018	0.022	0.026
b	0.25	0.30	0.35	0.010	0.012	0.014
e	0.65 BSC					
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.203 REF			0.008 REF		

Revision History

Revision	Date	Owner	Description
1.0	June 08, 2007	apg	Initial revision
	July 24, 2008		Changes made to values in Table 9 - Incremental Resolution
	Feb 13, 2009		Updated min, typ, max values for $t_{DOvalid}$ parameter in Table 5 - Timing Characteristics
	July 15, 2009	rfu	1) Note added under Table 6 - Slow and Fast Mode Parameters 2) Output Md0, Md1 description updated, (see User Selectable Settings on page 18)

	July 22, 2009	mub	Updated values in Table 5 - Timing Characteristics for the following parameters:
			  - $t_{DOvalid}$
			  - f_{PWM}
			  - PW_{MIN}
			  - PW_{MAX}

	July 23, 2009		Updated sections Electrical Characteristics on page 6, Timing Characteristics on page 9 and Detailed Description on page 10 according to AS5145 datasheet.
1.1	Oct 19, 2009	apg	Deleted the following -- 1) 'OTP Programming Connection' figure 2) Physical Placement of the magnet, Magnet Placement, Simulation Modeling
1.2	Nov 05, 2009		Timing Characteristics (page 9) - Deleted the parameter 'PWM Frequency' (f_{PWM})
1.3	Dec 04, 2009		Updated section Internal Timing Tolerance (page 26)
1.4	Apr 01, 2010		Updated standards in Absolute Maximum Ratings on page 5
	Apr 13, 2010		Updated Package Drawings and Markings on page 28
1.5	Jun 17, 2010	mub	Updated Mode_Index, PWM, Electrical Characteristics (page 6), fPWM (page 9), Figure 9, Table 11. Info on 'Magnet Input Specification' deleted from the document.

Note: Typos may not be explicitly mentioned under revision history.

11 Ordering Information

The devices are available as the standard products shown in Table 16.

Table 16. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5245HQFT	12-bit fully redundant magnetic rotary encoder	Tape & Reel	QFN 32 (7mm x 7mm)

Note: All products are RoHS compliant and Pb-free.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

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