AS5055

Data Sheet

Low Power 12 Bit Magnetic Rotary Encoder

1 General Description

The AS5055 is a single-chip magnetic rotary encoder IC with low voltage and low power features.

It includes 4 integrated Hall elements, a high resolution ADC and a smart power management controller.

The angle position, alarm bits and magnetic field information are transmitted over a standard 3-wire or 4-wire SPI interface to the host processor.

The AS5055 is available in a small QFN 16-pin 4x4x0.85mm package and specified over an operating temperature of -20 to +85℃.

2 Benefits

- Complete system-on-chip
- Low power consumption
- Low operating voltage
- Easy to use SPI interface

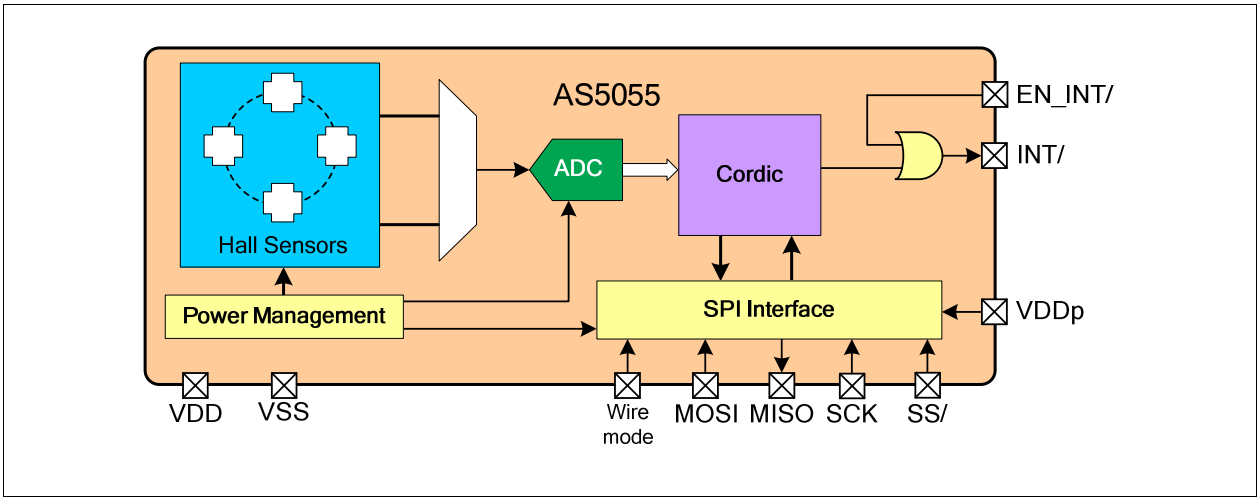
3 Key Features

- 12 bit resolution
- Standard SPI interface, 3 or 4 wire
- 3.0 to 3.6V core voltage, 1.8 to 3.6V peripheral supply voltage
- Automatic wakeup over SPI interface
- Interrupt output for conversion complete indication
- Low power mode:
  < 8mA (avg) @ 620us readout interval
  < 5mA (avg) @ 1ms readout interval
  < 500µA (avg) @ 10ms readout interval
  < 53µA (avg) @ 100ms readout interval
- Small size QFN-16 4x4x0.85mm

4 Applications

- Servo motor control
- Input device for battery operated portable devices
- Robotics

Figure 1. Block Diagram

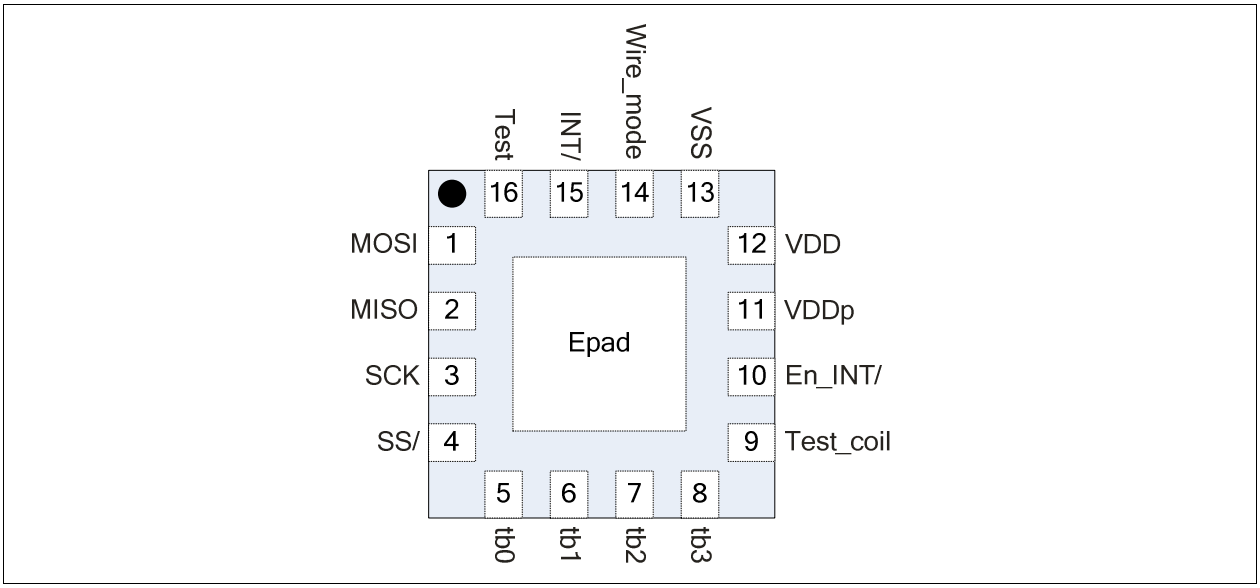


5 Table of Contents

6 Pinout

6.1 Pin Assignments

Figure 2. QFN-16 Package and Pinout (TOP View)



6.2 Pin Descriptions

Table 1. Pin Descriptions

Pin#	Symbol	Type	Description
1	MOSI	DI	SPI bus data input
2	MISO	DO	SPI bus data output
3	SCK	DI ST	SPI Clock Schmitt trigger
4	SS/	DI	SPI Slave Select, active LOW
5	tb0	AIO	Test pin, leave unconnected
6	tb1	AIO	Test pin, leave unconnected
7	tb2	AIO	Test pin, leave unconnected
8	tb3	AIO	Test pin, leave unconnected
9	Test coil	S	Test pin, connect to VSS
10	En_INT/	DI	Enable / disable Interrupt
11	VDDp	S	Peripheral power supply, 1.8V ~ VDD
12	VDD	S	Analog and digital power supply, 3.0 ~ 3.6V
13	VSS	S	Supply ground
14	Wire_mode	DIO	0 = 3-wire mode, 1 = 4-wire mode
15	INT/	DO	Interrupt output. Active LOW, when conversion is finished
16	Test	DIO	Test pin, leave unconnected
Epad	-	-	Center pad not connected

PIN Types:

DI	...	Digital input	DIO	...	Digital I/O
DI ST	...	Digital input Schmitt trigger	AIO	...	Analog I/O
DO	...	Digital output, tri-state buffer	S	...	Supply

7 General Specifications

7.1 Absolute Maximum Ratings (Non operating)

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage	VDD	-0.3	5.0	V	(1)
Peripheral supply voltage	VDDp	-0.3	VDD+0.3	V	
Input pin voltage	V_{in}	-0.3	5.0	V	
Input current (latchup immunity)	I_{scr}	-100	100	mA	Norm: Jedec 78
Electrostatic discharge	ESD	+/-1	-	kV	Norm: MIL 883 E method 3015
Package thermal resistance	Theta_JA	-	33.5	℃/W	Vel ocity=0, Multi Layer PCB; Jedec Standard Testboard
Total power dissipation	P_t		36	mW	
Storage temperature	T_{strg}	-55	125	℃	
Package body temperature	T_{body}		260	℃	Norm: IPC/JEDEC J-STD-020C (2) (3)
Humidity non-condensing		5	85	%	
Moisture Sensitive Level	MSL	3			Represents a max. floor life time of 168h

Notes:

(1) Value of these process dependent parameters to be taken from according Process Parameter document, current version

(2) The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.

(3) The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)

7.2 Operating Conditions

Table 3. Operating Conditions

Parameter	Conditions	Min	Max	Units
DC supply voltage	VDD	3.0	3.6	V
Peripheral supply voltage (1)	VDDp	1.8	VDD	V
Input pin voltage	V_{in}	-0.3	VDDp +0.3	V
Ambient operating temperature		-20	85	℃
External component	Power supply filter, pin VDD (2)	2.2	4.7	µF
		15	33	Ω
	Ceramic capacitor, pin VDDp to VSS	100		nF

Notes:

(1) VDDp must not exceed VDD (protection diode between VDDp and VDD)

(2) see 9.2

7.3 System Parameters

Table 4. System Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating current	I_10			0.5	mA	Average current @ 10 ms readout rate (1)
Operating current	I_100			53	µA	Average current @ 100 ms readout rate
Operating current	I_max			8.5	mA	Max readout rate
Readout rate		320		430	µs	Time between READ ANGLE command and INTERRUPT
Power down current				3	µA	Power down current
Lateral displacement range	Rd	-		+/- 0.5	mm	(2)
Magnetic field strength	B_Z	30	-	80	mT	
Serial interface	SPI mode 0 (CPOL = 0 / CPHA =0)					
Resolution; magnetic field measurement			12		bit	
Resolution; angle			12		bit	Programming version
INL		-1.41		1.41	degree	(3)
IC package		QFN 4x4x0.85				

Notes:

(1) Without the time for the SPI interface

(2) Centre of the magnet to the centre of the die

(3) Best-fit line - over supply, displacement and temperature – but without quantization

7.4 DC/AC Characteristics

Digital pads: MISO, MOSI, SCK, SS/, EN_INT/, INT/, Wire_mode

Table 5. DC/AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
High level input voltage	V_{IH}	0.7 * VDDp			V	
Low level input voltage	V_{IL}			0.3 * VDDp	V	VDDp > 2.7V
Low level input voltage	V_{IL}			0.25 * VDDp	V	VDDp < 2.7V
Input leakage current	I_{LEAK}			1	µA	
High level output voltage	V_{OH}	VDDp - 0.5			V	
Low level output voltage	V_{OL}			VSS + 0.4	V	
Capacitive load	C_L			35	pF	

8 User Programming

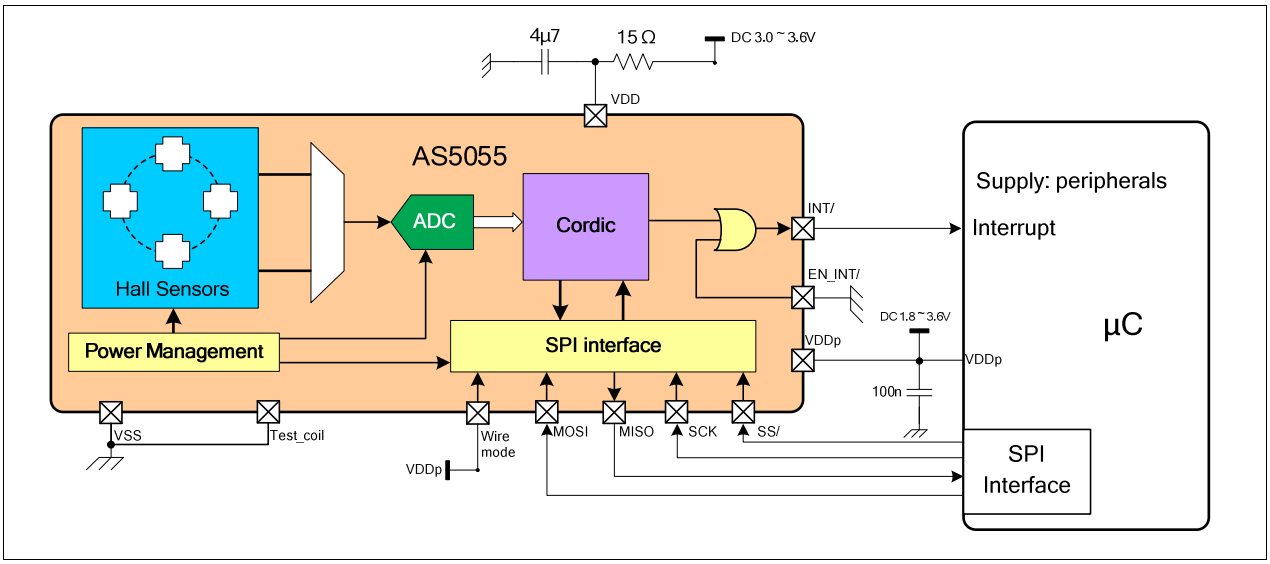
The AS5055 does not require any programming by the user. A dedicated on-chip zero position programming is not implemented. If a zero position programming is required, it is recommended to store the zero position offset in the host controller.

9 Operation Modes

9.1 Typical Application

The AS5055 requires only a few external components in order to operate immediately when connected to the host microcontroller. Only 6 wires are needed for a simple application using a single power supply: two wires for power and four wires for the SPI communication. A seventh connection can be added in order to send an interrupt to the host CPU to inform that a new valid angle can be read.

Figure 3. Typical Application Using SPI 4-Wire Mode and INT/ Output



Upon power-up, the AS5055 performs a full power-up sequence including one angle measurement. The completion of this cycle is indicated at the INT/ output pin and the angle value is stored in an internal register. Once this output is set, the AS5055 suspends to sleep mode.

9.2 Power Supply Filter

Due to the sequential internal sampling of the Hall sensors, fluctuations on the analog power supply (pin#12: VDD) may cause additional jitter of the measured angle. This jitter can be avoided by providing a stable VDD supply. The easiest way to achieve that is to add a RC filter: 15Ω + 4.7µF in the power supply line as shown in *Figure 3*.

Alternatively, a filter: 33Ω + 2.2µF may be used. However with this configuration, the minimum supply voltage is 3.15V.

9.3 Reading an Angle

The external microcontroller can respond to the INT request by reading the angle value from the AS5055 over the SPI interface. Once the angle value is read, the INT output is cleared again.

Sending a “read angle” command by the SPI interface also automatically powers up the chip and starts another angle measurement. As soon ad the microcontroller has completed reading of the angle value, the INT output is cleared and a new result is stored in the angle register. The completion of the angle measurement is again indicated by setting the INT output and a corresponding flag in the status register.

9.3.1 Reducing the Angle Jitter

Due to the measurement principle of the chip, only a single angle measurement is performed in very short time (~600µs) after each power-up sequence. As soon as the measurement of one angle is completed, the chip suspends to power-down state. An on-chip filtering of the angle value by digital averaging is not implemented, as this would require more than one angle measurement and consequently, a longer power- up time which is not desired in low-power applications.

The angle jitter can be reduced by averaging of several angle samples in the external microcontroller. For example, an averaging of 4 samples reduces the jitter by 6dB (50%).

9.4 Low Power Mode

After completing the readout of an angle value, the device is in very low power condition. The AS5055 remains in sleep mode until it receives another angle reading request over the SPI interface. The average power consumption therefore depends on the interval, at which the external controller reads an angle over the SPI Interface. The timing ratio between active and sleep phase:

$$I_{avg} = \frac{t_{on} * I_{on} + t_{off} * I_{off}}{t_{on} + t_{off}}$$

For:	ton =	Minimum on-time for power-up and angle measurement	600µs
	toff =	Pause interval between measurements, determined by the polling rate of the external microcontroller	
	Ion =	Current consumption in active mode	8mA avg.
	Ioff =	Current consumption in sleep mode	3µA

Examples:

3000 measurements per second (continuous mode)	I = 8mA
1000 measurements per second	Iavg = 5mA
100 measurements per second	Iavg = 500µA
10 measurements per second	Iavg = 53µA

Note that even in low power mode, the power supply must be capable of supporting the active current at least for the time Ton, until the AS5055 is suspended to sleep mode.

9.5 Interrupt Chaining

Every chip contains a configurable gate to combine its own internally generated interrupt signal with a signal applied externally over the XENINT-pin. The INT-mode register is preset via an OTP register can be overwritten by the SPI interface.

Case A

Device A is set to mode 0

Device B is set to mode 0

The micro controller recognizes an interrupt if both devices signalize that the computation is finished.

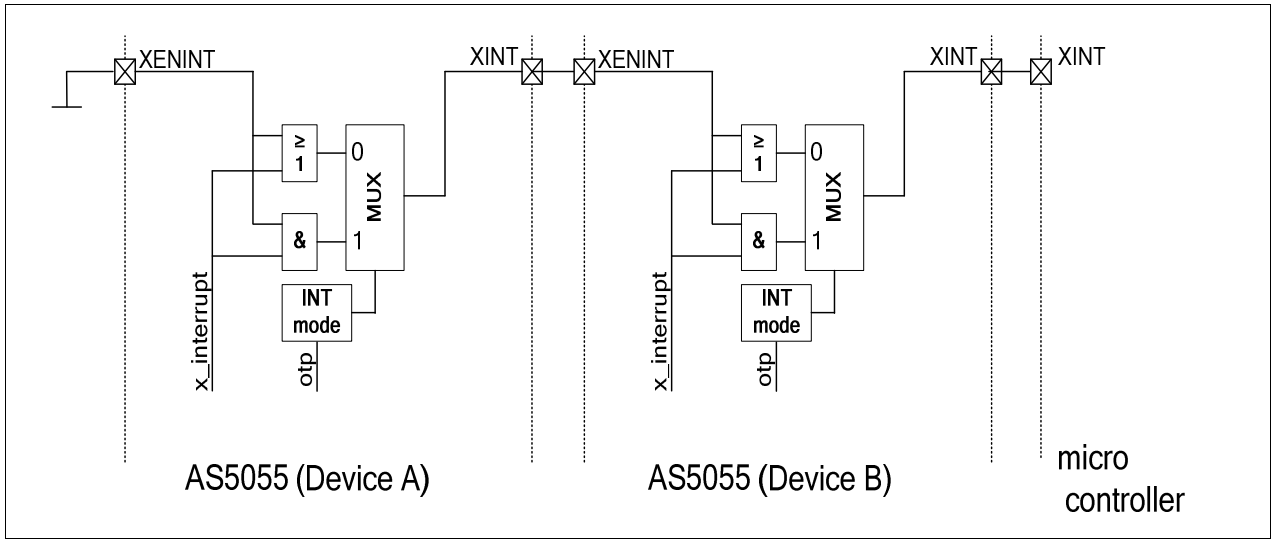
Case B

Device A is set to mode 0

Device B is set to mode 1

The micro controller recognizes an interrupt if one of the two devices signalize that the computation is finished.

Figure 4. Interrupt Chain



10 SPI Communication

The transmitted data consists of 14 bit data, an *Error-Flag* and a *Parity* bit. When writing data to the chip, the *Error-Flag* is not applicable. The *Parity* is generated from the upper 15 bit and forms an even parity over the whole frame. The *Error-Flag* indicates that a failure occurred in a previous transmission.

10.1 Command Package

Every command sent to the AS5055 is represented with the following layout.

Command Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	RWn	Address<13:0>														PAR
Bit Definition & Description																
RWn		Indicates read or write command														
Address		14 bit address code														
PAR		Parity bit (EVEN)														

10.2 Read Package (Value Read from AS5055)

The read frame always contains two alarm bits, the error and parity flags and the addressed data of the previous read command.

Read Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	Data <13:0>														EF	PAR
Bit Definition & Description																
Data		14 bit addressed data														
EF		Error flag indicating a transmission error in a previous host transmission														
PAR		Parity bit (EVEN)														

10.3 Write Data Package (Value Written to AS5055)

The write frame is compatible to the read frame and contains two additional bits, the don't care and parity flag.

If the previous command was a write command a second package has to be transmitted.

Data Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	Data <13:0>														Don't care	PAR
Bit Definition & Description																
Data		14 bit data to write to former selected address														
PAR		Parity bit (EVEN)														

10.4 Register Block

Register	Bits	Mode		Reset Value	Bit	Description
Power ON Reset (POR) Register - [0x3F22]						
POR_OFF	8	r/w		0x00	<7:0>	The POR cell is deactivated when the value 0x5A is written to this register (30µA reduction of current consumption)
Software Reset Register - [0x3C00]						
software_reset	14	w		0x0	<13:0>	See to the description of the software reset
Clear Error Flag Register - [0x3380]						
clr_error_flag	14	r		0x0	<13:0>	See to the description of the clear error flag command
No Operation Register - [0x0000]						
NOP	14	w		0x0	<13:0>	See to the description of the no operation command
Automatic Gain Control (AGC) Register - [0x03FF8]						
AGC	6	r/w		0x20	<5:0>	Automatic gain control: low values = strong magnetic field high values = weak magnetic field
Angular Data - [0x3FFF]						
Angle Value	12	r		0x000	<11:0>	Measured angular value, 12 bit
Alarm LO	1	r		0	<12>	Alarm bit indicating a too low magnetic field, active HIGH (1)
Alarm HI	1	r		0	<13>	Alarm bit indicating a too high magnetic field, active HIGH (1)
System Configuration Register 1 - [0x3F20]						
resolution	2	r		'00'	<13:12>	'00' indicates 12 bit resolution
chip ID	3	r		'001'	<11:9>	Silicon version 001
invert_spinning	1	r/w		0	<8>	Invert the channel voltage
FE_bw_setting	2	r/w		'00'	<6:5>	FE BW setting
FE_gain_setting	2	r/w		'00'	<4:3>	FE gain setting
break_AGC_loop	1	r/w		0	<2>	Breaks the automatic gain control loop to use the AGC registers in a static mode
break_offset_loop	1	r/w		0	<1>	Breaks the offset compensation loop to use the offset registers in a static mode
interrupt_mode	1	r/w		0	<0>	Interrupt gate mode 0 = mode 0 1 = mode1

Note:

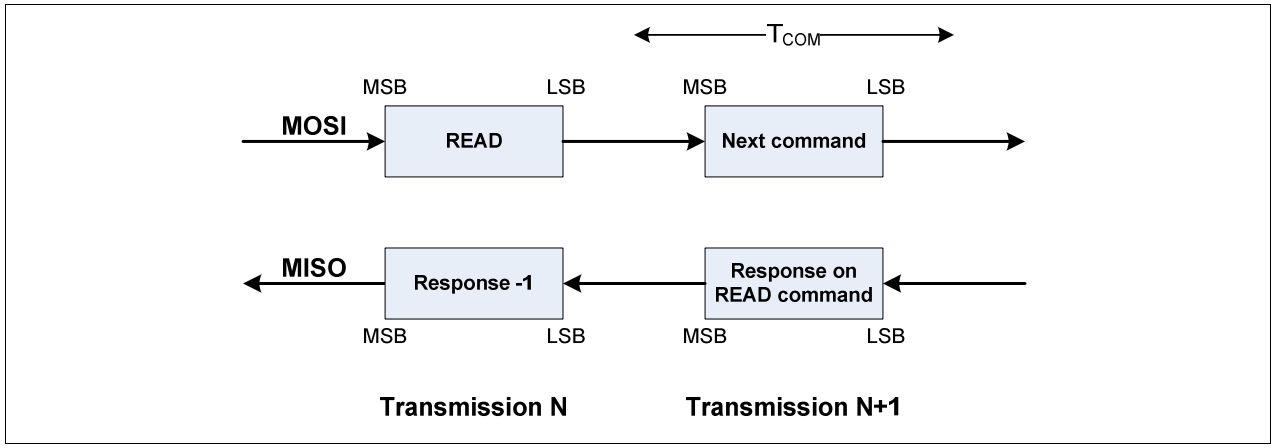
(1) Both bits High: Alarm LO = Alarm Hi = 1 indicate a major system error (DAC overflow, CORDIC overflow or Hall current error)

10.5 SPI Interface Commands

10.5.1 READ Command

For a single *READ* command two transmission sequences are necessary. The first package written to the AS5055 contains the *READ* command **(MSB high)** and the address the chip has to access, the second package transmitted to the AS5055 device can be *any command* the chip has to process next. The content of the desired register is available in the *MISO* register of the *master device* at the end of the second transmission cycle.

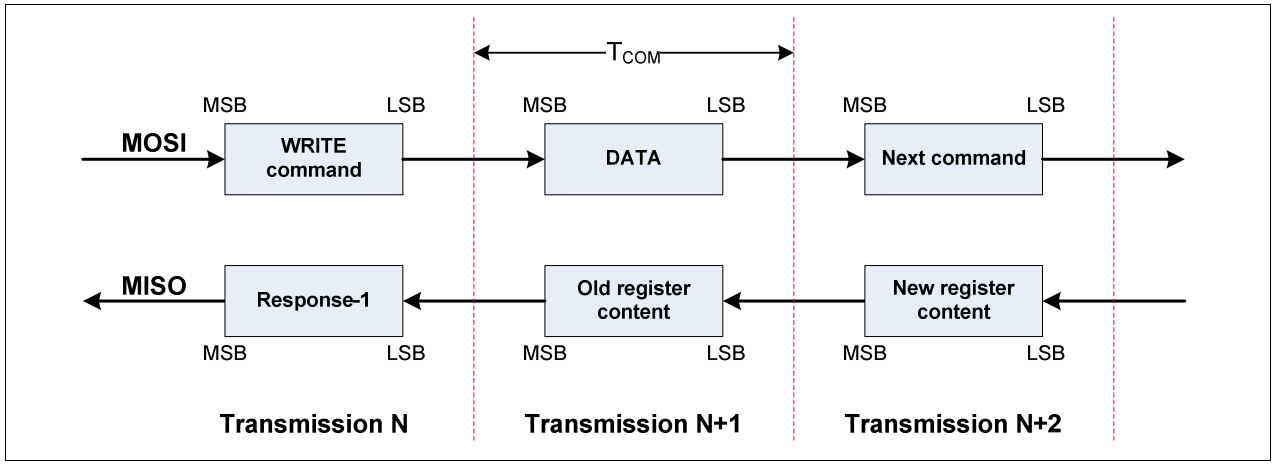
Figure 5. READ Command



10.5.2 WRITE Command

A single *WRITE* command takes two transmission cycles. With a NOP command after the WRITE command you can verify the sent data with three transmission cycles because the data will be send back during the NOP command.

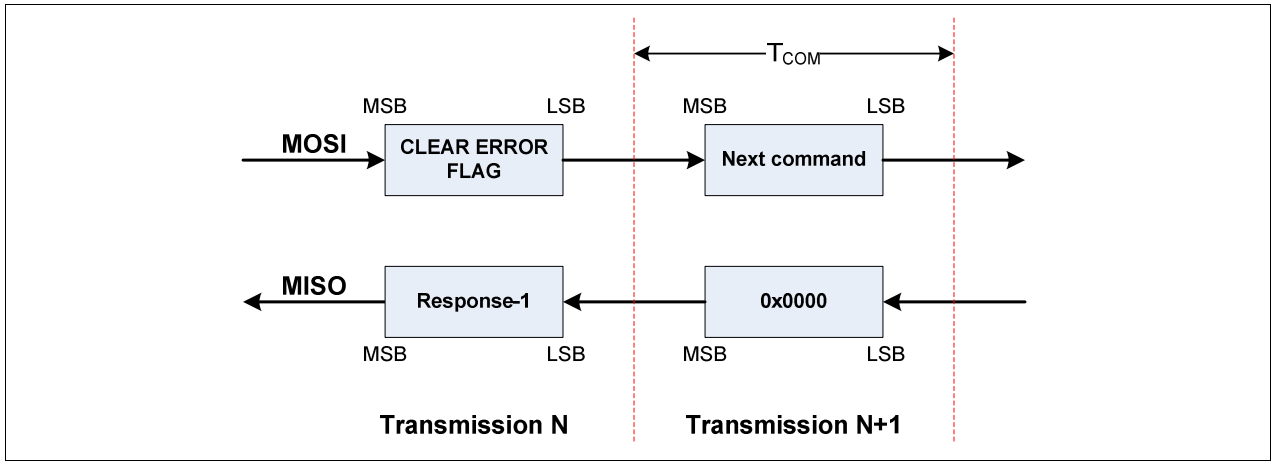
Figure 6. WRITE Command



10.5.3 CLEAR ERROR FLAG Command

The *CLEAR ERROR FLAG* command is implemented as *READ* command. This command clears the *ERROR FLAG* which is contained in every *READ* frame. The *READ* data are 0x0000, which indicates a successful clear command.

Figure 7. CLEAR ERROR FLAG Command



The package necessary to perform a *CLEAR ERROR FLAG* is built up as follows.

CLEAR ERROR FLAG Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	PAR
	CLEAR ERROR FLAG command															PAR

Possible conditions which force the ERROR FLAG to be set:

- wrong parity
- wrong command
- wrong number of clocks (no full transmission cycle or too many clocks)

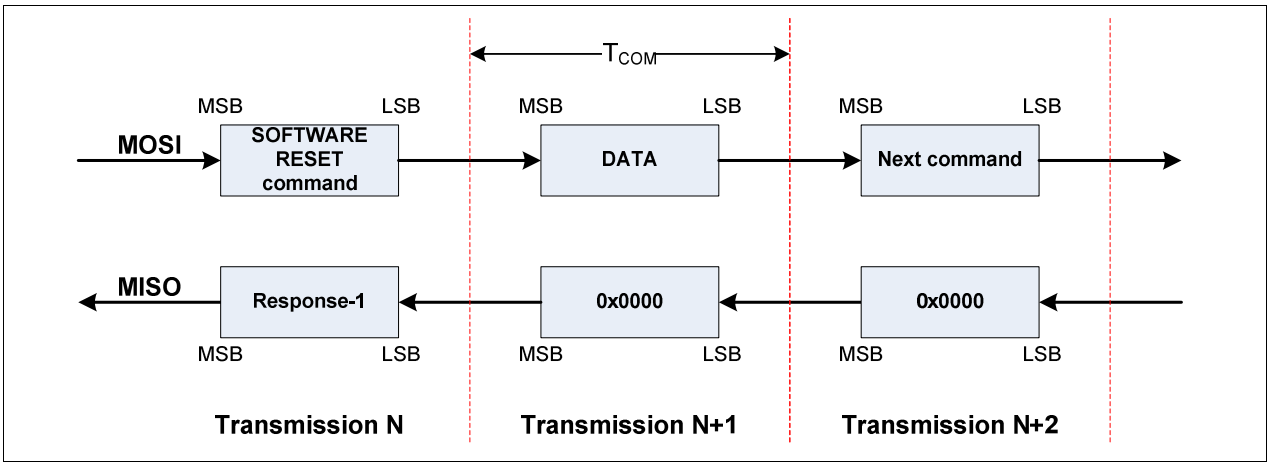
Note: If the error flag is set to high because of a communication problem the flag remains set until it will be cleared by an external command.

10.5.4 SOFTWARE RESET Command

The *SOFTWARE RESET* command is implemented as *WRITE* command. The bit 'RES SPI' of the DATA package indicates if the SPI registers should be reset as well. The soft reset resets the digital part ('RES SPI' is set to one) as well as the PPTRIM. A new PPTRIM auto-load is initiated and the reset values stored in the PPTRIM are loaded into the configuration registers. The command following the *SOFTWARE RESET* command can be *any of the commands* specified in this chapter.

After the data package is sent, the soft reset is generated. The fuses of the PPTRIM are loaded into the registers and a new conversion cycle will be started. If the device is in sleep mode the oscillator will be started first.

Figure 8. SOFTWARE RESET Command



In order to invoke a software reset on the AS5055 the following bit pattern has to be sent.

SOFTWARE RESET Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	PAR
	SOFTWARE RESET command															PAR

Data Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	Don't care													RES SPI	Don't care	PAR
Bit Definition & Description																
RES SPI	If set to one, SPI registers are reset as well (1)															
PAR	Parity bit (EVEN)															

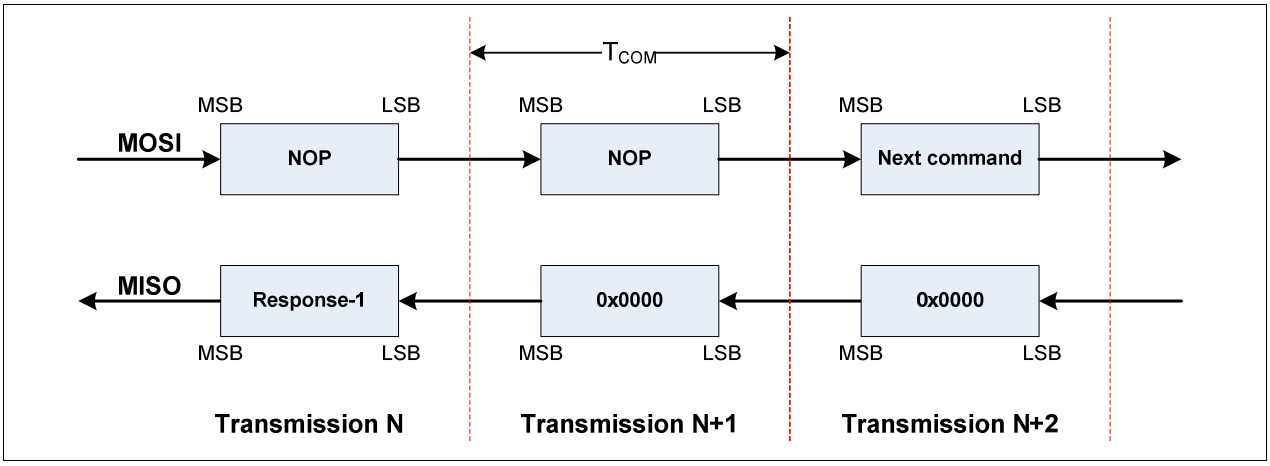
Note:

(1) After a power on reset the OTP will be read and hence otp-related registers are changed independent on the RES SPI flag

10.5.5 NOP Command

The *NOP* command represents a dummy write to the AS5055.

Figure 9. NOP Command



The NOP command frame looks like follows.

NOP Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	NOP command (0x0000)															

The chip's response on this command is 0x0000 – if no error happens.

11 SPI Interface

The 16 bit SPI Interface enables read / write access to the register blocks and is compatible to a standard micro controller interface. The SPI module is active as soon as /SS pin is pulled low. The AS5055 then reads the digital value on the MOSI (master out slave in) input with every falling edge of SCK and writes on its MISO (master in slave out) output with the rising edge. After 16 clock cycles /SS has to be set back to a high status in order to reset some parts of the interface core.

The SPI Interface can be set into two different modes - 3-wire mode or 4-wire mode.

Note: The wire mode selection is read in during the POWER-UP state and can be changed with a power on reset or a software reset command.

The SPI Interface can be set into two different modes - 3-wire mode or 4-wire mode.

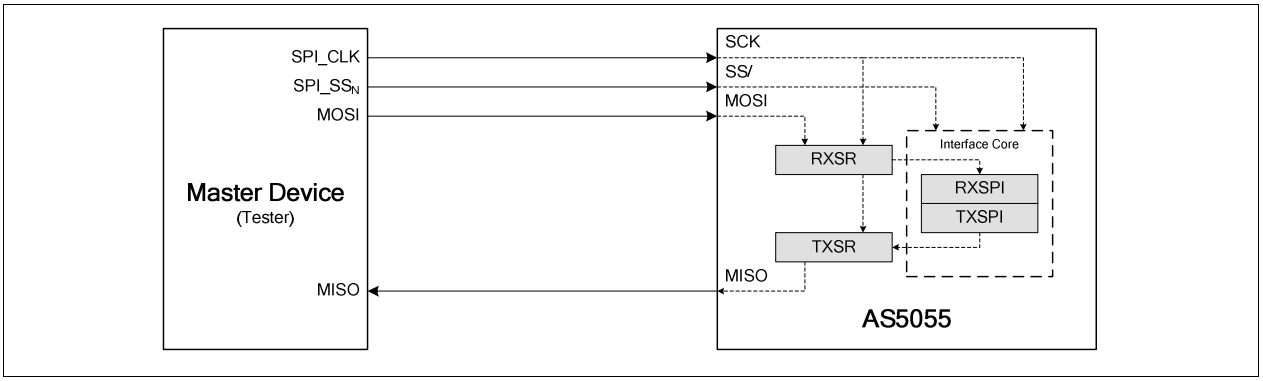
Table 6. Wire Mode Selection

Wire Mode Selection (pad 14)	
wire_mode = LO	3-wire mode
wire_mode = HI	4-wire mode

11.1 SPI Interface Signals (4-Wire Mode, Wire_mode = 1)

The AS5055 only supports slave operation mode. Therefore SCK for the communication as well as the /SS signal has to be provided by the test equipment. The following picture shows a basic interconnection diagram with one master and an AS5055 device and a principle schematic of the interface core.

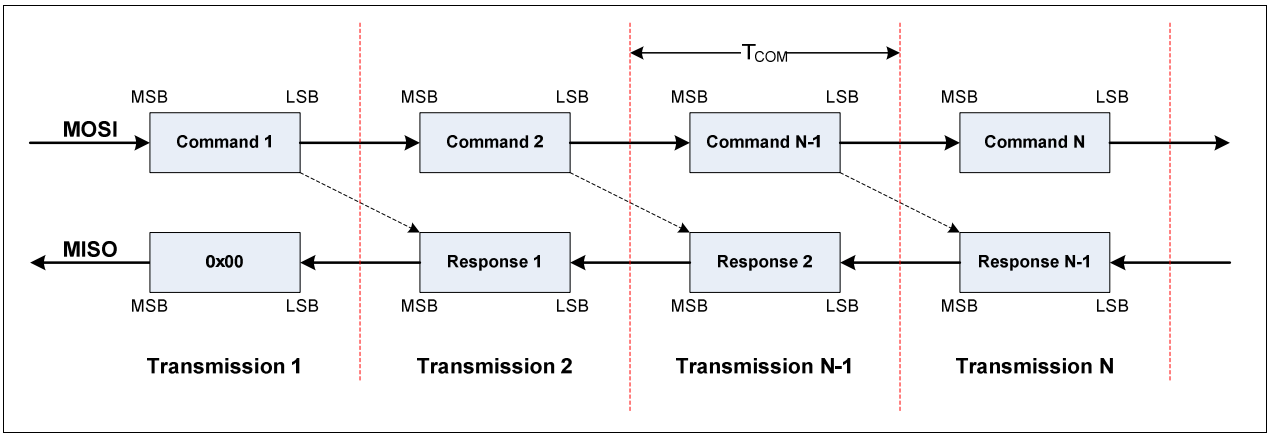
Figure 10.SPI Interface Connection



Because the interface has to decode the sent command before it can react and provide data the response of the chip to a specific command applied at a time T can be accessed in the next transmission cycle ending at T + TCOM.

The data are sent and read with **MSB first**. Every time the chip is accessed it is sending and receiving data.

Figure 11. SPI Command/Response Data Flow



11.2 SPI Timing

Figure 12. SPI Timing Diagram

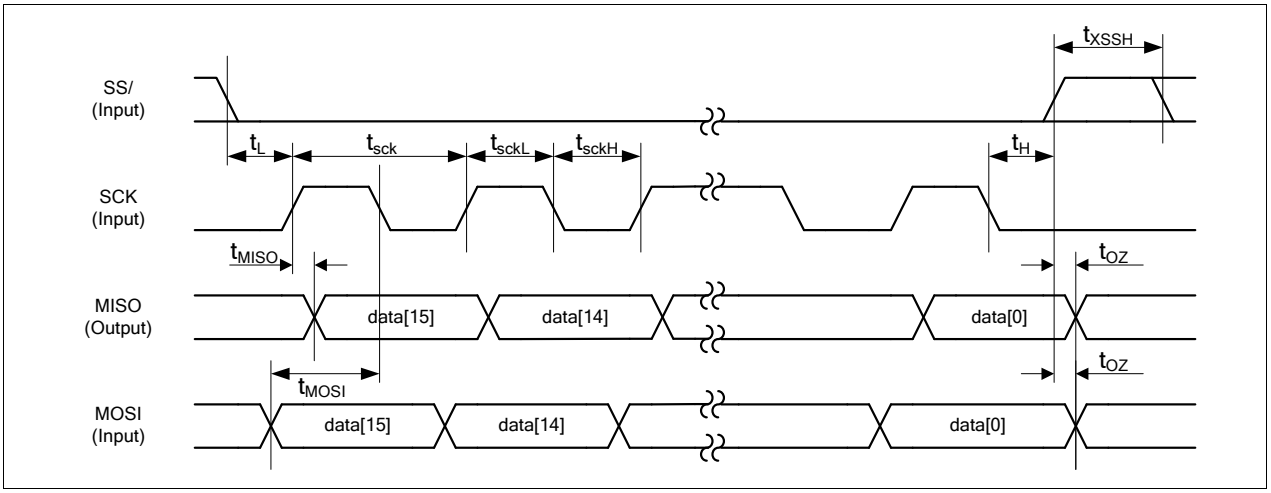


Table 7. SPI Timing Characteristics

Parameter	Description	Min	Max	Unit
t_L	Time between SS/ falling edge and SCK rising edge	10 (2)		ns
t_L	Time between SS/ falling edge and SCK rising edge	350 (1)		ns
t_{SCK}	Serial clock period	100		ns
t_{SCKL}	Low period of serial clock	50		ns
t_{SCKH}	High period of serial clock	50		ns
t_H	Time between last falling edge of SCK and rising edge of SS/	t_{SCK} / 2		ns
t_{XSSH}	High time of SS/ between two transmissions	10 (2)		ns
t_{XSSH}	High time of SS/ between two transmissions	350 (1)		ns
t_{MOSI}	Data input valid to clock edge	20		ns
t_{MISO}	SCK edge to data output valid		20	ns

Notes:

(1) Synchronization with the internal clock → 2 * t_{CLK_SYS} + 10 ns (e.g. at 8 MHz → 253 ns)

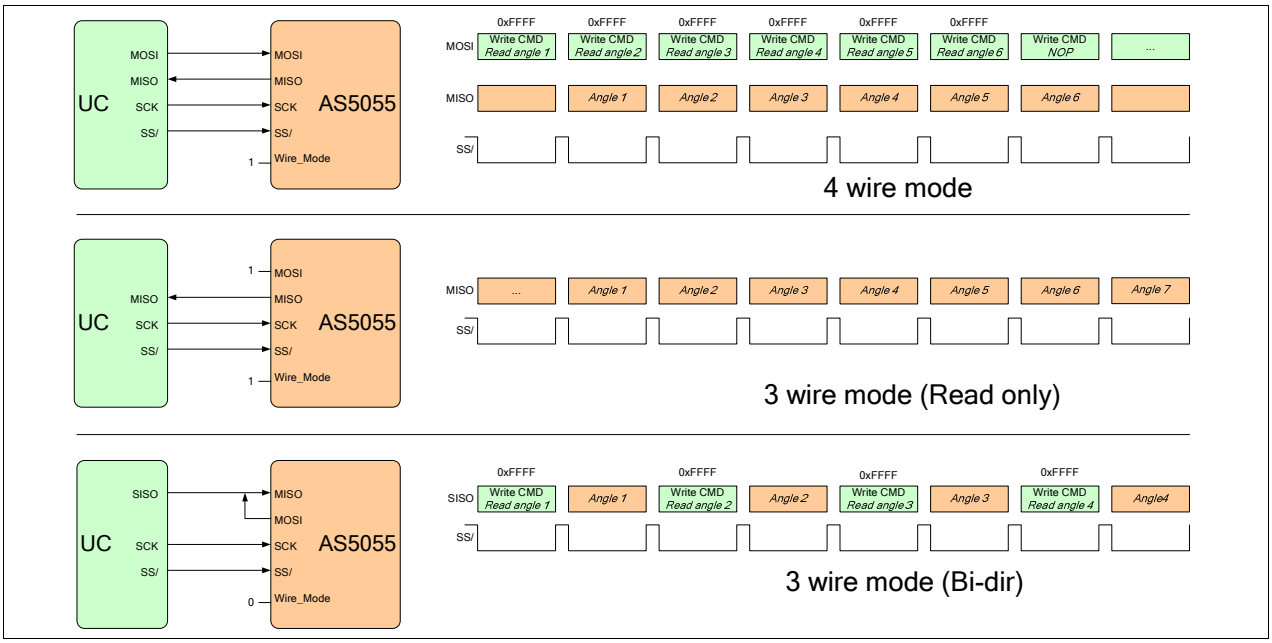
(2) No synchronization needed because the internal clock is inactive

(3) 2 internal system clock cycles (e.g. at 8 MHz → 250 ns)

11.3 SPI Connection to the Host UC

11.3.1 Single Slave Mode

Figure 13. Single Slave Mode



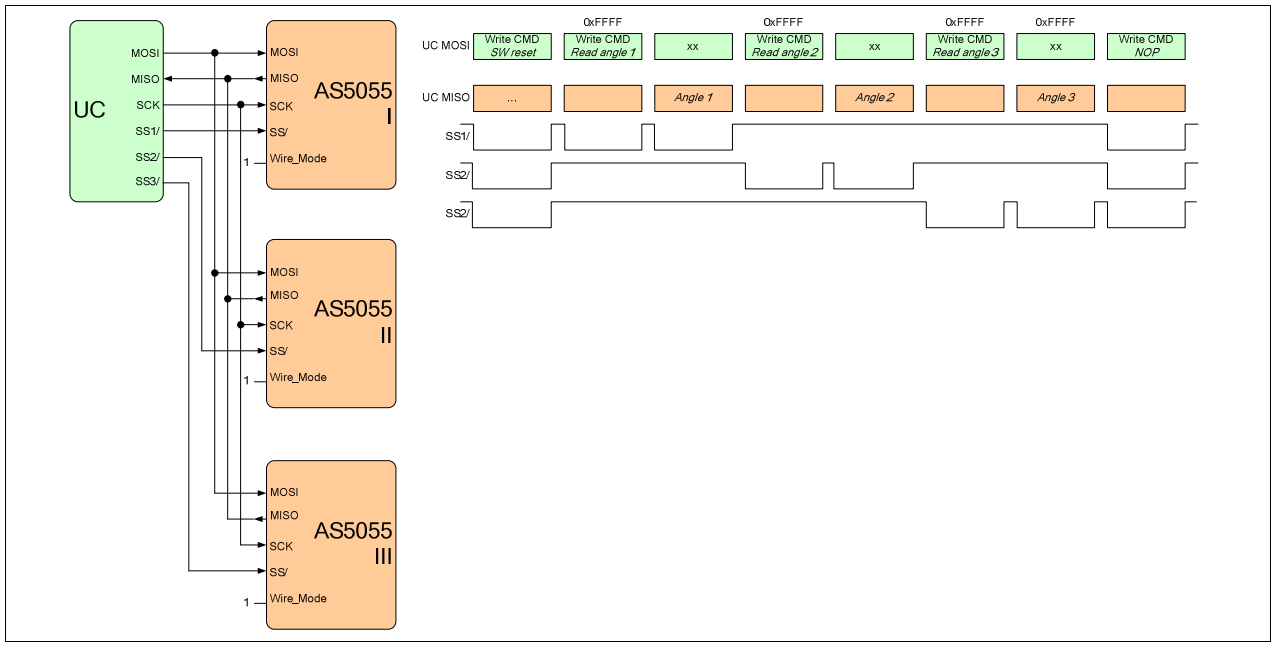
Note:

3 Wire Mode (read only):

If the ERROR FLAG is set the device must be externally reset.

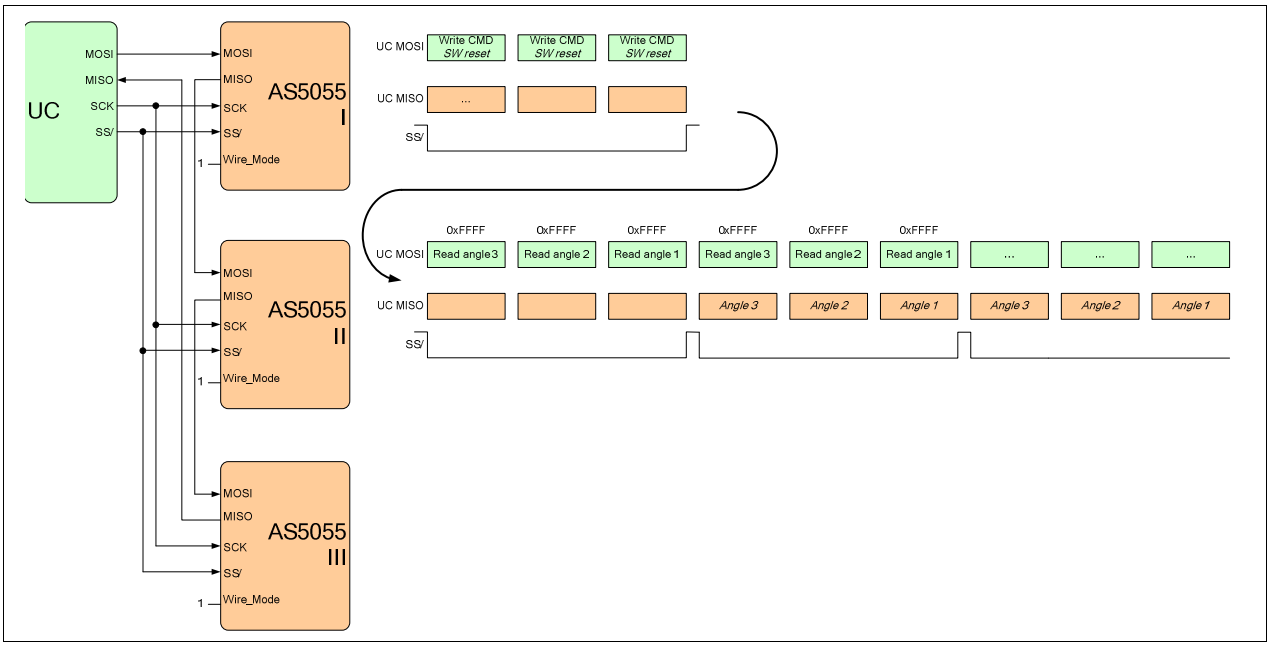
11.3.2 Multiple Slave, n+3 Wire (Separate ChipSelect)

Figure 14. Multiple Slave, n+3 Wire (Separate ChipSelect)



11.3.3 Daisy Chain, 4 Wire

Figure 15. Daisy Chain, 4 Wire



12 Placement of the Magnet

12.1 Non-Linearity Error over Displacement

As shown in *Figure 17*, the recommended horizontal position of the magnet axis is over the diagonal center of the IC.

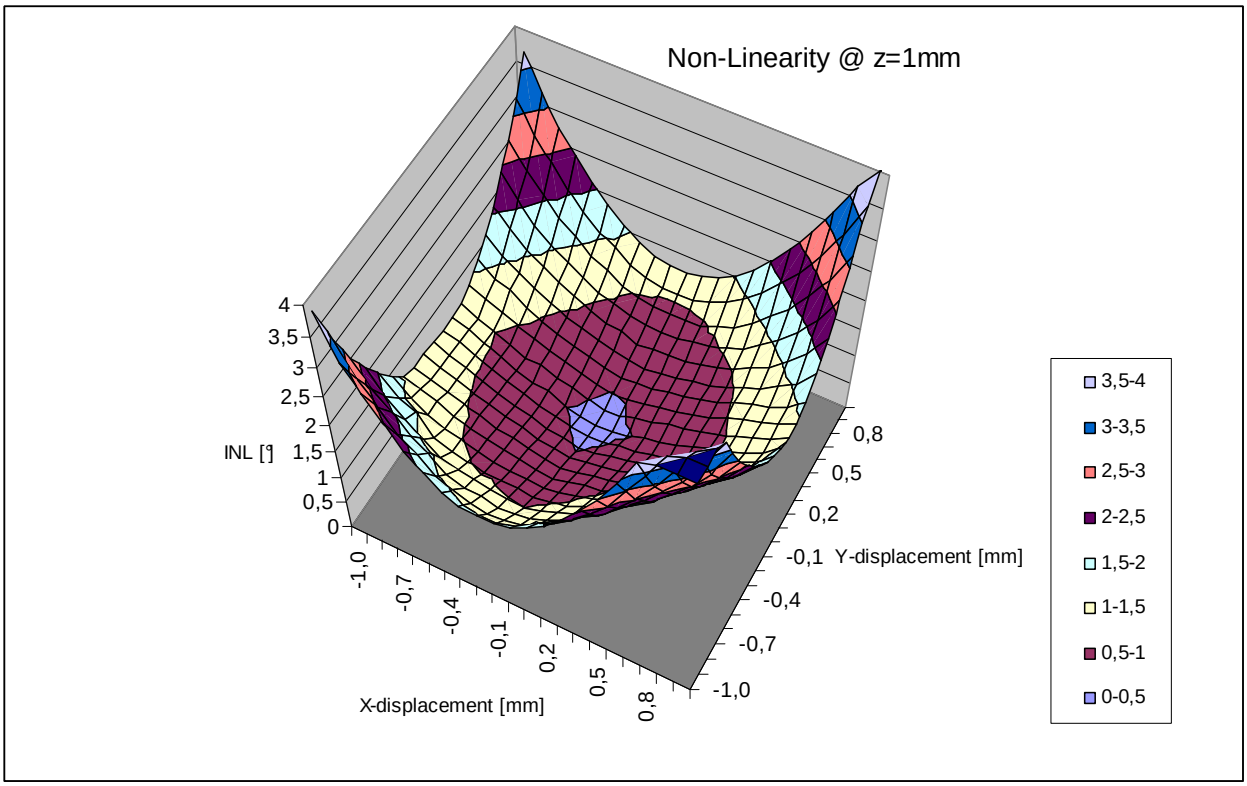
Figure 16 shows a typical error curve at a vertical magnet distance of 1.0mm, measured with a NdFeB N35H magnet with 6mm diameter and 2.5mm height.

The X- and Y- axis of the graph indicate the lateral displacement of the magnet center with respect to the IC center.

At X = Y = 0, the magnet is perfectly centered over the IC. The total displacement plotted on the graph is for ± 1mm in both directions.

The Z-axis displays the worst case INL error over a full turn at each given X-and Y- displacement. The error includes the quantization error of ± ½ LSB. At the sample shown in *Figure 16*, the accuracy for a centered magnet is better than 0.5°. Within a radius of 0.5mm, the accuracy is about 1.0° (spec = 1.41° over temperature).

Figure 16. Integral Non-Linearity over Displacement of the Magnet



13 Package Information

Figure 17. Package Drawing and Hall Sensor Locations

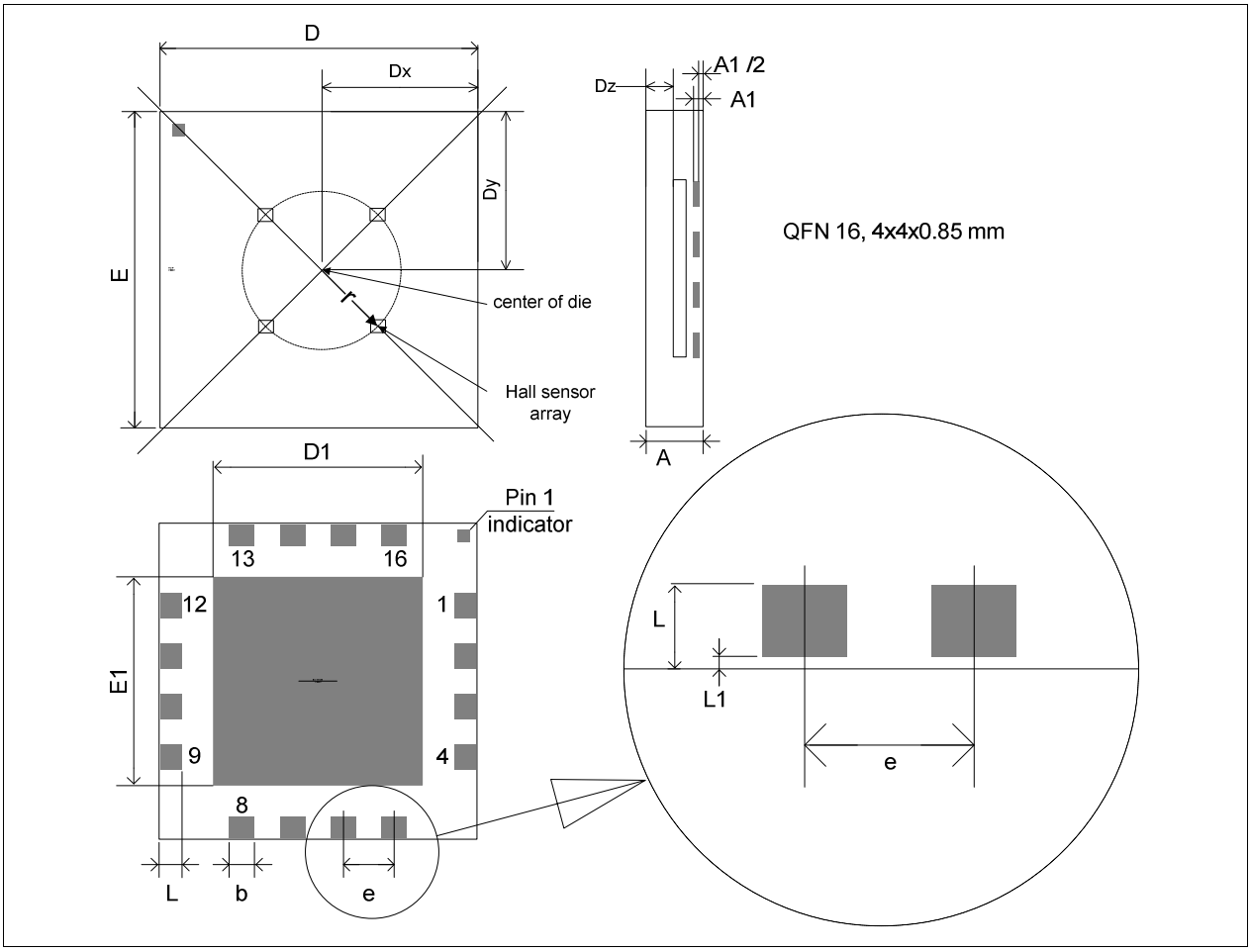


Table 8. Mechanical Dimensions

Dimension (mm)	Min	Nom	Max	Note
A	0.80	0.85	0.90	
A1	0.00		0.05	
b	0.25	0.30	0.35	
D		4.00 BSC		
E		4.00 BSC		
D1	2.50	2.60	2.70	
E1	2.50	2.60	2.70	
e	-	0.65 BSC	-	
L	0.40	0.45	0.50	
L1			0.10	
Dx	1.85	2.00	2.15	Center of die to package edge
Dy	1,85	2.00	2.15	Center of die to package edge
Dz	0.323	0.383	0.443	Surface of die to package surface
r		1.00		Radius of Hall array

13.1 Ordering Information

Table 9. Ordering Information

Model	Description	Delivery Form	Package
AS5055 EQFT	12-bit low power magnetic rotary encoder	Tape & Reel	QFN 4x4x0.85mm

Revision History

Table 10. Revision History

Revision	Date	Owner	Description
1.0	23-Mar-2010	JJA	Initial revision of public release version
1.1	08-Jun-2010	JLU	Pin description updated (pin 16), Fig. 3 updated (chapter 9.1 Typical Application), Fig. 12, 13, 14 updated (chapter 11.3 SPI Connection to the Host UC)
1.11	03-Nov-2010	AGT	Updates: Chapter 6.2 Pin Description, 7.2 Power Supply Filter, 8.4 Register Block (POR_OFF, data_log_en), 9.3 SPI Connection to the Host UC, 10.1 Absolute Maximum Ratings, 10.3 System Parameters
	08-Nov-2010	AGT	Chapter 9.5 Interrupt Chaining added; SPI mode description changed (chapter 7.3 System Parameters)

Copyrights

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or lifesustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact Information

Headquarters

austriamicrosystems AG

A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0

Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact