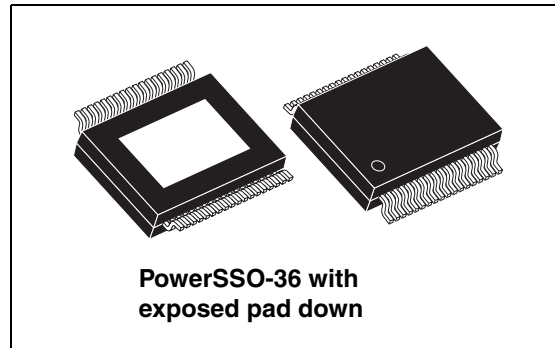


## 20 W + 20 W dual BTL class-D audio amplifier

### Features

- 20 W + 20 W continuous output power:  
 $R_L = 8 \Omega$ , THD = 10% at  $V_{CC} = 18 V$
- Wide range single supply operation (5 V - 18 V)
- High efficiency ( $\eta = 90\%$ )
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No 'pop' at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable



### Description

The TDA7491HV is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no separate heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

The TDA7491HV is pin to pin compatible with the TDA7491P and TDA7491LP.

**Table 1. Device summary**

Order code	Operating temperature	Package	Packaging
TDA7491HV	0 to 70 °C	PowerSSO-36 EPD	Tube
TDA7491HV13TR	0 to 70 °C	PowerSSO-36 EPD	Tape and reel

# Contents

<b>1</b>	<b>Device block diagram</b>	<b>7</b>
<b>2</b>	<b>Pin description</b>	<b>8</b>
2.1	Pin out	8
2.2	Pin list	9
<b>3</b>	<b>Electrical specifications</b>	<b>10</b>
3.1	Absolute maximum ratings	10
3.2	Thermal data	10
3.3	Electrical specifications	10
<b>4</b>	<b>Characterization curves</b>	<b>12</b>
4.1	With 4- $\Omega$ load at $V_{CC} = 14$ V	12
4.2	With 6- $\Omega$ load at $V_{CC} = 16$ V	17
4.3	With 8- $\Omega$ load at $V_{CC} = 18$ V	23
4.4	Test board	29
<b>5</b>	<b>Package mechanical data</b>	<b>30</b>
<b>6</b>	<b>Applications circuit</b>	<b>32</b>
<b>7</b>	<b>Application information</b>	<b>33</b>
7.1	Mode selection	33
7.2	Gain setting	34
7.3	Input resistance and capacitance	34
7.4	Internal and external clocks	35
7.4.1	Master mode (internal clock)	35
7.4.2	Slave mode (external clock)	35
7.5	Filterless modulation	36
7.6	Output low-pass filter	37
7.7	Protection function	38
7.8	Diagnostic output	38
7.9	Heatsink requirements	39

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<b>8</b>	<b>Revision history</b> .....	<b>40</b>
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## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin description list . . . . .	9
Table 3.	Absolute maximum ratings . . . . .	10
Table 4.	Thermal data . . . . .	10
Table 5.	Electrical specifications . . . . .	10
Table 6.	PowerSSO-36 EPD dimensions . . . . .	31
Table 7.	Mode settings . . . . .	33
Table 8.	Gain settings . . . . .	34
Table 9.	How to set up SYNCLK . . . . .	35
Table 10.	Document revision history . . . . .	40

## List of figures

Figure 1.	Internal block diagram (one channel only)	7
Figure 2.	Pin connection (top view, PCB view)	8
Figure 3.	Output power vs supply voltage	12
Figure 4.	THD vs output power (1 kHz)	12
Figure 5.	THD vs output power (100 Hz)	13
Figure 6.	THD vs frequency	13
Figure 7.	Frequency response	13
Figure 8.	Crosstalk vs frequency	14
Figure 9.	FFT (0 dB)	14
Figure 10.	FFT (-60 dB)	14
Figure 11.	Power supply rejection ratio vs frequency	15
Figure 12.	Power dissipation and efficiency vs output power	15
Figure 13.	Closed-loop gain vs frequency	15
Figure 14.	Current consumption vs voltage on pin MUTE	16
Figure 15.	Attenuation vs voltage on pin MUTE	16
Figure 16.	Current consumption vs voltage on pin STBY	16
Figure 17.	Attenuation vs voltage on pin STBY	17
Figure 18.	Output power vs supply voltage	17
Figure 19.	THD vs output power (1 kHz)	18
Figure 20.	THD vs output power (100 Hz)	18
Figure 21.	THD vs frequency	18
Figure 22.	Frequency response	19
Figure 23.	Crosstalk vs frequency	19
Figure 24.	FFT (0 dB)	19
Figure 25.	FFT (-60 dB)	20
Figure 26.	Power supply rejection ratio vs frequency	20
Figure 27.	Power dissipation and efficiency vs output power	20
Figure 28.	Closed-loop gain vs frequency	21
Figure 29.	Current consumption vs voltage on pin MUTE	21
Figure 30.	Attenuation vs voltage on pin MUTE	21
Figure 31.	Current consumption vs voltage on pin STBY	22
Figure 32.	Attenuation vs voltage on pin STBY	22
Figure 33.	Output power vs supply voltage	23
Figure 34.	THD vs output power (1 kHz)	23
Figure 35.	THD vs output power (100 Hz)	24
Figure 36.	THD vs frequency	24
Figure 37.	Frequency response	24
Figure 38.	Crosstalk vs frequency	25
Figure 39.	FFT (0 dB)	25
Figure 40.	FFT (-60 dB)	25
Figure 41.	Power supply rejection ratio vs frequency	26
Figure 42.	Power dissipation and efficiency vs output power	26
Figure 43.	Closed-loop gain vs frequency	26
Figure 44.	Current consumption vs voltage on pin MUTE	27
Figure 45.	Attenuation vs voltage on pin MUTE	27
Figure 46.	Current consumption vs voltage on pin STBY	27
Figure 47.	Attenuation vs voltage on pin STBY	28
Figure 48.	Test board (TDA7491HV) layout	29

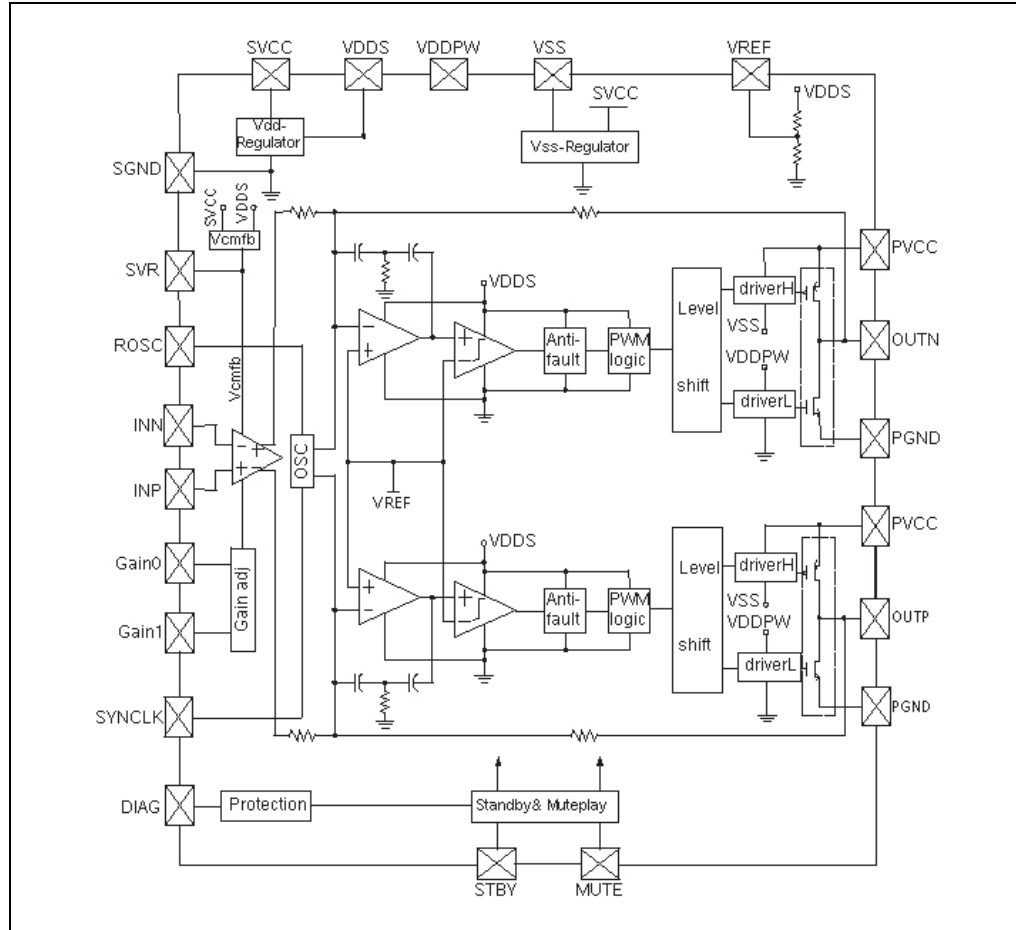
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Figure 49.	PowerSSO-36 EPD outline drawing . . . . .	30
Figure 50.	Applications circuit for class-D amplifier . . . . .	32
Figure 51.	Standby and mute circuits . . . . .	33
Figure 52.	Turn-on/off sequence for minimizing speaker "pop" . . . . .	33
Figure 53.	Device input circuit and frequency response . . . . .	34
Figure 54.	Master and slave connection . . . . .	35
Figure 55.	Unipolar PWM output . . . . .	36
Figure 56.	Typical LC filter for a 8-Ω speaker . . . . .	37
Figure 57.	Typical LC filter for a 4-Ω speaker . . . . .	37
Figure 58.	Behavior of pin DIAG for various protection conditions . . . . .	38
Figure 59.	Power derating curves for PCB used as heatsink . . . . .	39

# 1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491HV.

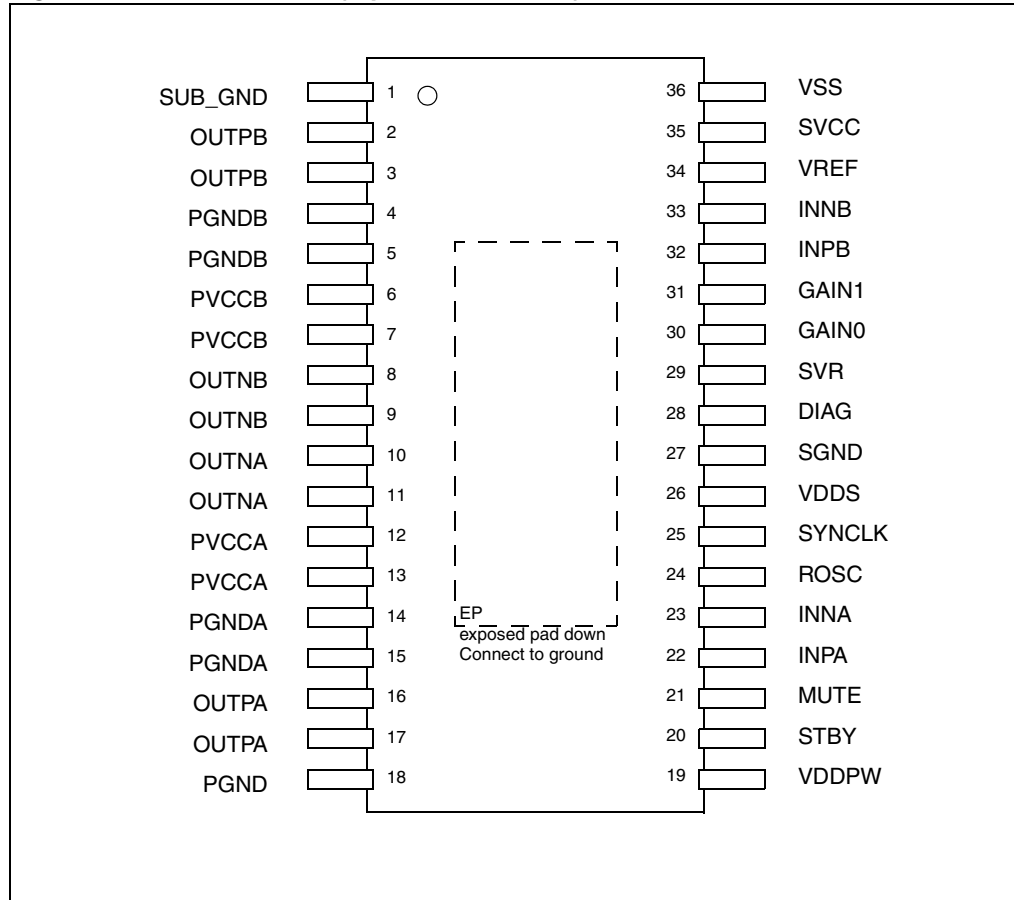
Figure 1. Internal block diagram (one channel only)



## 2 Pin description

### 2.1 Pin out

Figure 2. Pin connection (top view, PCB view)





## 2.2 Pin list

**Table 2. Pin description list**

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM for right channel
4,5	PGNDB	POWER	Power stage ground for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for right channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage ground for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage ground
19	VDDPW	OUT	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for ground-plane heatsink, to be connected to GND

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage for pins PVCCA, PVCCB, SVCC	23	V
$T_{op}$	Operating temperature	0 to 70	°C
$T_j$	Junction temperature	-40 to 150	°C
$T_{stg}$	Storage temperature	-40 to 150	°C

### 3.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j-case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j-amb}$	Thermal resistance, junction to ambient (mounted on recommended PCB) <sup>(1)</sup>	-	24	-	

1. FR4 with vias to copper area of 9 cm<sup>2</sup> (see also [Section 7.9: Heatsink requirements on page 39](#)).

### 3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5](#) below are given for the conditions:  $V_{CC} = 18\text{ V}$ ,  $R_L$  (load) = 8  $\Omega$ ,  $R_{OSC} = R3 = 39\text{ k}\Omega$ ,  $C8 = 100\text{ nF}$ ,  $f = 1\text{ kHz}$ ,  $G_V = 20\text{ dB}$ , and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

**Table 5. Electrical specifications**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{CC}$	Supply voltage for pins PVCCA, PVCCB, SVCC	-	5	-	18	V
$I_q$	Total quiescent current	-	-	26	35	mA
$I_{qSTBY}$	Quiescent current in standby	-	-	2.5	5.0	$\mu\text{A}$
$V_{OS}$	Output offset voltage	Play mode	-150	-	150	mV
$V_{OS}$	Output offset voltage	Mute mode	-150	-	150	mV
$I_{OCP}$	Overcurrent protection threshold	$R_L = 0\ \Omega$	3	5	-	A
$T_j$	Junction temperature at thermal shut-down	-	-	150	-	°C
$R_i$	Input resistance	Differential input	55	60	-	k $\Omega$
$V_{OVP}$	Overvoltage protection threshold	-	18.5	21	-	V

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{\text{UVP}}$	Undervoltage protection threshold	-	-	-	4	V
$R_{\text{dsON}}$	Power transistor on resistance	High side	-	0.2	-	$\Omega$
		Low side	-	0.2	-	
$P_o$	Output power	THD = 10%	-	20	-	W
		THD = 1%	-	16	-	
$P_o$	Output power	$R_L = 8 \Omega$ , THD = 10%	-	9.5	-	W
		$R_L = 8 \Omega$ , THD = 1% $V_{\text{CC}} = 12 \text{ V}$	-	7.2	-	
$P_D$	Dissipated power	$P_o = 20 \text{ W} + 20 \text{ W}$ , THD = 10%	-	4.0	-	W
$\eta$	Efficiency	$P_o = 20 \text{ W} + 20 \text{ W}$	80	90	-	%
THD	Total harmonic distortion	$P_o = 1 \text{ W}$	-	0.1	0.4	%
$G_V$	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
$\Delta G_V$	Gain matching	-	-1	-	1	dB
CT	Cross talk	$f = 1 \text{ kHz}$	-	50	-	dB
eN	Total input noise	A Curve, $G_V = 20 \text{ dB}$	-	20	-	$\mu\text{V}$
		$f = 22 \text{ Hz to } 22 \text{ kHz}$	-	25	35	
SVRR	Supply voltage rejection ratio	$f_r = 100 \text{ Hz}$ , $V_r = 0.5 \text{ V}$ , $C_{\text{SVR}} = 10 \mu\text{F}$	40	50	-	dB
$T_r, T_f$	Rise and fall times	-	-	50	-	ns
$f_{\text{SW}}$	Switching frequency	Internal oscillator	290	310	330	kHz
$f_{\text{SWR}}$	Output switching frequency	With internal oscillator <sup>(1)</sup>	250	-	-	kHz
		With external oscillator <sup>(2)</sup>	250	-	-	
$V_{\text{inH}}$	Digital input high (H)	-	2.3	-	-	V
$V_{\text{inL}}$	Digital input low (L)		-	-	0.8	
$A_{\text{MUTE}}$	Mute attenuation	$V_{\text{MUTE}} = 1 \text{ V}$	60	80	-	dB
Function mode	Standby, mute and play modes	$V_{\text{STBY}} < 0.5 \text{ V}$ , $V_{\text{MUTE}} = X$	Standby			-
		$V_{\text{STBY}} > 2.5 \text{ V}$ , $V_{\text{MUTE}} < 0.8 \text{ V}$	Mute			-
		$V_{\text{STBY}} > 2.5 \text{ V}$ , $V_{\text{MUTE}} > 2.5 \text{ V}$	Play			-

1.  $f_{\text{SW}} = 10^6 / ((16 * R_{\text{OSC}} + 182) * 4)$  kHz,  $f_{\text{SYNCLK}} = 2 * f_{\text{SW}}$  with  $R_3 = 39 \text{ k}\Omega$  (see [Figure 50](#)).

2.  $f_{\text{SW}} = f_{\text{SYNCLK}} / 2$  with the frequency of the external oscillator.

## 4 Characterization curves

The following characterization curves were made using the SZ-LAB-TDA7492P demo board. The LC filter for the 4-Ω load uses components of 15 μH and 470 nF, whilst that for the 6-Ω load uses 22 μH and 220 nF and that for the 8-Ω load uses 33 μH and 220 nF.

All other test conditions are given along side the corresponding curves.

### 4.1 With 4-Ω load at V<sub>CC</sub> = 14 V

Figure 3. Output power vs supply voltage

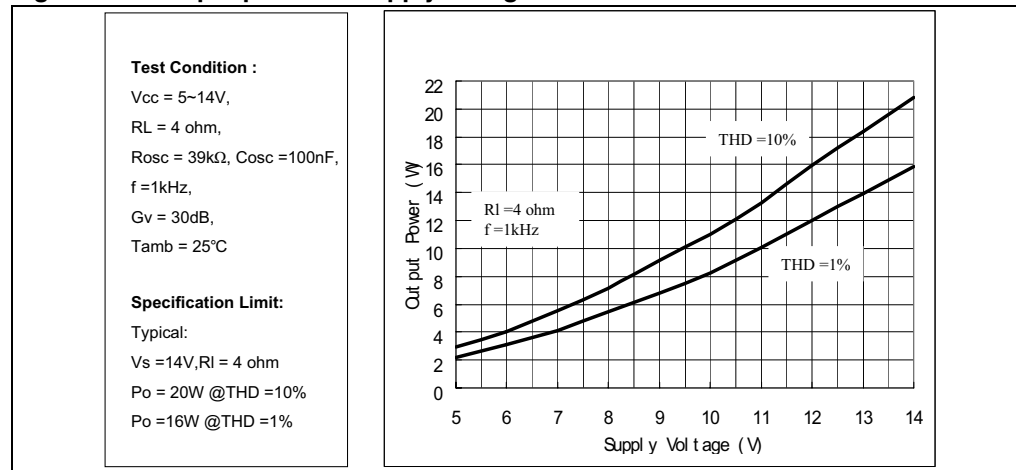
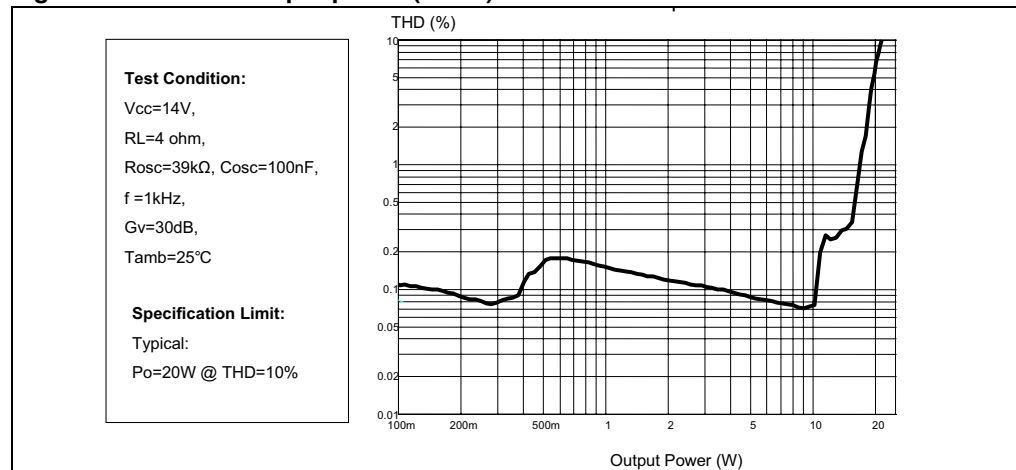
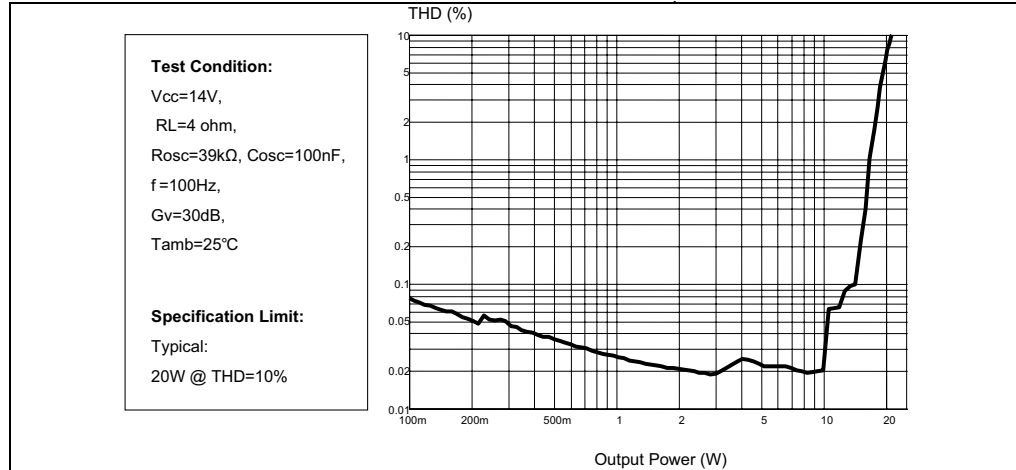


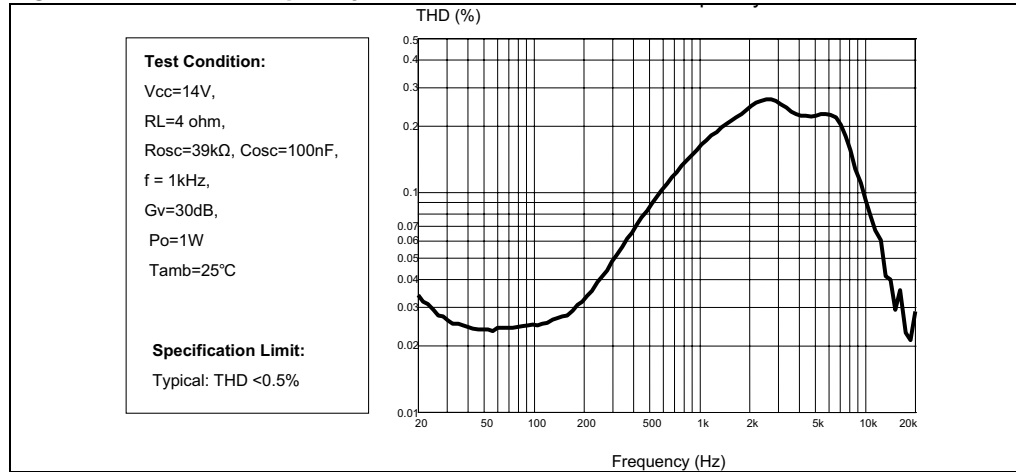
Figure 4. THD vs output power (1 kHz)



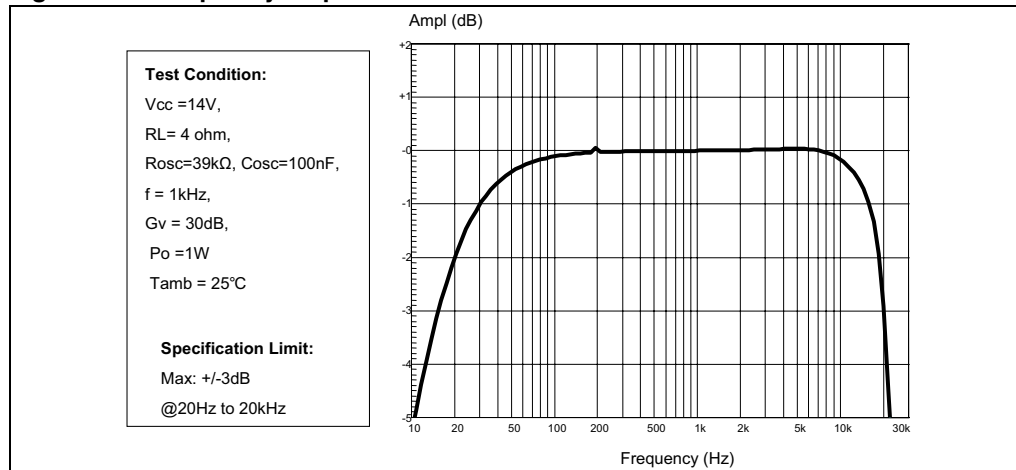
**Figure 5. THD vs output power (100 Hz)**



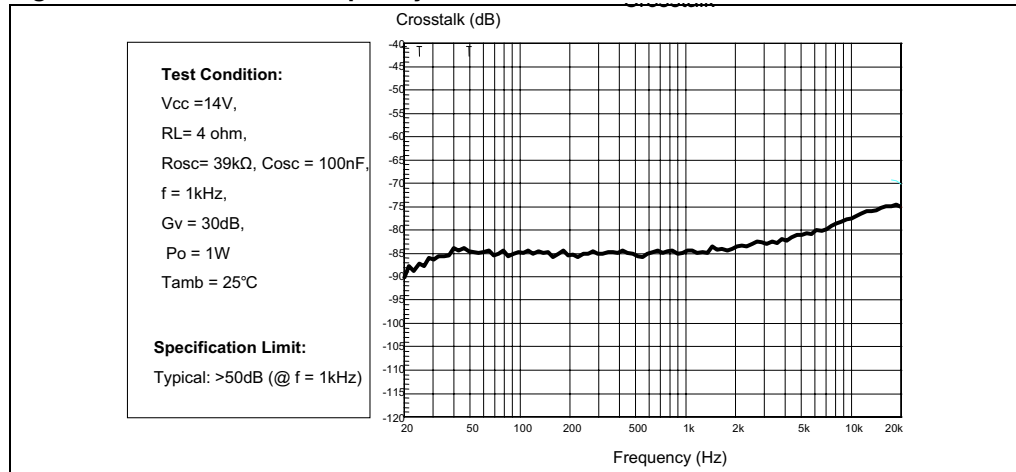
**Figure 6. THD vs frequency**



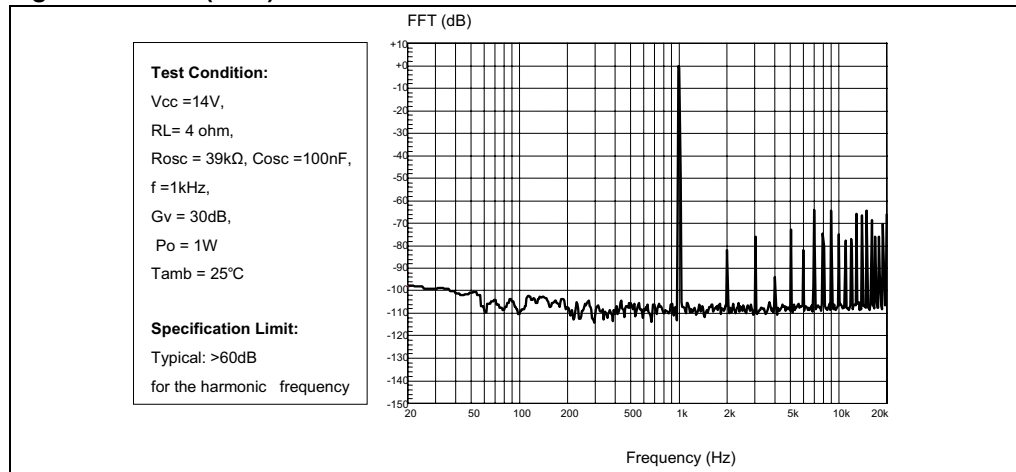
**Figure 7. Frequency response**



**Figure 8. Crosstalk vs frequency**



**Figure 9. FFT (0 dB)**



**Figure 10. FFT (-60 dB)**

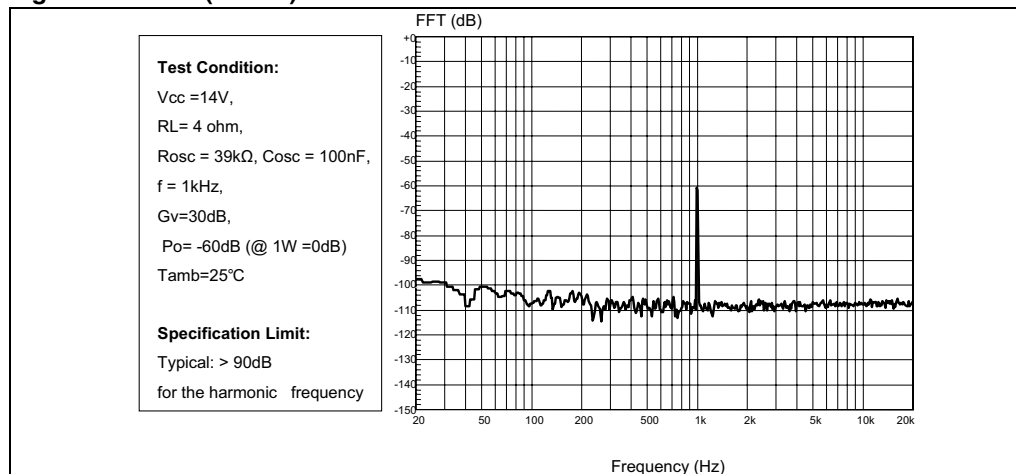


Figure 11. Power supply rejection ratio vs frequency

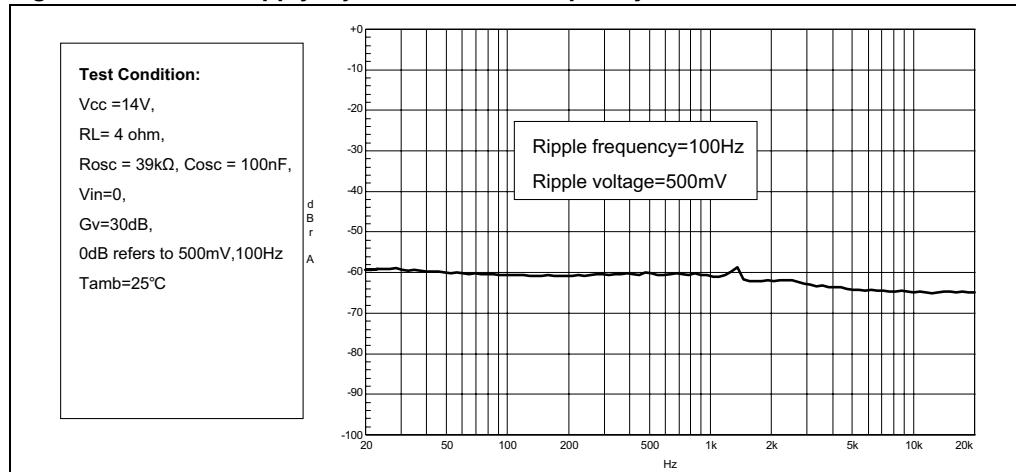


Figure 12. Power dissipation and efficiency vs output power

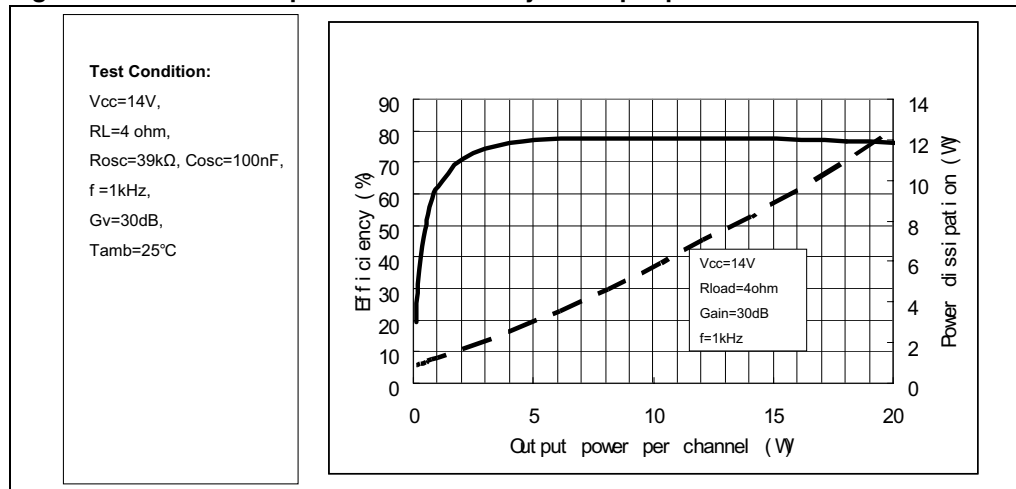
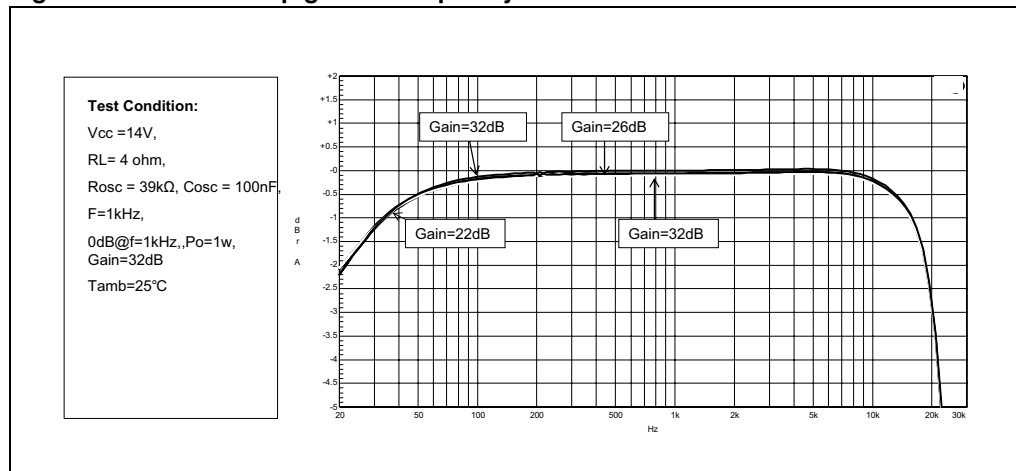
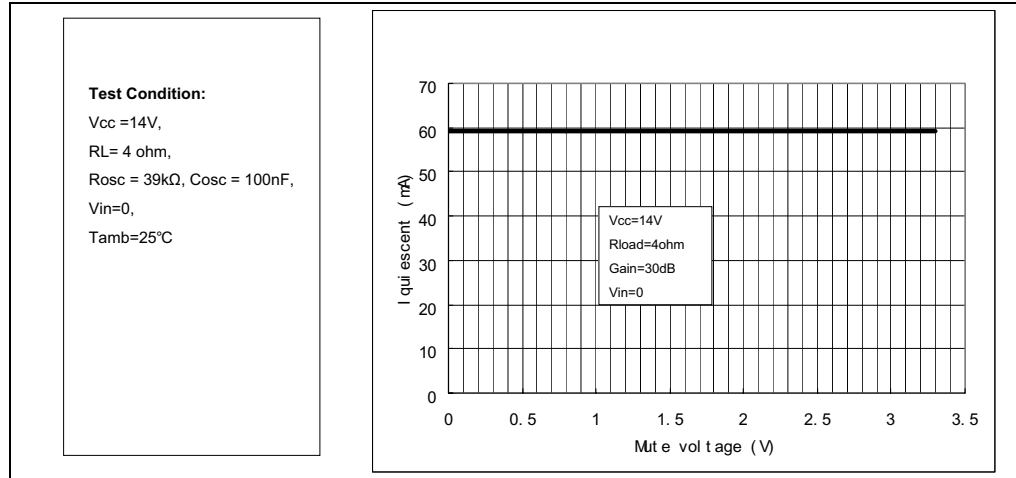


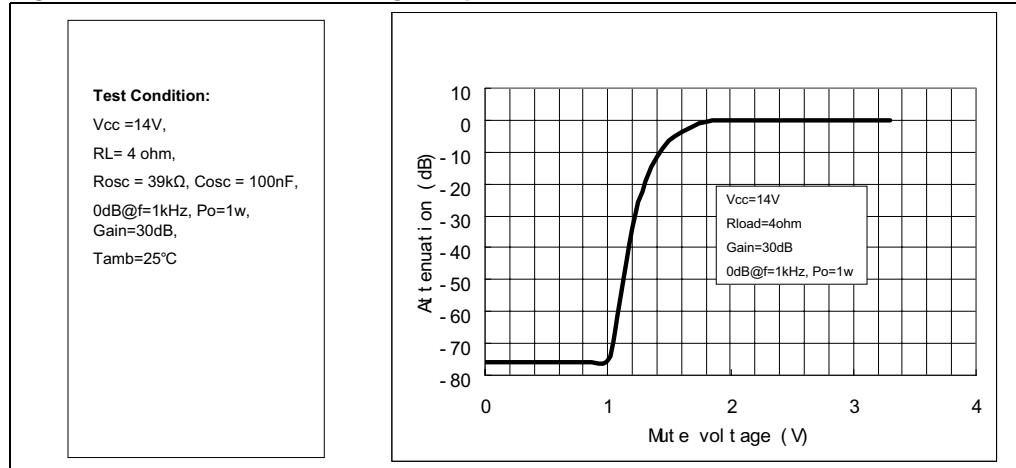
Figure 13. Closed-loop gain vs frequency



**Figure 14. Current consumption vs voltage on pin MUTE**



**Figure 15. Attenuation vs voltage on pin MUTE**



**Figure 16. Current consumption vs voltage on pin STBY**

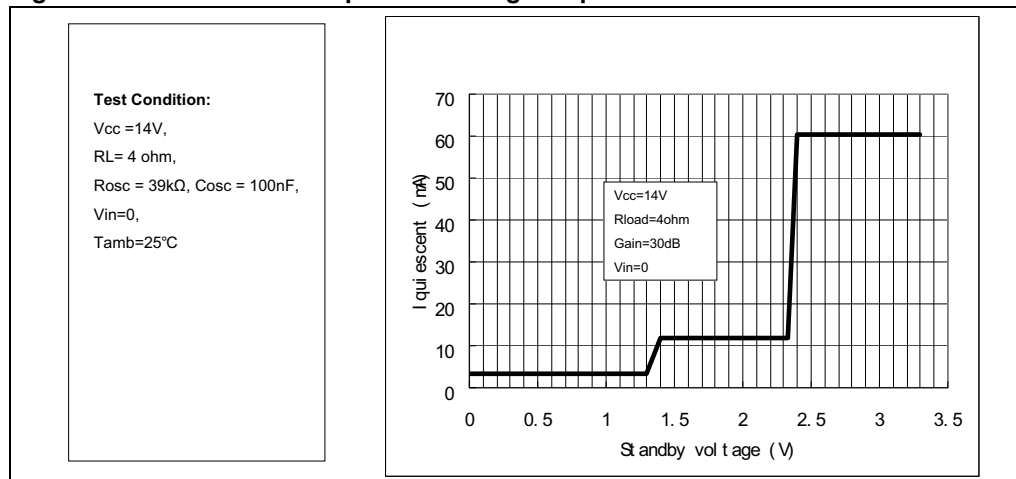
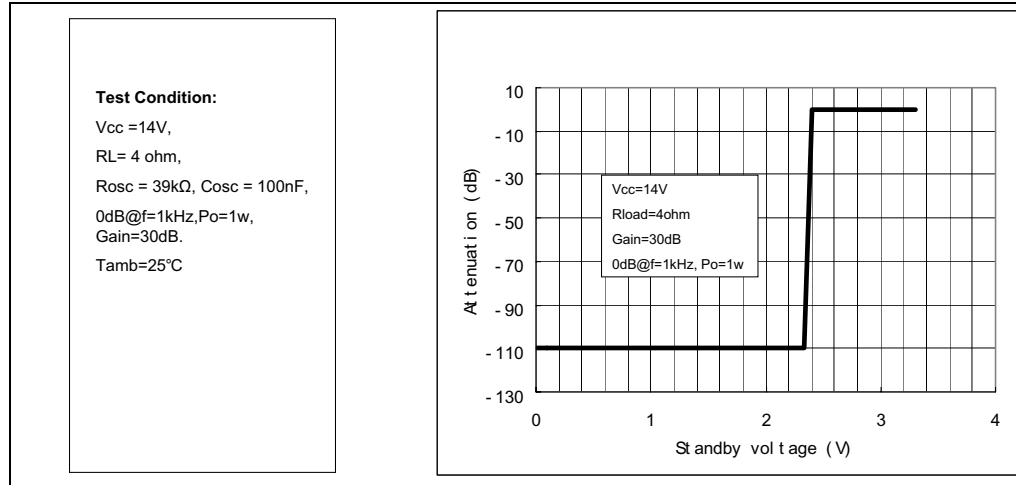


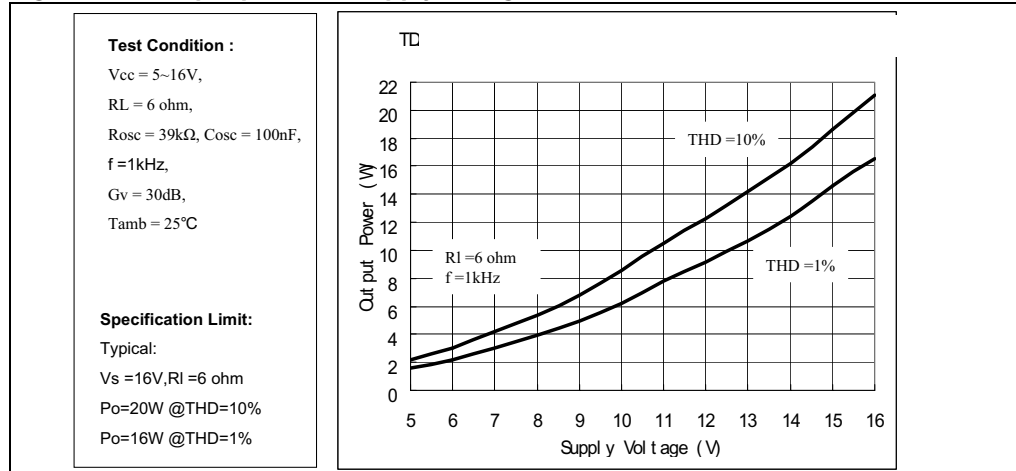


Figure 17. Attenuation vs voltage on pin STBY

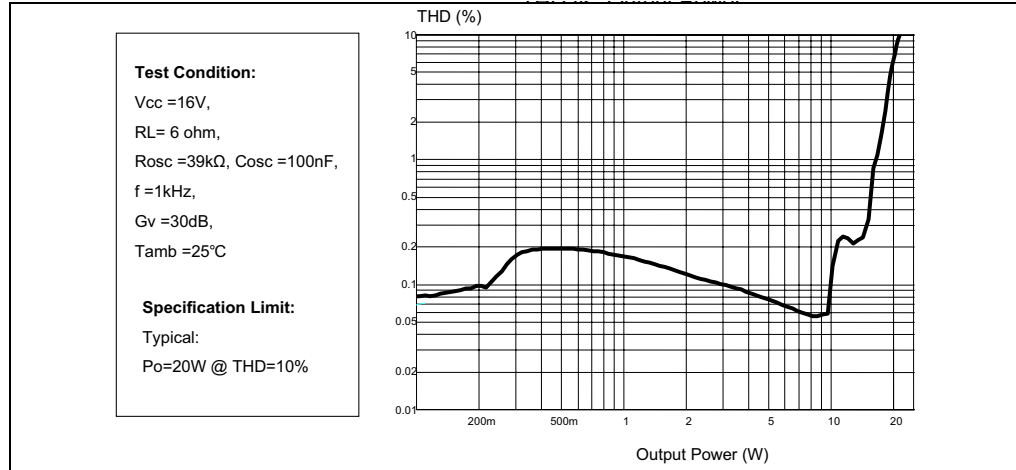


## 4.2 With 6-Ω load at V<sub>CC</sub> = 16 V

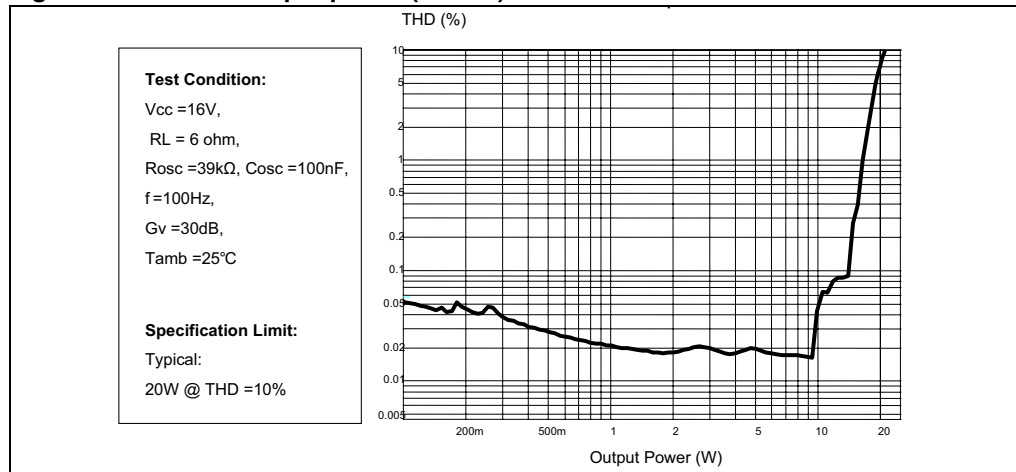
Figure 18. Output power vs supply voltage



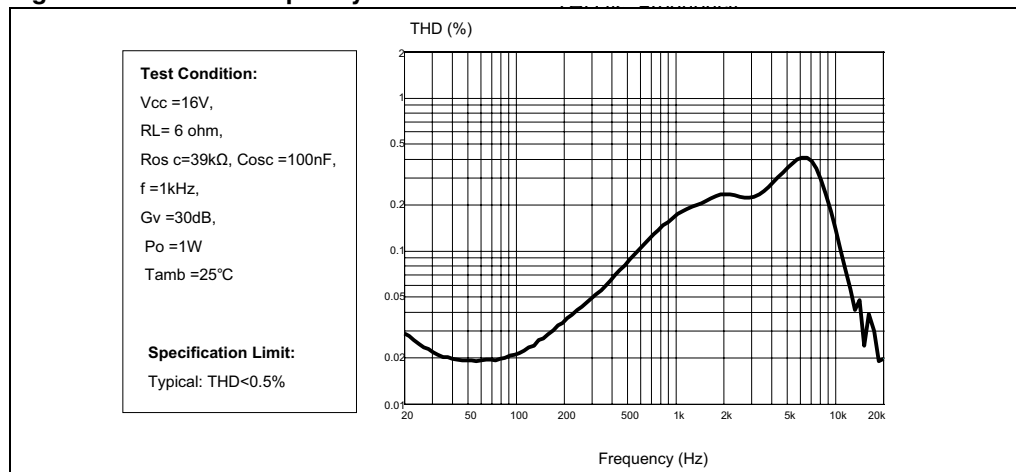
**Figure 19. THD vs output power (1 kHz)**



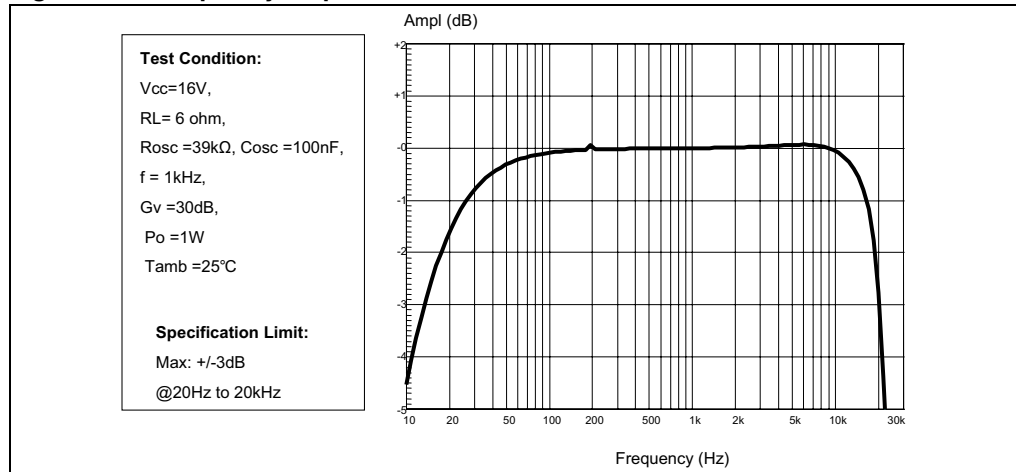
**Figure 20. THD vs output power (100 Hz)**



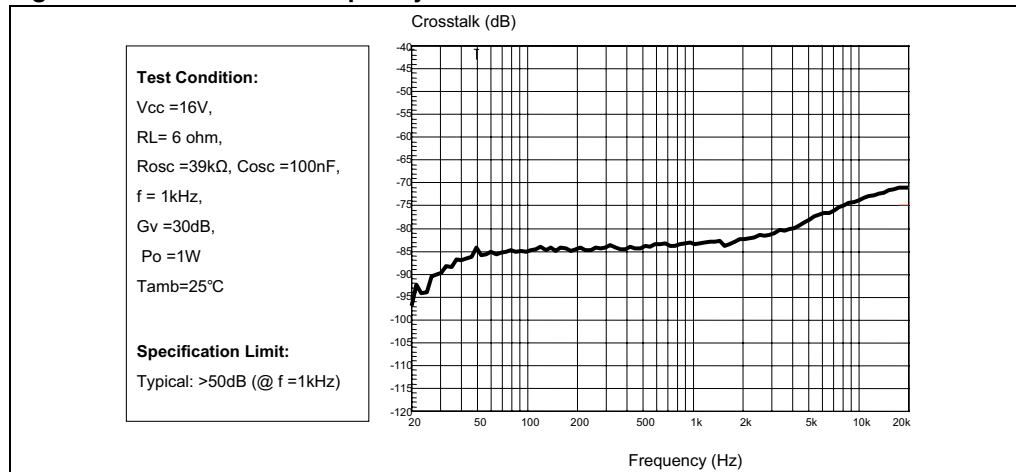
**Figure 21. THD vs frequency**



**Figure 22. Frequency response**



**Figure 23. Crosstalk vs frequency**



**Figure 24. FFT (0 dB)**

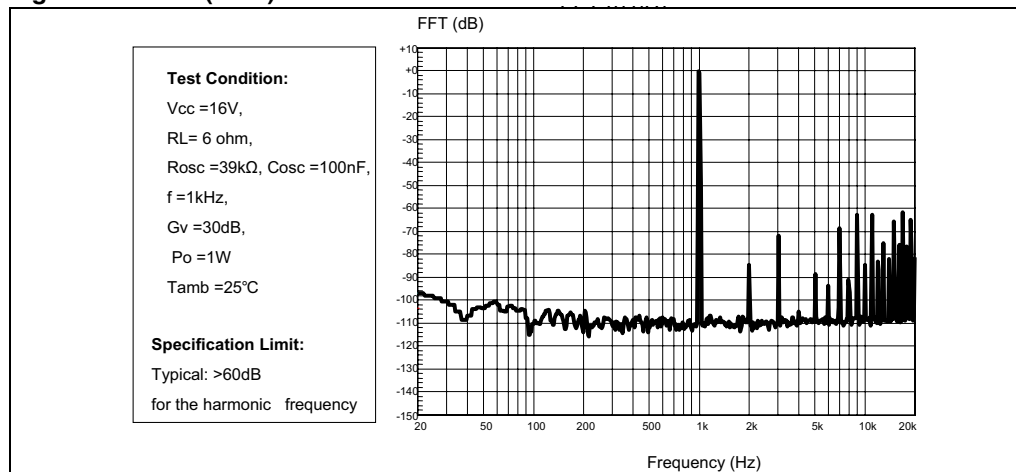


Figure 25. FFT (-60 dB)

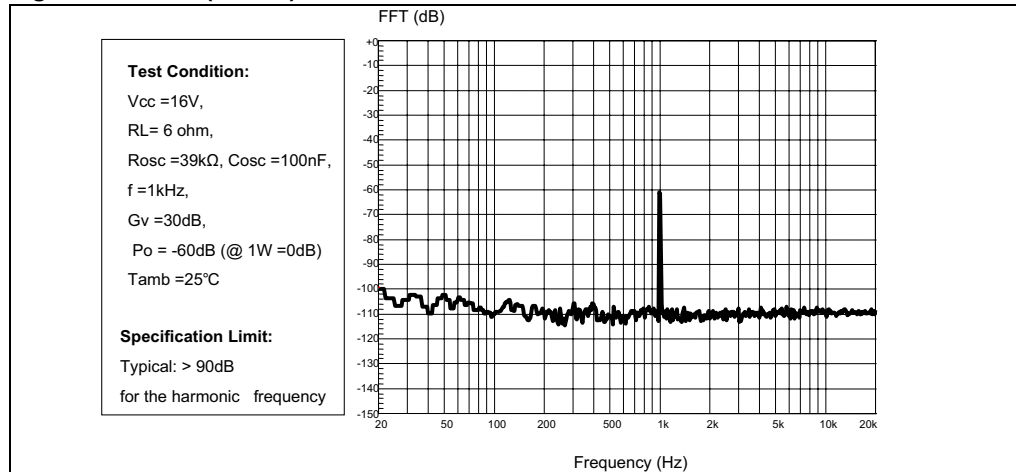


Figure 26. Power supply rejection ratio vs frequency

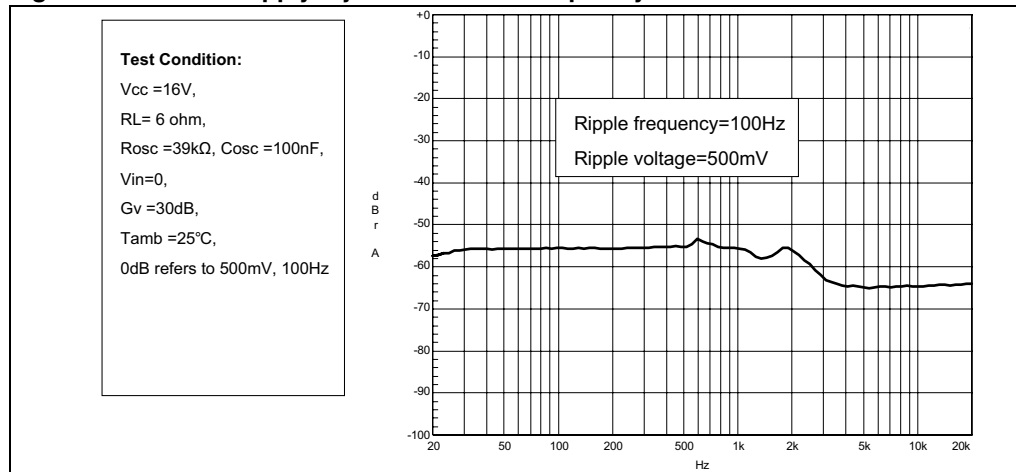


Figure 27. Power dissipation and efficiency vs output power

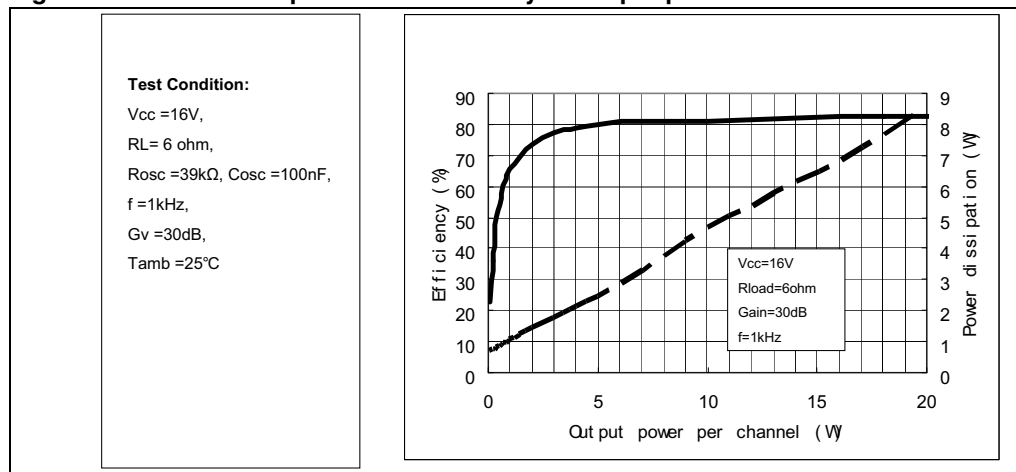


Figure 28. Closed-loop gain vs frequency

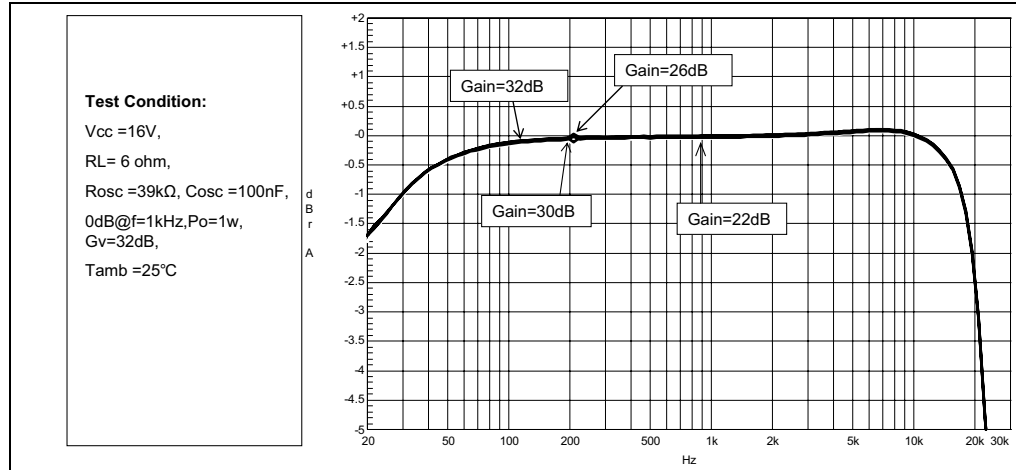


Figure 29. Current consumption vs voltage on pin MUTE

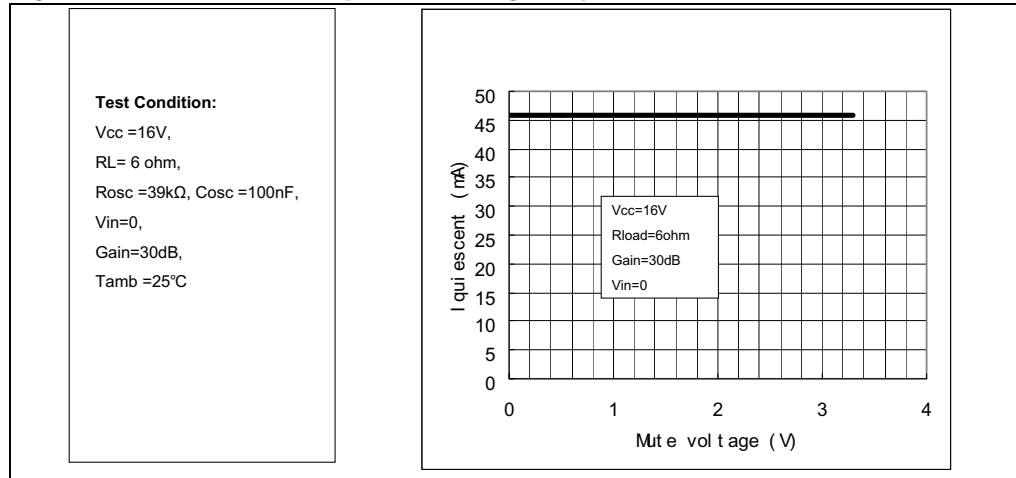
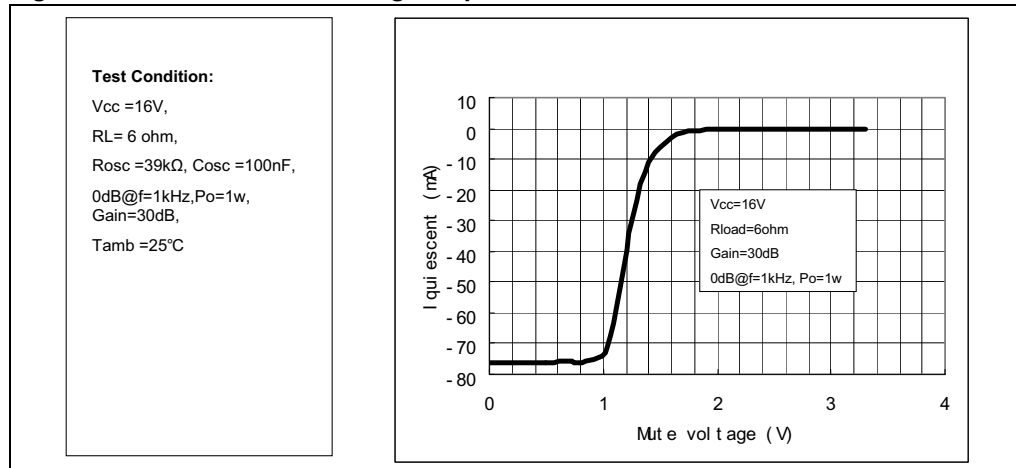
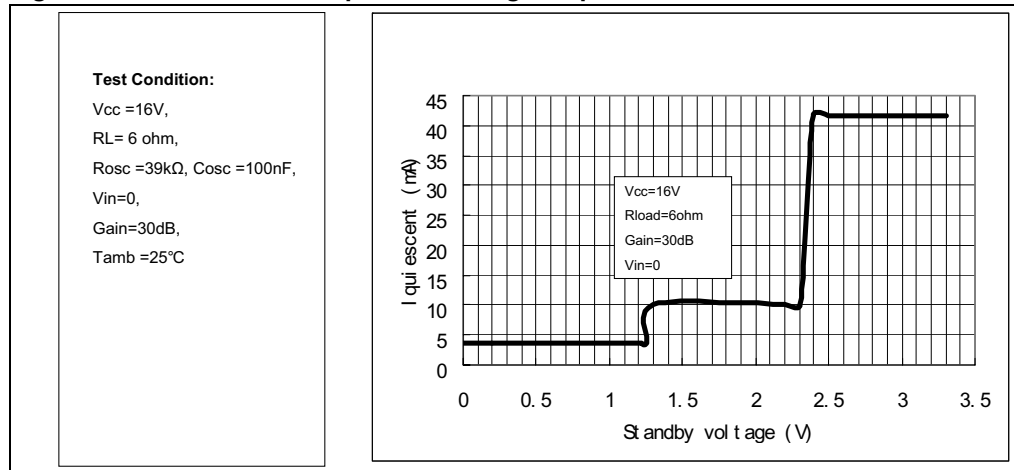


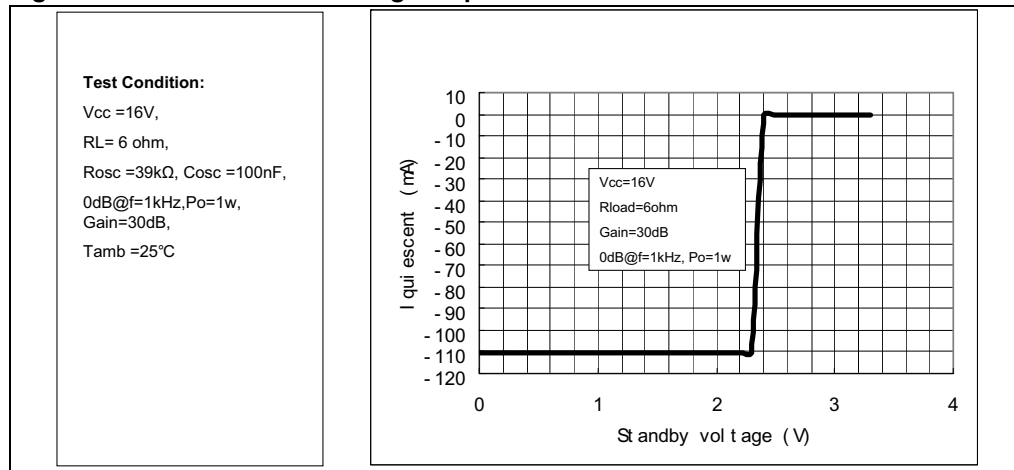
Figure 30. Attenuation vs voltage on pin MUTE



**Figure 31. Current consumption vs voltage on pin STBY**



**Figure 32. Attenuation vs voltage on pin STBY**



### 4.3 With 8-Ω load at V<sub>CC</sub> = 18 V

Figure 33. Output power vs supply voltage

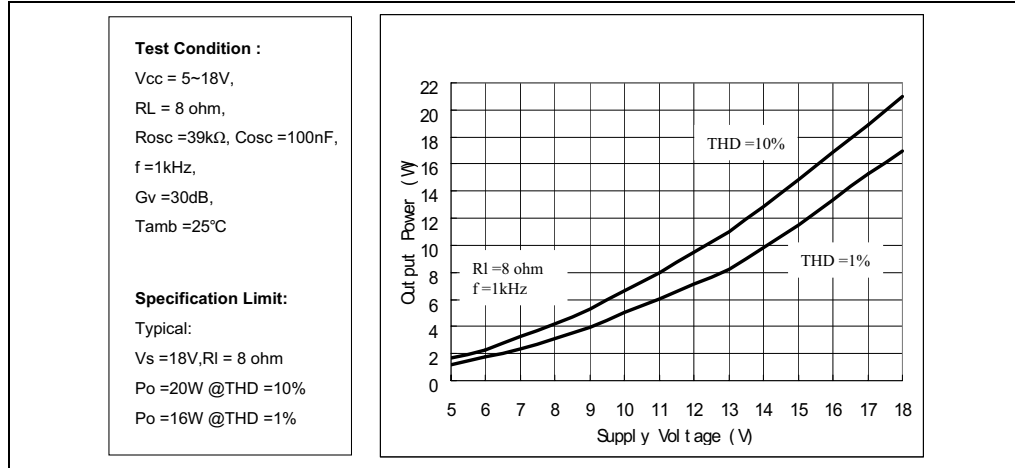
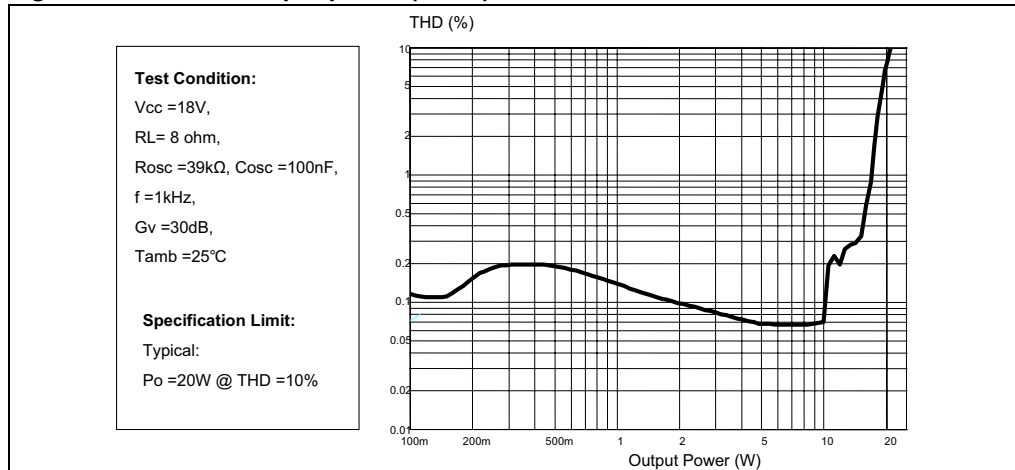
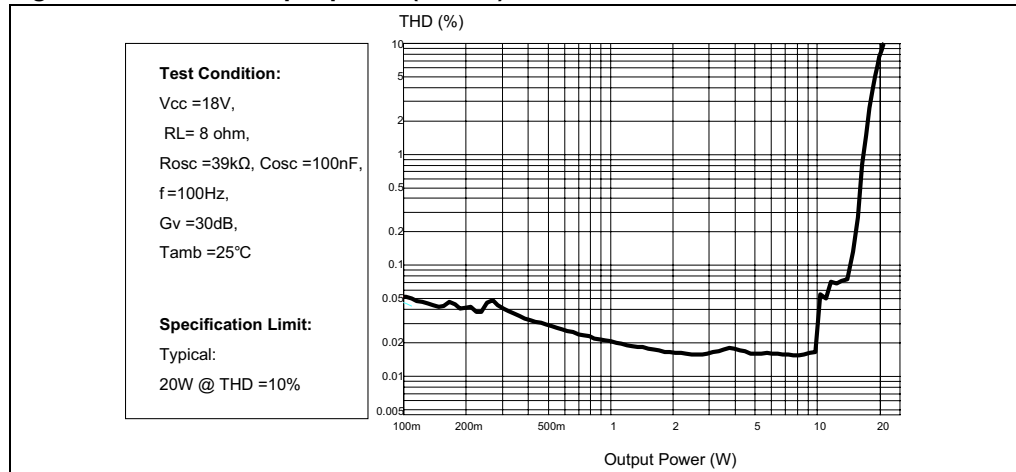


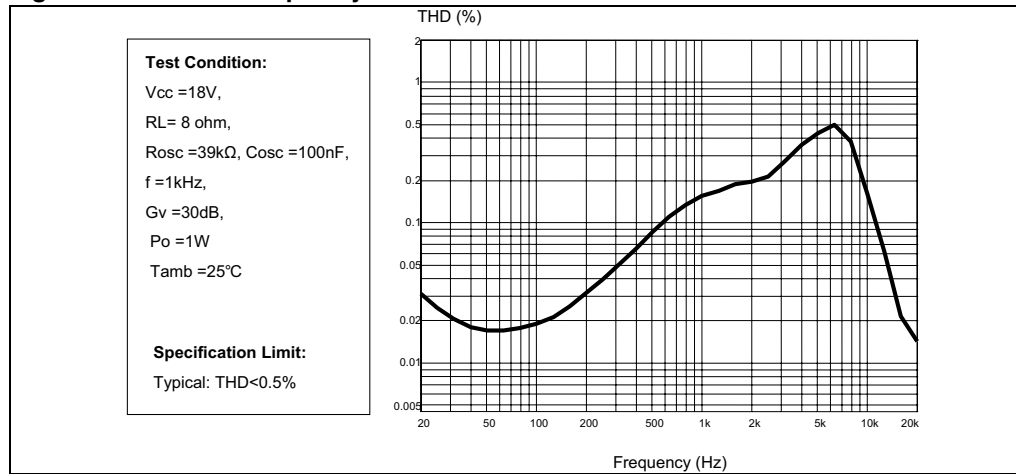
Figure 34. THD vs output power (1 kHz)



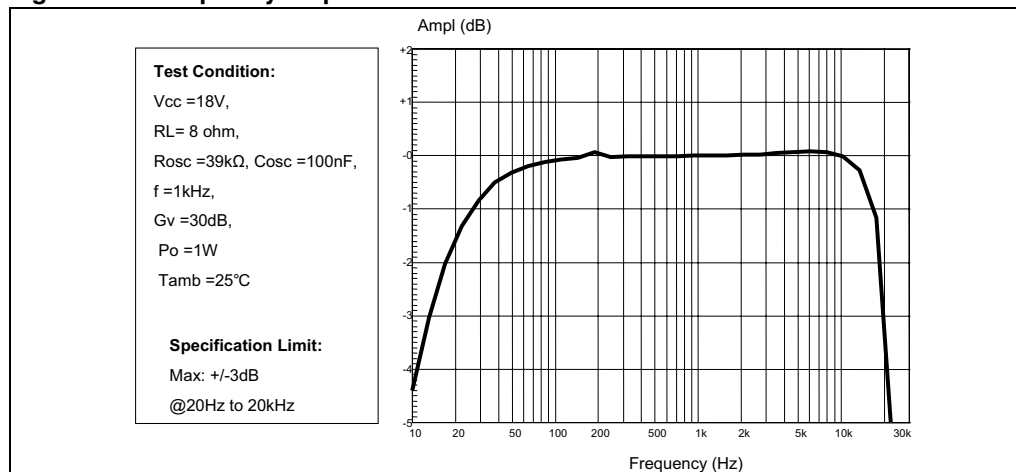
**Figure 35. THD vs output power (100 Hz)**



**Figure 36. THD vs frequency**

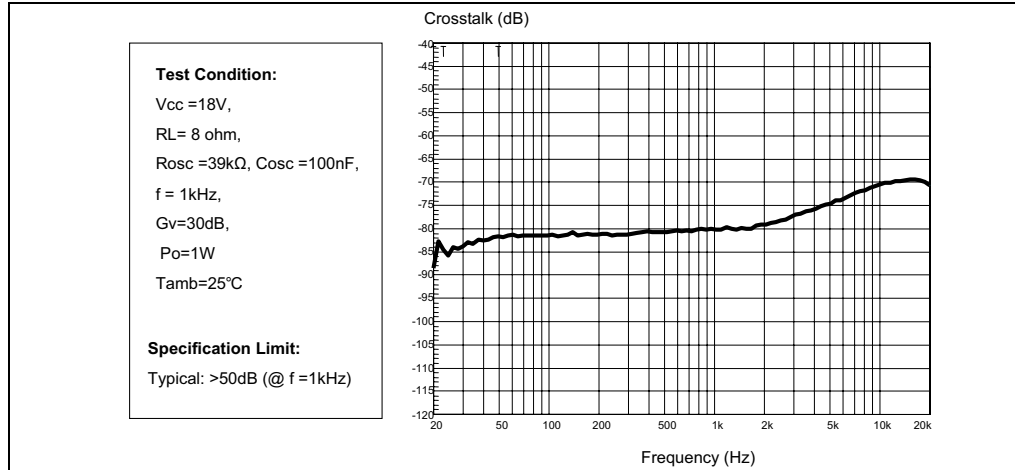


**Figure 37. Frequency response**

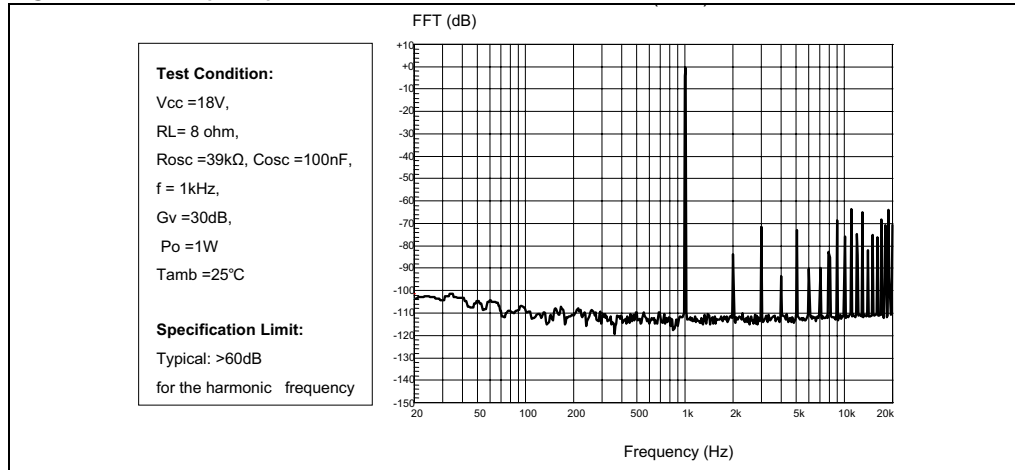




**Figure 38. Crosstalk vs frequency**



**Figure 39. FFT (0 dB)**



**Figure 40. FFT (-60 dB)**

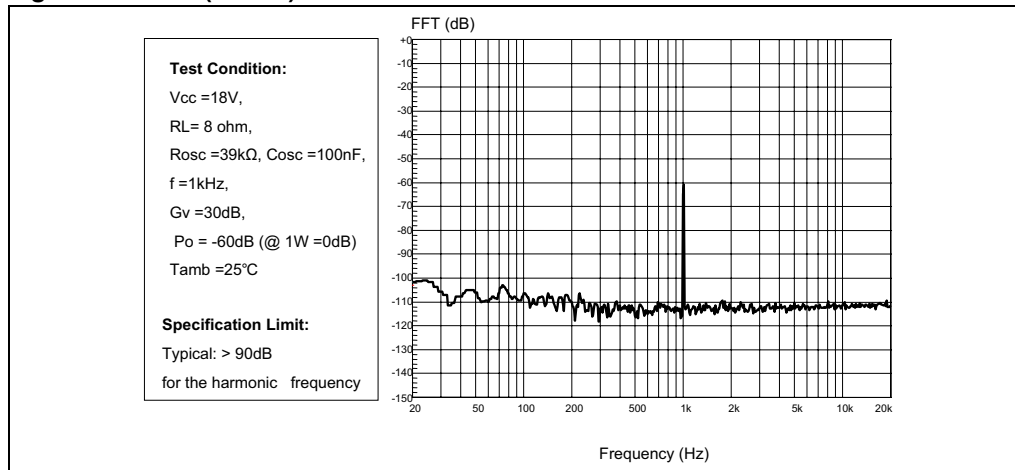


Figure 41. Power supply rejection ratio vs frequency

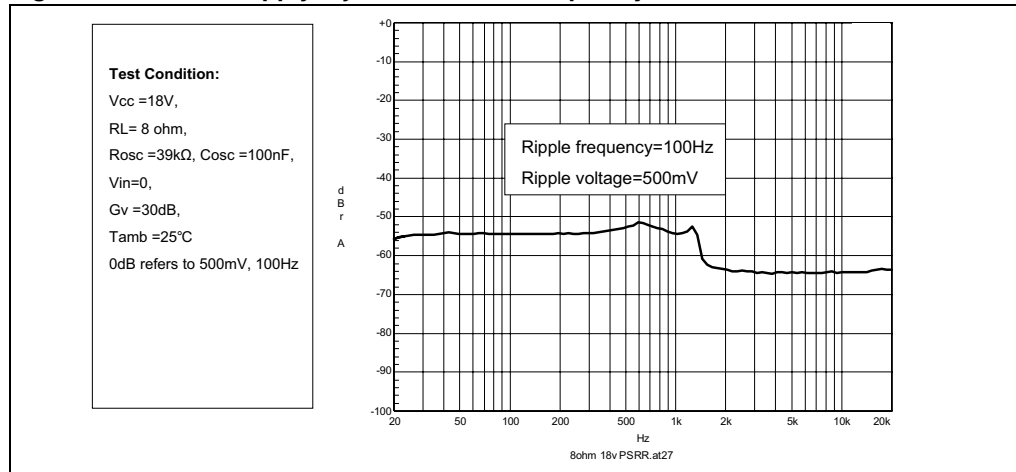


Figure 42. Power dissipation and efficiency vs output power

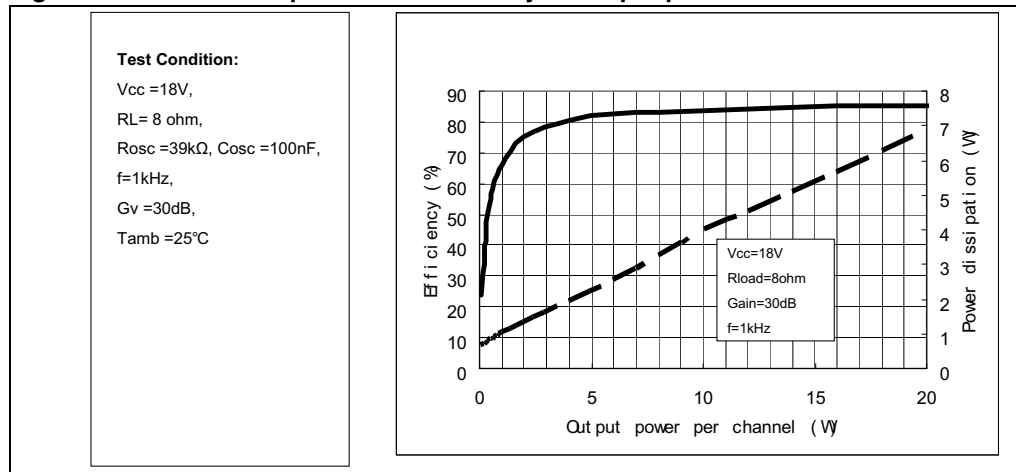
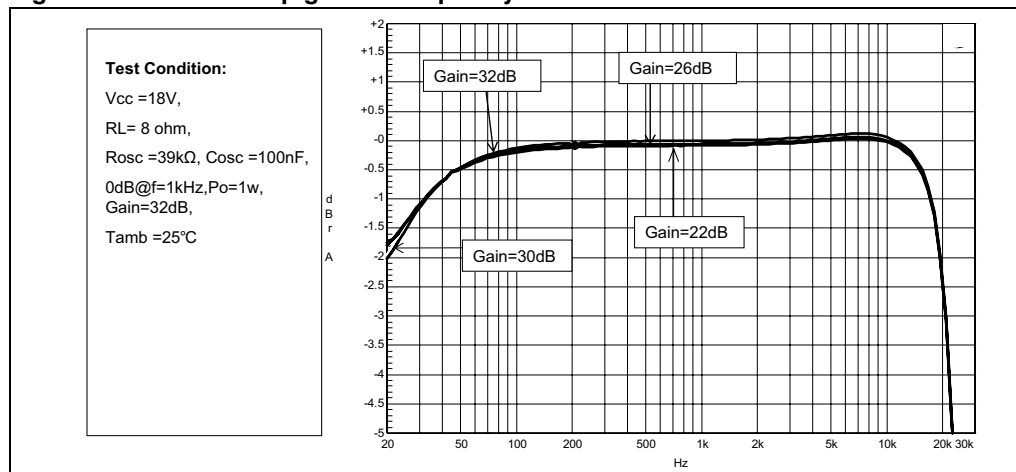
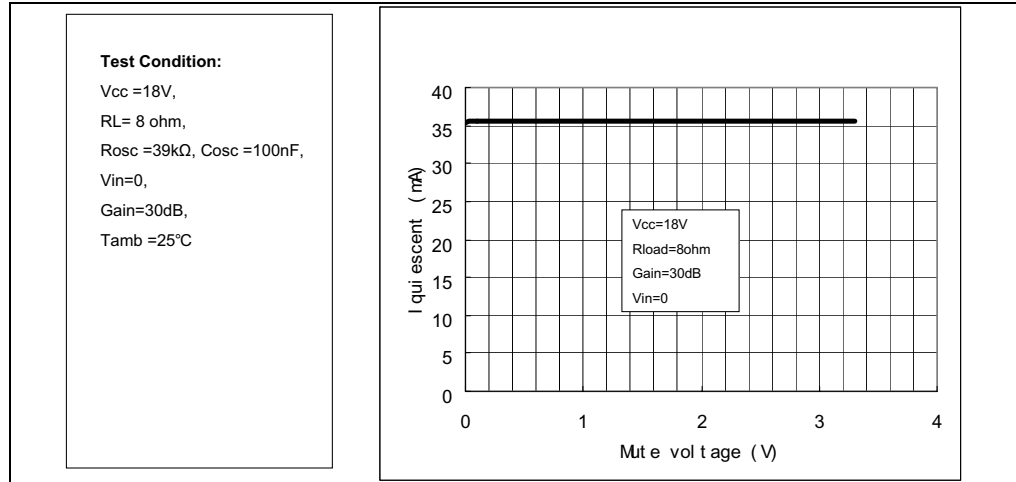


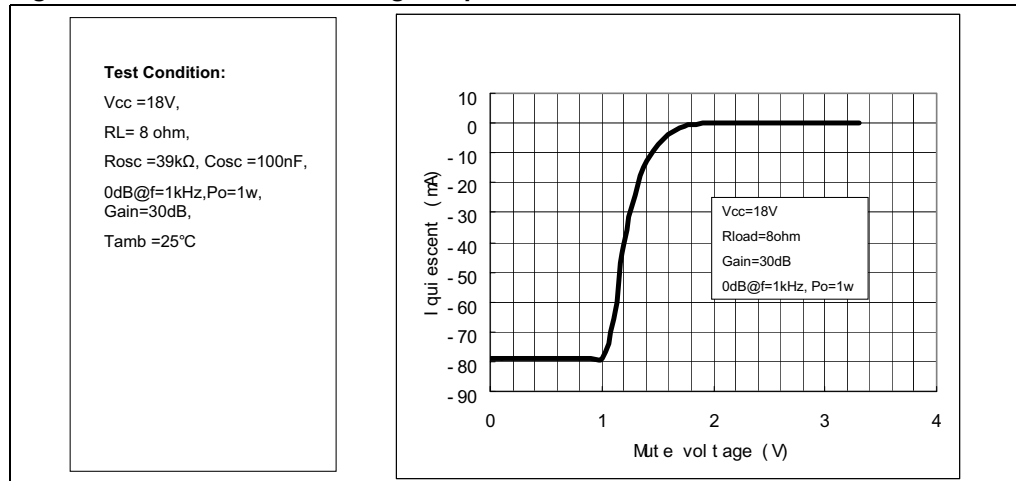
Figure 43. Closed-loop gain vs frequency



**Figure 44. Current consumption vs voltage on pin MUTE**



**Figure 45. Attenuation vs voltage on pin MUTE**



**Figure 46. Current consumption vs voltage on pin STBY**

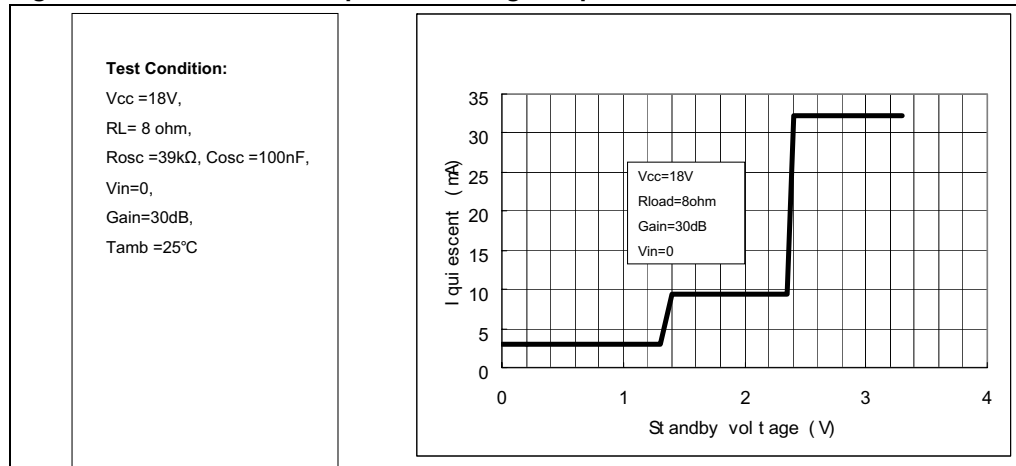
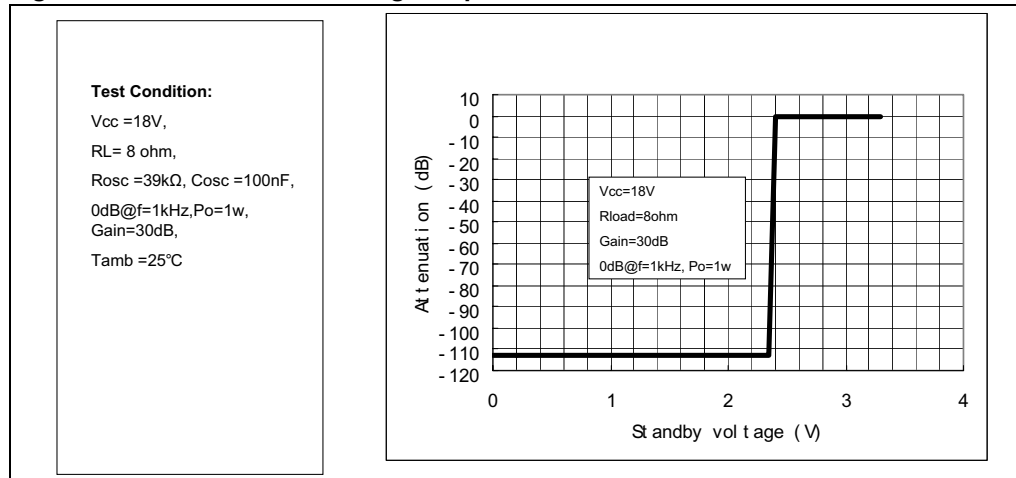
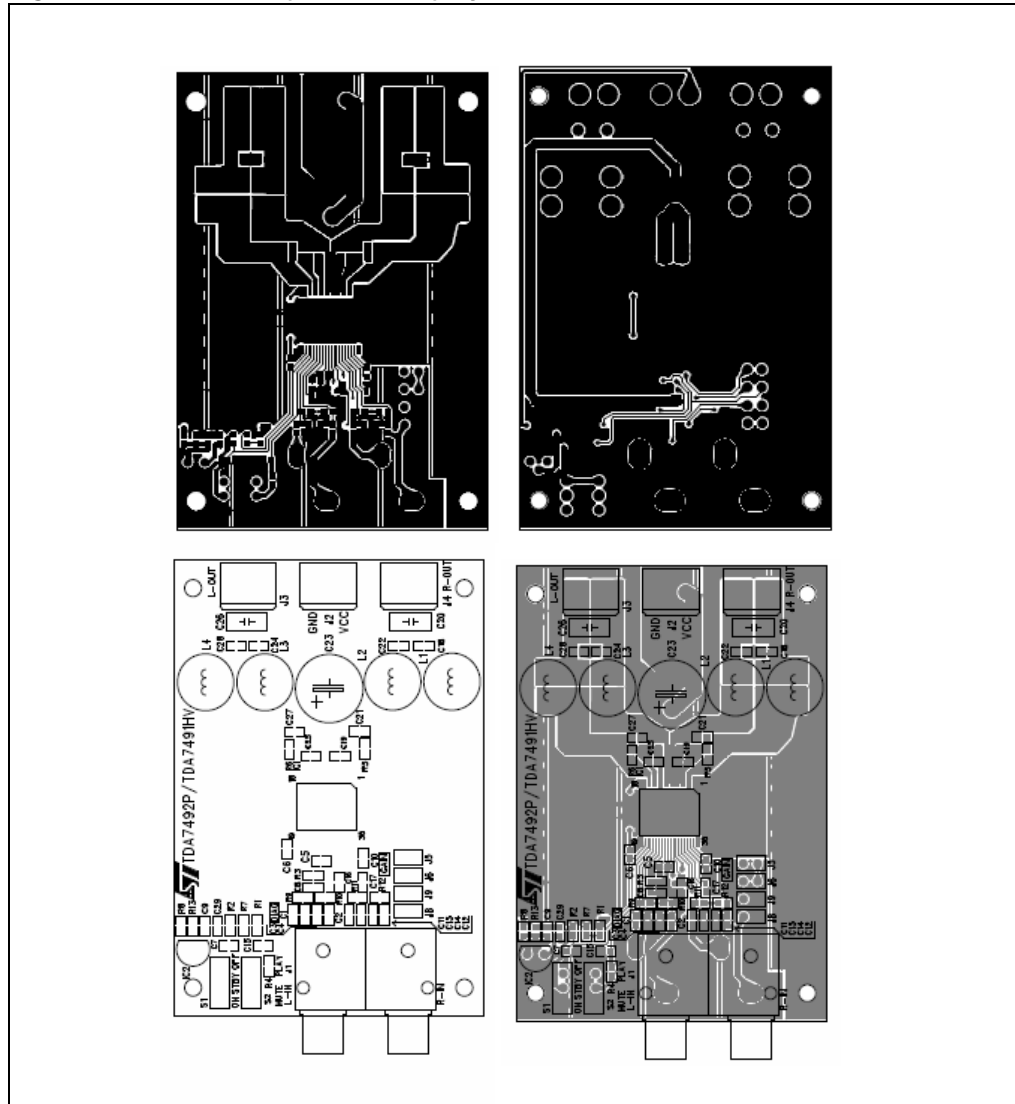


Figure 47. Attenuation vs voltage on pin STBY



### 4.4 Test board

Figure 48. Test board (TDA7491HV) layout



## 5 Package mechanical data

The TDA7491HV comes in a 36-pin PowerSSO package with exposed pad down (EPD).

[Figure 49](#) below shows the package outline and [Table 6](#) gives the dimensions.

**Figure 49. PowerSSO-36 EPD outline drawing**

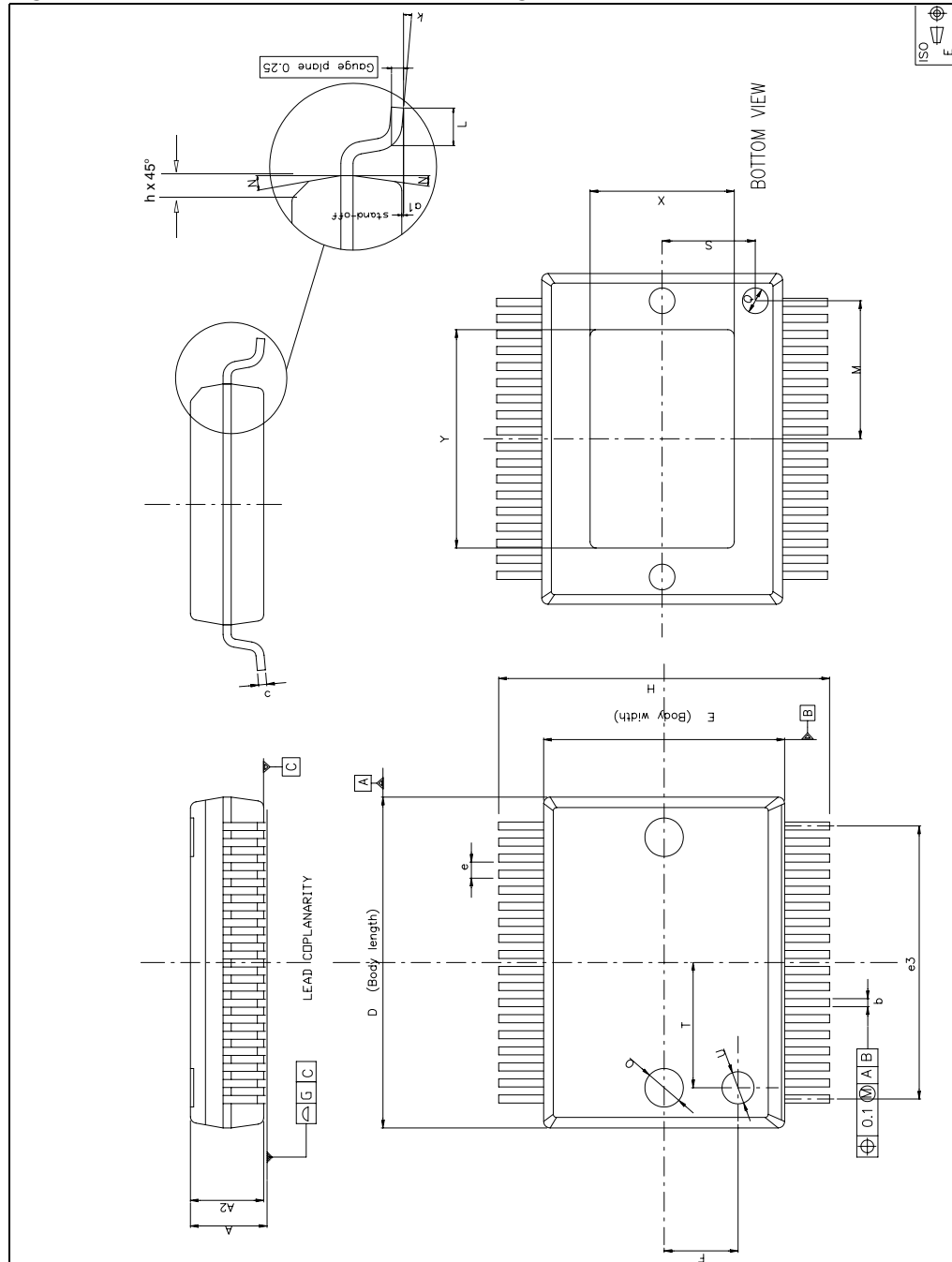


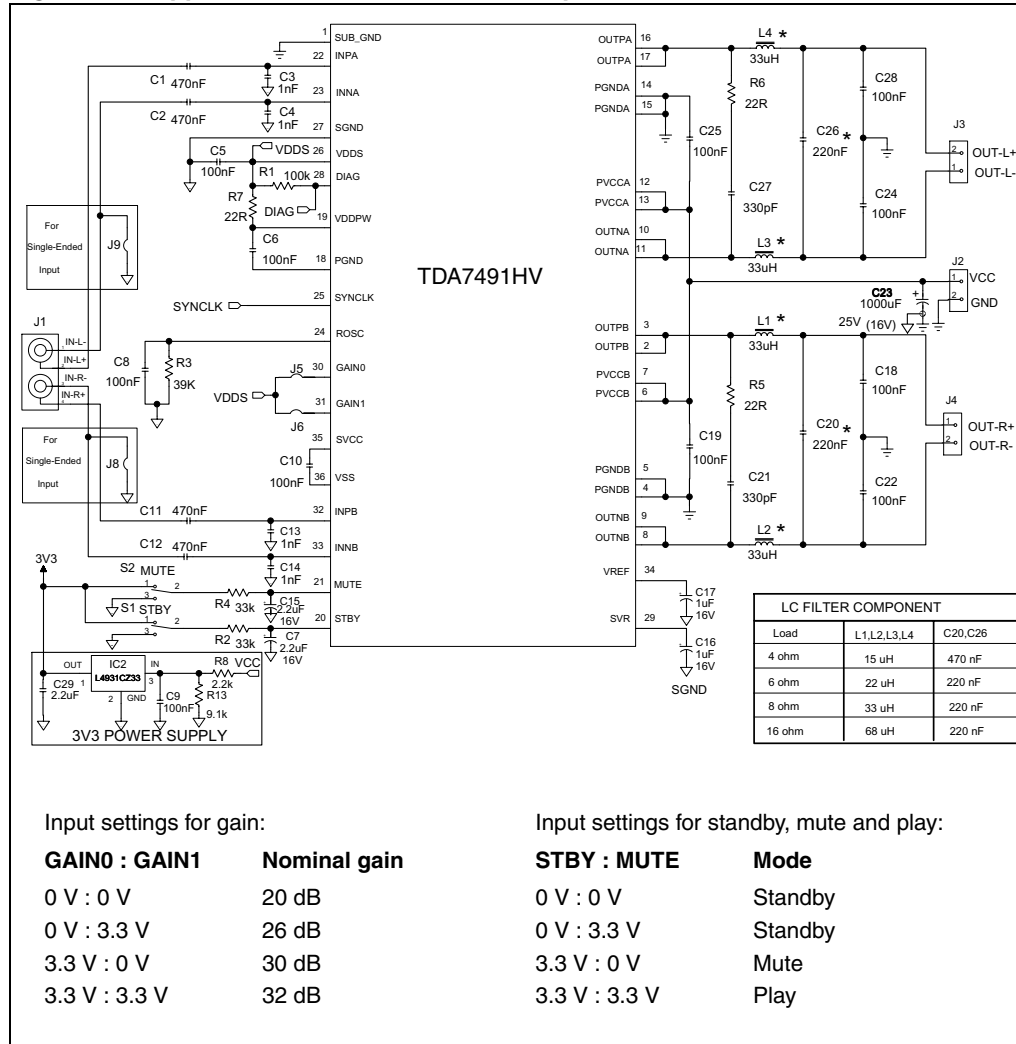
Table 6. PowerSSO-36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.000	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

# 6 Applications circuit

Figure 50. Applications circuit for class-D amplifier





## 7 Application information

### 7.1 Mode selection

The three operating modes of the TDA7491HV are set by the two inputs STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

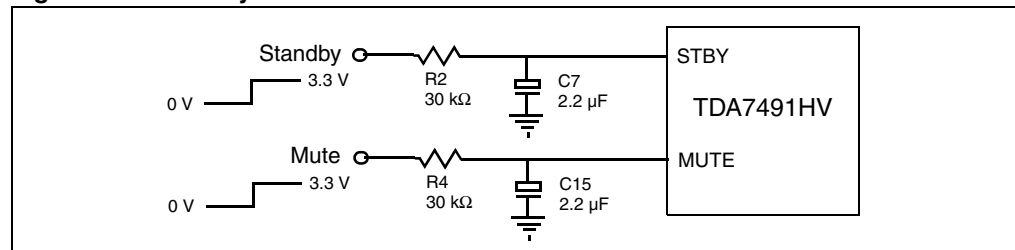
The protection functions of the TDA7491HV are realized by pulling down the voltages of the STBY and MUTE inputs shown in [Figure 51](#). The input current of the corresponding pins must be limited to 200  $\mu$ A.

**Table 7. Mode settings**

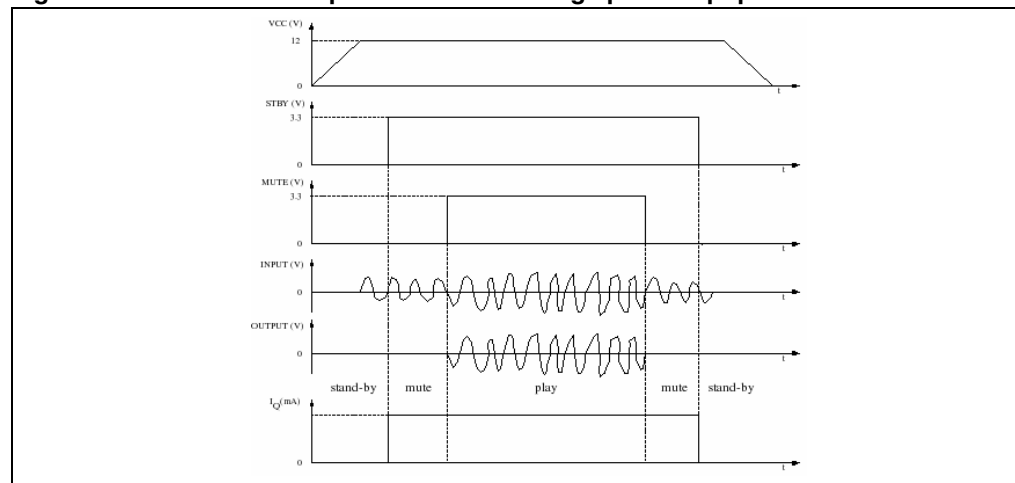
Mode Selection	STBY	MUTE
Standby	L <sup>(1)</sup>	X (don't care)
Mute	H <sup>(1)</sup>	L
Play	H	H

1. Drive levels defined in [Table 5: Electrical specifications on page 10](#)

**Figure 51. Standby and mute circuits**



**Figure 52. Turn-on/off sequence for minimizing speaker "pop"**



## 7.2 Gain setting

The gain of the TDA7491HV is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

**Table 8. Gain settings**

GAIN0	GAIN1	Nominal gain, $G_v$ (dB)
0	0	20
0	1	26
1	0	30
1	1	32

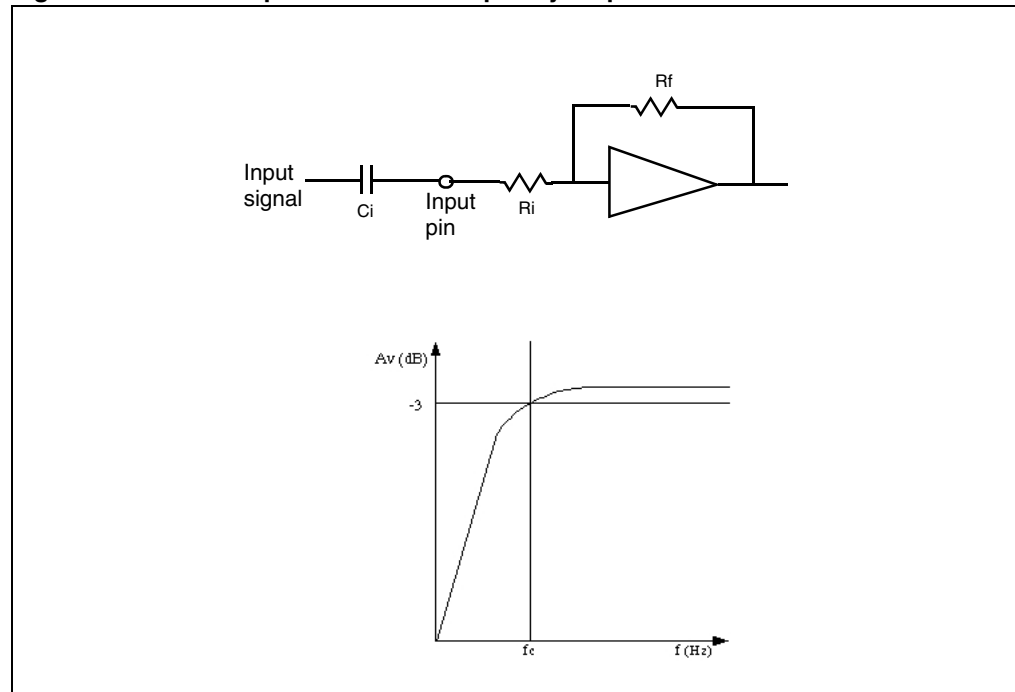
## 7.3 Input resistance and capacitance

The input impedance is set by an internal resistor  $R_i = 60 \text{ k}\Omega$  (typical). An input capacitor ( $C_i$ ) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in [Figure 53](#). For  $C_i = 220 \text{ nF}$  the high-pass filter cut-off frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

**Figure 53. Device input circuit and frequency response**



## 7.4 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7491HV as master clock, while the other devices are in slave mode (that is, externally clocked). The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

### 7.4.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency,  $f_{SW}$ , is controlled by the resistor,  $R_{OSC}$ , connected to pin ROOSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where  $R_{OSC}$  is in  $k\Omega$ .

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor  $R_{OSC}$  must be less than 60  $k\Omega$  as given below in [Table 9](#).

### 7.4.2 Slave mode (external clock)

In order to accept an external clock input the pin ROOSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in [Table 9](#).

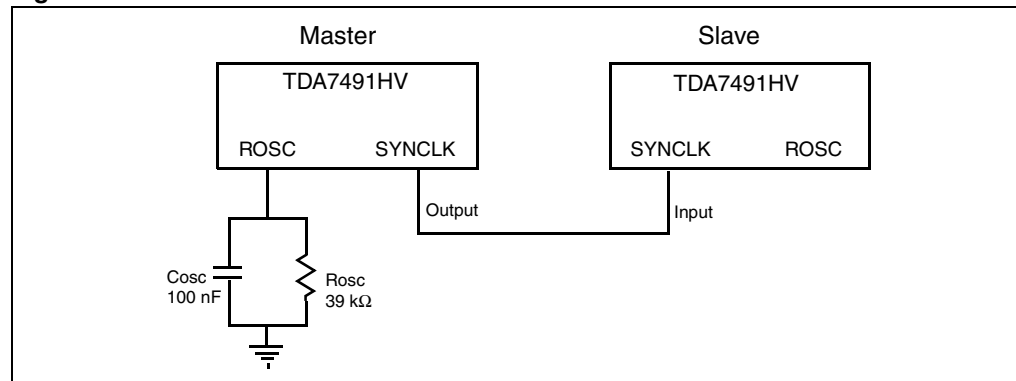
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

**Table 9. How to set up SYNCLK**

Mode	ROOSC	SYNCLK
Master	$R_{OSC} < 60 \text{ k}\Omega$	Output
Slave	Floating (not connected)	Input

**Figure 54. Master and slave connection**



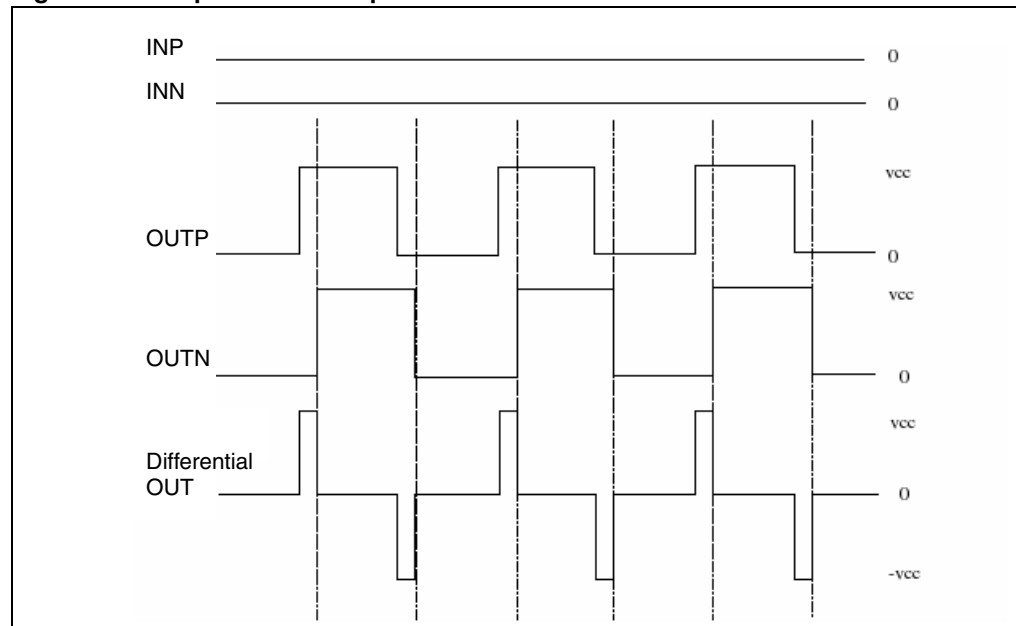
## 7.5 Filterless modulation

The output modulation scheme of the BTL is called unipolar pulse width modulation (PWM). The differential output voltages change between 0 V and  $+V_{CC}$  and between 0 V and  $-V_{CC}$ . This is in contrast to the traditional bipolar PWM outputs which change between  $+V_{CC}$  and  $-V_{CC}$ .

An advantage of this scheme is that it effectively doubles the switching frequency of the differential output waveform. The OUPN and OUTN are in the same phase when the input is zero, then the switching current is low and the loss in the load is small. In practice, a short delay is introduced between these two outputs in order to avoid the BTL output switching at the same time.

TDA7491HV can be used without a filter before the speaker, because the frequency of the TDA7491HV output is beyond the audio frequency, the audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

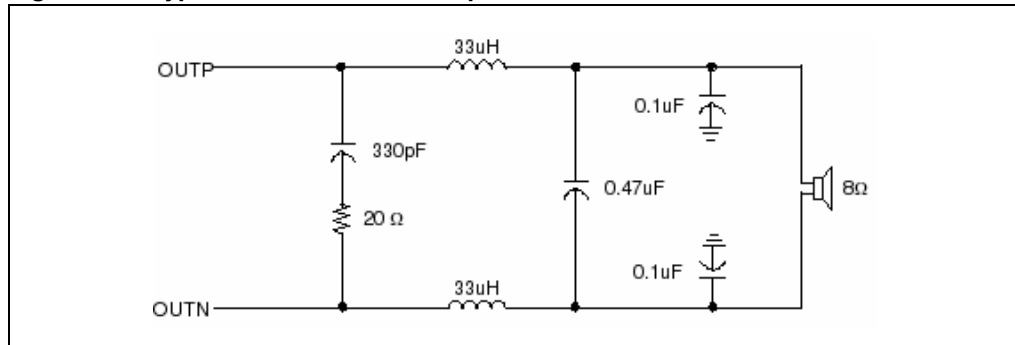
**Figure 55. Unipolar PWM output**



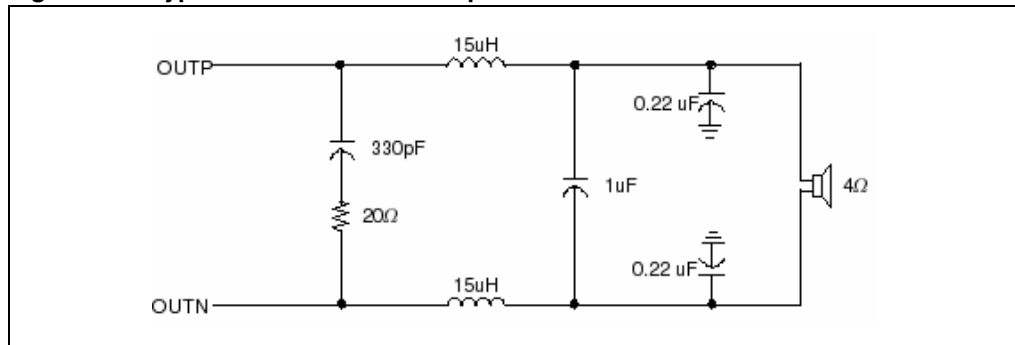
## 7.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in [Figure 56](#) and [Figure 57](#) below.

**Figure 56. Typical LC filter for a 8-Ω speaker**



**Figure 57. Typical LC filter for a 4-Ω speaker**



## 7.7 Protection function

The TDA7491HV is fully protected against overvoltages, undervoltages, overcurrents and thermal overloads as explained here.

### Overvoltage protection (OVP)

If the supply voltage exceeds the value for  $V_{OVP}$  given in [Table 5: Electrical specifications on page 10](#) the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage drops to below the threshold value the device restarts.

### Undervoltage protection (UVP)

If the supply voltage drops below the value for  $V_{UVP}$  given in [Table 5: Electrical specifications on page 10](#) the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers the device restarts.

### Overcurrent protection (OCP)

If the output current exceeds the value for  $I_{OCP}$  given in [Table 5: Electrical specifications on page 10](#) the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time,  $T_{OC}$ , is determined by the R-C components connected to pin STBY.

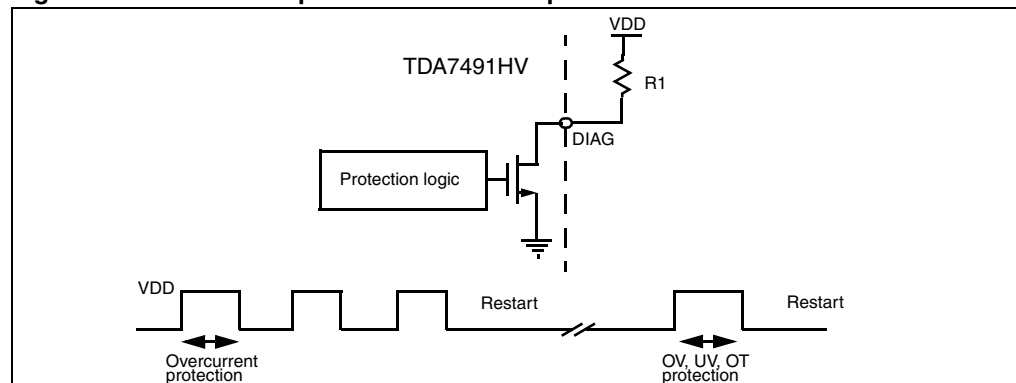
### Thermal protection (OTP)

If the junction temperature,  $T_j$ , reaches 145 °C (nominal), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature reaches the value for  $T_j$ , given in [Table 5: Electrical specifications on page 10](#) the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

## 7.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (<18 V) by a pull-up resistor whose value is limited by the maximum sinking current (200  $\mu$ A) of the pin.

**Figure 58. Behavior of pin DIAG for various protection conditions**



## 7.9 Heatsink requirements

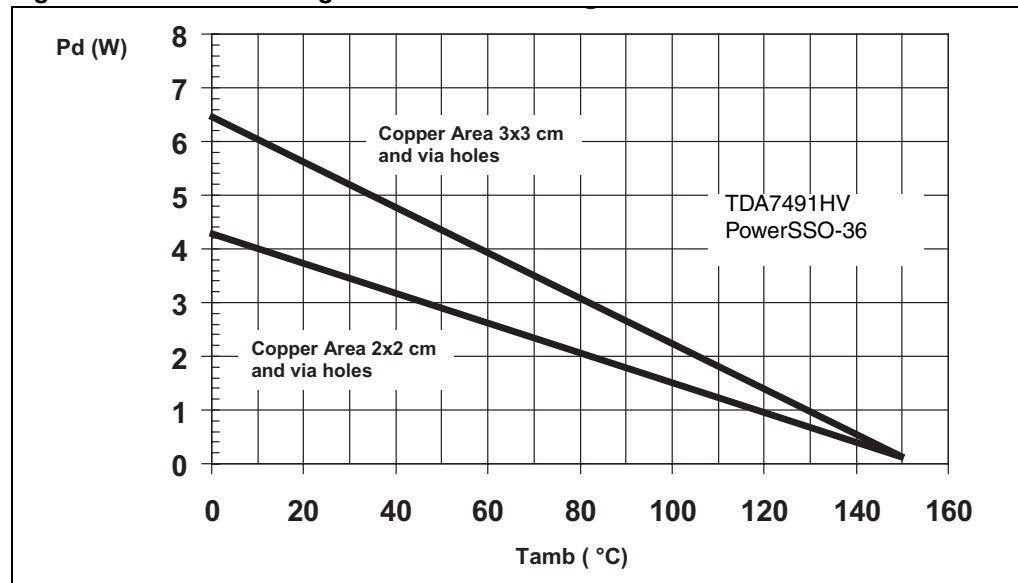
A thermal resistance of 24 °C/W can be obtained using the PCB copper ground layer with 16 vias connecting it to the contact area for the exposed pad. Ensure that the copper ground area is a nominal 9 cm<sup>2</sup> for 24 °C/W.

*Figure 59* shows the derating curves for copper areas of 4 cm<sup>2</sup> and 9 cm<sup>2</sup>.

As with most amplifiers, the power dissipated within the device depends primarily on the supply voltage, the load impedance and the output modulation level.

The maximum estimated power dissipation for the TDA7491HV is less than 4 W. When properly mounted on the above PCB the junction temperature could increase by 96 °C. However, with a musical program the dissipated power is about 40% less than this, leading to a temperature increase of around 60 °C. So even at the maximum recommended ambient temperature for consumer applications there is still a margin of safety before the maximum junction temperature is reached.

**Figure 59. Power derating curves for PCB used as heatsink**



## 8 Revision history

Table 10. Document revision history

Date	Revision	Changes
02-Jul-2007	1	Initial release.
03-Oct-2008	2	Updated AMR table Updated <a href="#">Chapter 4: Characterization curves on page 12</a> Added <a href="#">Figure 48: Test board (TDA7491HV) layout on page 29</a> Updated <a href="#">Figure 49: PowerSSO-36 EPD outline drawing on page 30</a> and <a href="#">Table 6: PowerSSO-36 EPD dimensions on page 31</a> Updated <a href="#">Figure 50: Applications circuit for class-D amplifier on page 32</a>
29-Jun-2009	3	Updated text concerning oscillator R and C in <a href="#">Section 3.3: Electrical specifications on page 10</a> Updated VOVP minimum value, added VUVP maximum value, updated STBY and MUTE voltages in <a href="#">Table 5: Electrical specifications on page 10</a> Updated equation for $f_{sw}$ <a href="#">on page 11</a> and <a href="#">on page 35</a> Updated <a href="#">Figure 50: Applications circuit for class-D amplifier on page 32</a>
03-Sep-2009	4	Added text for exposed pad in <a href="#">Figure 2 on page 8</a> Added text for exposed pad in <a href="#">Table 2 on page 9</a> Updated exposed pad Y (Min) dimension in <a href="#">Table 6 on page 31</a> Updated supply voltage for pin DIAG pull-up resistor in <a href="#">Section 7.8 on page 38</a> .



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