1/4-Inch System-On-A-Chip (SOC) VGA NTSC and PAL CMOS Digital Image Sensor

MT9V125

For the latest data sheet, refer to Micron's Web site: www.micron.com/imaging

Features

- Micron® DigitalClarity® CMOS imaging technology
- Superior low-light performance
- System-on-a-chip (SOC)—completely integrated camera system
- Supports use of external devices for addition of custom overlay graphics
- NTSC/PAL (true two-field) analog composite video output
- ITU-R BT.656 parallel output (8-bit, interlaced)
- Simultaneous composite and digital video outputs Serial LVDS data output
- Image flow processor (IFP) for sophisticated processing
- Color recovery and correction, sharpening, gamma, lens shading correction, and on-the-fly defect correction
- Automatic features:
- auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, and auto defect identification and correction
- Simple two-wire serial programming interface
- Low power, interlaced scan CMOS image sensor

Applications

- Automotive
  - Rear view camera
  - Side mirror replacement
  - Blind spot view
  - Occupant monitoring

Data Sheet Applicable to Silicon Revision: Rev4

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/4-inch (4:3)
Active imager size		3.63mm(H) x 2.78mm(V) 4.57mm diagonal
Active pixels		640H x 480V
NTSC output		720H x 486V
PAL output		720H x 576V
Pixel size		5.6µm x 5.6µm
Color filter array		RGB paired Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ master clock		13.5 Mp/s, 27 MHz
Frame rate – VGA (640H x 480V)		30 fps at 27 MHz (NTSC) 25 fps at 27 MHz (PAL)
Integration time (composite video)		16µs–33ms (NTSC) 16µs–40ms (PAL)
ADC resolution		10-bit, on-chip
Responsivity		5 V/lux-s (550nm)
Pixel dynamic range		70dB
SNR_{MAX}		39dB
Supply voltage	I/O digital	2.5–3.1V (2.8V nominal)
	Core digital	2.5–3.1V (2.8V nominal)
	Analog	2.5–3.1V (2.8V nominal)
Power consumption	Operating	320mW
	Standby	0.56mW
Operating temperature		–40°C to +105°C
Packaging		52-ball iBGA

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9V125IA7XTC	52-Ball iBGA (Pb-free)
MT9V125I77XTC	52-Ball iBGA
MT9V125D00XTC K12BC1	Bare die
MT9V125IA7XTCD ES	Demo kit (Pb-free)
MT9V125IA7XTCH ES	Headboard (Pb-free)
MT9V125IA7XTCR ES	Reference camera (Pb-free)

General Description

The MT9V125 is a VGA CMOS image sensor featuring Micron's breakthrough DigitalClarity technology—a low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, low power, and integration advantages of CMOS.

The MT9V125 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction.

The MT9V125 outputs interlaced-scan images at 30 or 25 fps, supporting both NTSC and PAL video formats.

The MT9V125 also includes digital video output that can be switched to the NTSC/PAL encoder. This can be used in conjunction with an external digital signal processor (DSP) to provide an overlay (such as a steering aid) on top of the live video.

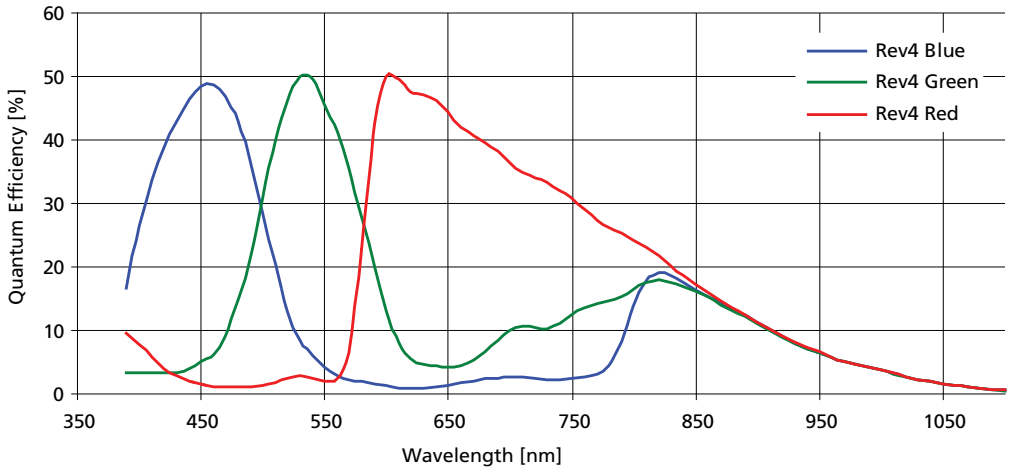
The image data can be output on any one of three output ports:

- Composite analog video (single-ended and differential support)
- Low-voltage differential signaling (LVDS)
- CCIR 656 interlaced digital video in parallel 8-bit format

Table 3: MT9V125 Detailed Performance Parameters

Parameter	Value
Effective fill factor (with microlens)	TBD
Output gain	28 e-/LSB
Read noise	6 e-RMS at 16X
Dark current	119 e-/pix/s at 55°C

Figure 1: Quantum Efficiency vs. Wavelength



Functional Overview

The MT9V125 is a fully-automatic, single-chip camera, requiring only a single power supply, lens, and clock source for basic operation. Output video is streamed via the chosen output port. The MT9V125 internal registers are configured using a two-wire serial interface.

The device can be put into a low-power sleep mode by asserting STANDBY and shutting down the clock. Output signals can be tri-stated. Both tri-stating output signals and entry into standby mode can be achieved via two-wire serial interface register writes.

The MT9V125 requires an input clock of 27 MHz to support correct NTSC or PAL timing.

Internal Architecture

Internally, the MT9V125 consists of a sensor core and an image flow processor (IFP). The IFP is divided in two sections, the color pipe and the camera controller. The sensor core captures raw images that are then input into the IFP. The color pipe section processes the incoming stream to create interpolated, color-corrected output, and the camera controller section controls the sensor core to maintain the desired exposure and color balance.

The IFP scales the image and an integrated video encoder generates either NTSC or PAL analog composite output. The MT9V125 supports three different output ports; analog composite video out, LVDS serial out and CCIR 656 interlaced digital video in parallel 8-bit format.

Figure 2 shows the major functional blocks of the MT9V125. The built-in NTSC/PAL encoder and the LVDS formatter allow simultaneous outputs of composite and digital video signals.

Figure 2: Functional Block Diagram

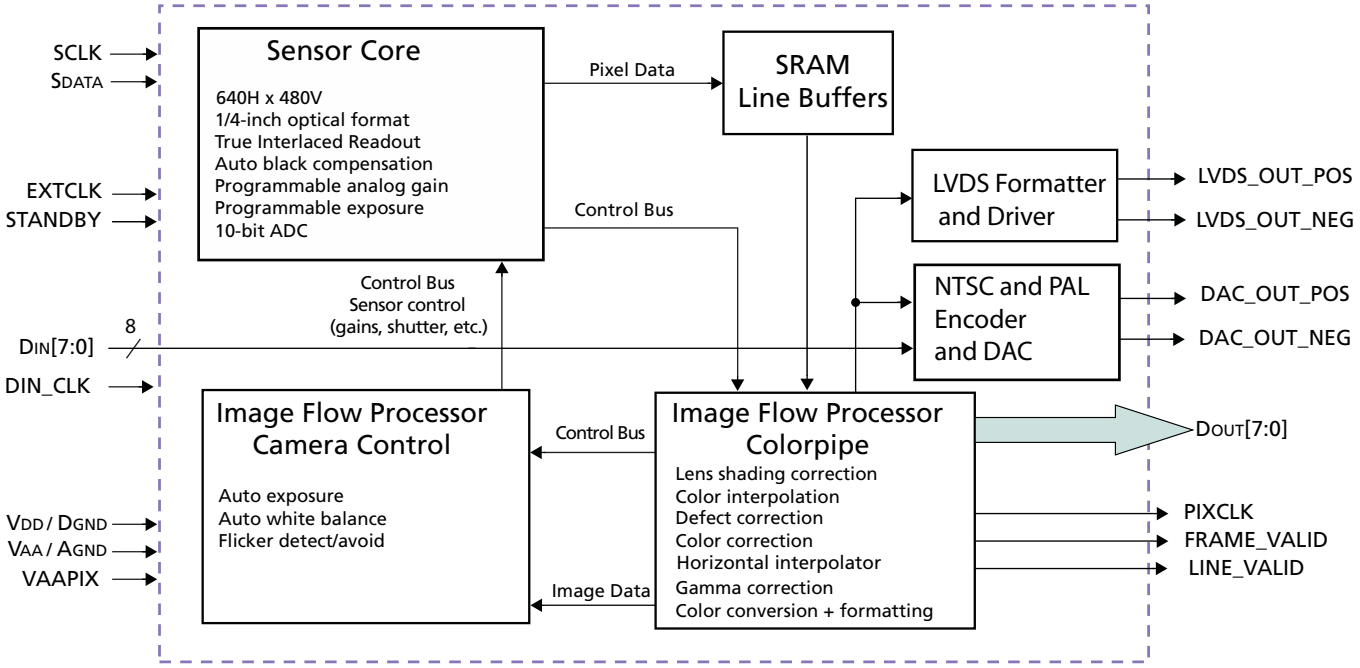
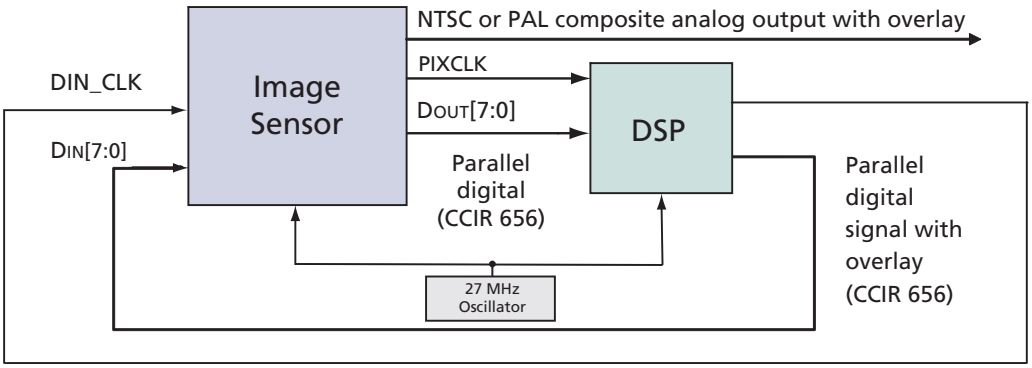


Figure 3 shows a typical application using a DSP to produce a video overlay (such as a steering aid). The parallel digital video output is sent to the DSP, which adds the overlay. The digital video with the overlay is then looped back into the MT9V125 to the NTSC/ PAL encoder and LVDS formatter to provide simultaneous composite analog and digital LVDS outputs.

Figure 3: Typical Usage Configuration with Overlay



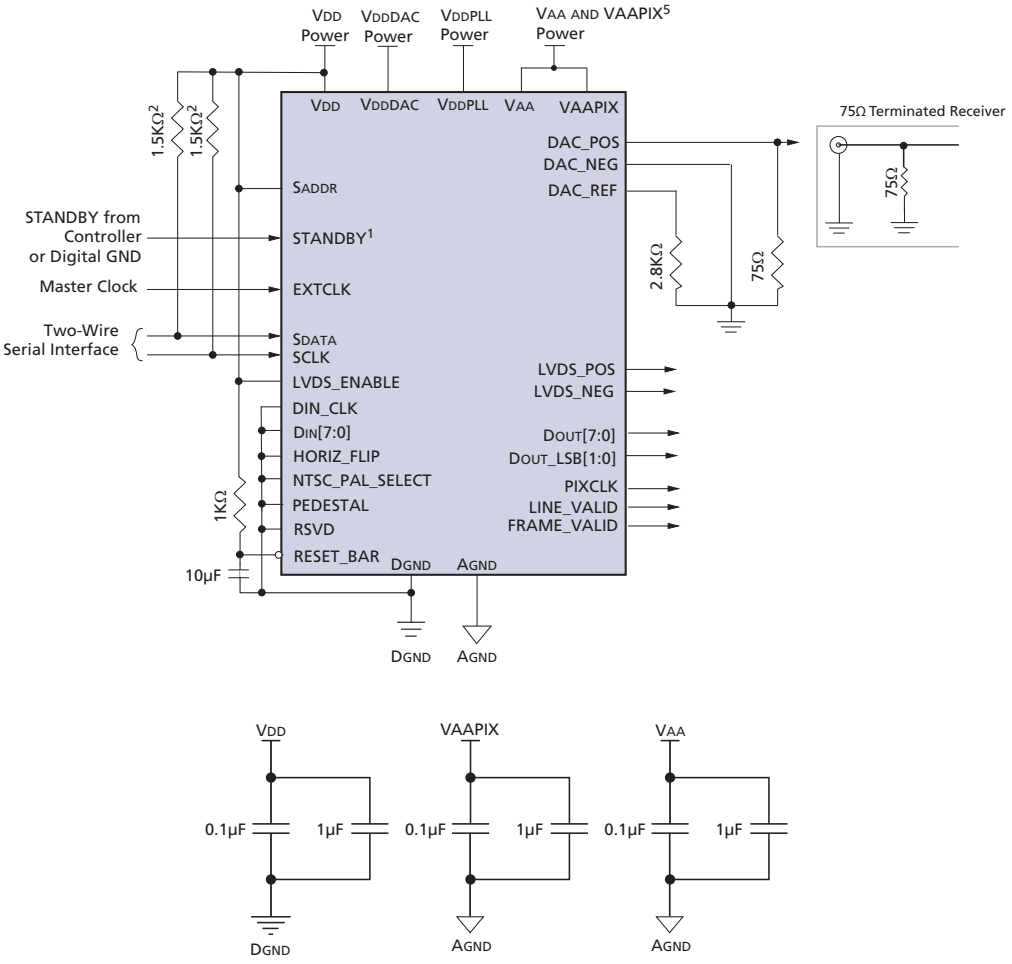
Typical Connections

Figure 4 shows a detailed MT9V125 device configuration. For low-noise operation, the MT9V125 requires separate analog and digital power supplies. Incoming digital and analog ground conductors can be tied together next to the die.

Power supply voltages VAA (the primary analog voltage) and VAAPIX (the main voltage to the pixel array) should be decoupled separately.

The MT9V125 requires a single external voltage supply level.

Figure 4: Typical Configuration (without use of overlay)

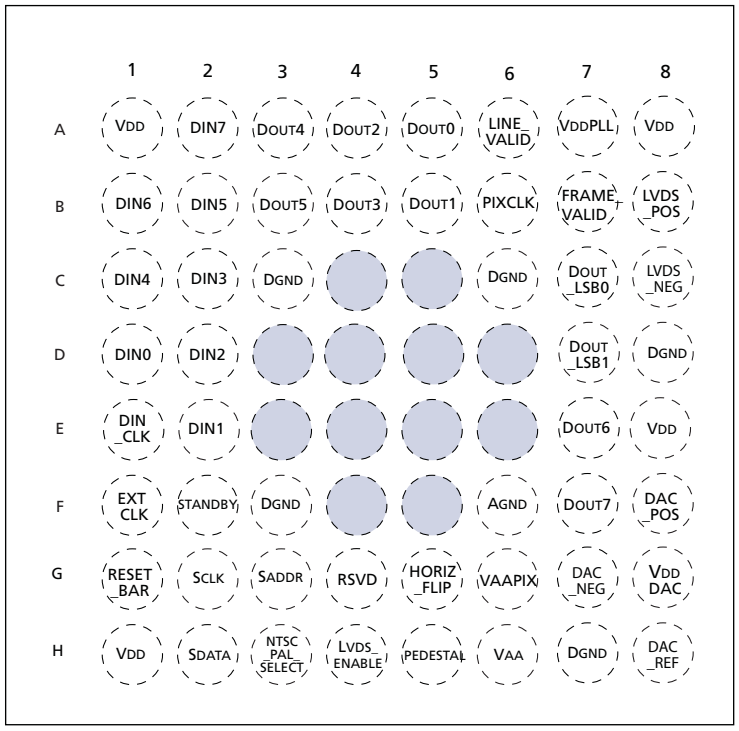


Notes:
1. MT9V125 STANDBY can be connected directly to the customer's ASIC controller or to DGND, depending on the controller's capability.
2. A 1.5KΩ resistor value is recommended, but may be greater for slower (for example, 100Kb) two-wire speed.
3. LVDS_ENABLE must be tied HIGH if LVDS is to be used.
4. Pull down DAC_REF with a 2.8KΩ resistor for 1.0V peak-to-peak video output. For a 1.4V peak-to-peak video output, change the resistor to 2.4KΩ.
5. VAA and VAAPIX must be tied to the same potential for proper operation.

Ball Assignments

Figure 5 shows the location of the balls and their corresponding signals on the MT9V125. The 12 balls in the middle of the package are unconnected.

Figure 5: 52-Ball iBGA Assignment



Top View
(Ball Down)

Table 4: Ball Descriptions

Ball Assignment	Name	Type	Description
F1	EXTCLK	Input	Master clock in sensor.
G1	RESET_BAR	Input	Active LOW: asynchronous reset.
G3	SADDR	Input	Two-wire serial interface device ID selection 1:0xBA, 0:0x90.
G4	RSVD	Input	Must be attached to DGND. G4
G2	SCLK	Input	Two-wire serial interface clock.
F2	STANDBY	Input	Multifunctional signal to control device addressing, power-down, and state functions (covering output enable function).
G5	HORIZ_FLIP	Input	If “0” at reset: Default horizontal setting. If “1” at reset: Flips the image readout format in the horizontal direction.
H3	NTSC_PAL_SELECT	Input	If “0” at reset: Default NTSC mode. If “1” at reset: Default PAL mode.
H5	PEDESTAL	Input	If “0” at reset: Does not add pedestal to composite video output. If “1” at reset: Adds pedestal to composite video output. Valid for NTSC only, pull LOW for PAL operation.

Table 4: Ball Descriptions (continued)

Ball Assignment	Name	Type	Description
H4	LVDS_ENABLE	Input	Active HIGH: Enables the LVDS output port. Must be HIGH if LVDS is to be used.
A2, B1, B2, C1, C2, D2, E2, D1	DIN[7:0]	Input	External data input port selectable at video encoder input.
E1	DIN_CLK	Input	DIN capture clock. (This clock must be synchronous to EXTCLK.)
H2	SDATA	Output	Two-wire serial interface data I/O.
F7, E7, B3, A3, B4, A4, B5, A5	DOUT[7:0]	Output	Pixel data output DOUT7 (most significant bit [MSB]), DOUT0 (least significant bit [LSB]). Data output [9:2] in sensor stand-alone mode
C7	DOUT_LSB0	Output	Sensor stand-alone mode output 0—typically left unconnected for normal SOC operation.
D7	DOUT_LSB1	Output	Sensor stand-alone mode output 1—typically left unconnected for normal SOC operation.
B7	FRAME_VALID	Output	Active HIGH: FRAME_VALID (FV); indicates active frame.
A6	LINE_VALID	Output	Active HIGH: LINE_VALID (LV); indicates active pixel.
B6	PIXCLK	Output	Pixel clock output.
F8	DAC_POS	Output	Positive video DAC output in differential mode. Video DAC output in single-ended mode.
G7	DAC_NEG	Output	Negative video DAC output in differential mode. Tie to GND in single-ended mode.
H8	DAC_REF	Output	External reference resistor for video DAC.
B8	LVDS_POS	Output	LVDS positive output.
C8	LVDS_NEG	Output	LVDS negative output.
F6	AGND	Supply	Analog ground.
D8, C3, C6, F3, H7	DGND	Supply	Digital ground.
H6	VAA	Supply	Analog power: 2.5–3.1V (2.8V nominal).
G6	VAAPIX	Supply	Pixel array analog power supply: 2.5–3.1V (2.8V nominal).
A1, A8, E8 ,H1	VDD	Supply	Digital power: 2.5–3.1V (2.8V nominal).
G8	VDDDAC	Supply	DAC power: 2.5–3.1V (2.8V nominal).
A7	VDDPLL	Supply	LVDS PLL power: 2.5–3.1V (2.8V nominal).

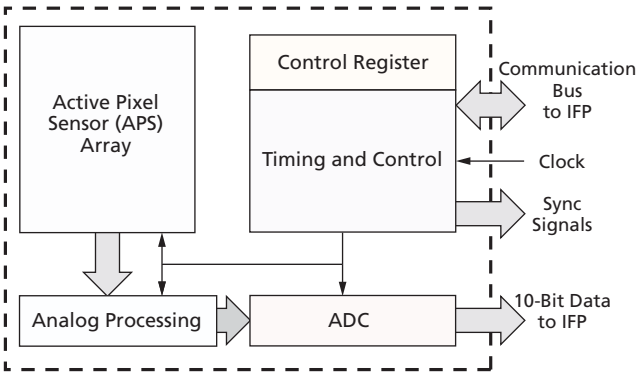
Notes:
1. ALL power pins (VDD/VDDDAC/VDDPLL/VAA/VAAPIX) must be connected to 2.8V (nominal). Power pins cannot be floated.
2. ALL ground pins (AGND/DGND) must be connected to ground. Ground pins cannot be floated.
3. Inputs are not tolerant to signal voltages above 3.1V.
4. All unused inputs must be tied to GND or VDD.
5. VAA and VAAPIX must be tied to the same potential for proper operation.

Detailed Architecture Overview

Sensor Core

The sensor consists of a pixel array of 695 x 512, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control, as illustrated in Figure 6.

Figure 6: Sensor Core Block Diagram

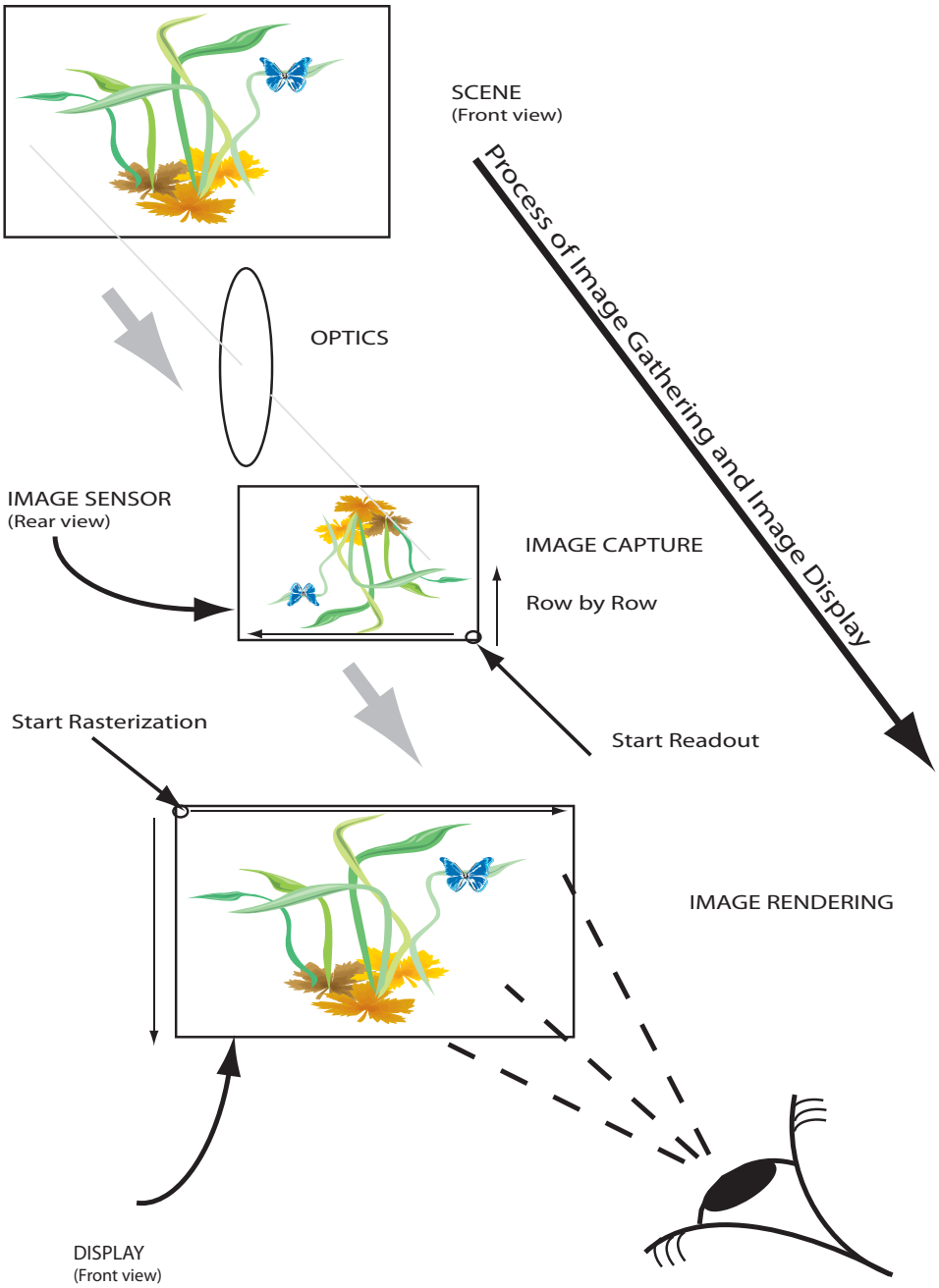


There are 649 columns by 498 rows of optically-active pixels that include a pixel boundary around the VGA (640 x 480) image to avoid boundary effects during color interpolation and correction.

The one additional active column and two additional active rows are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

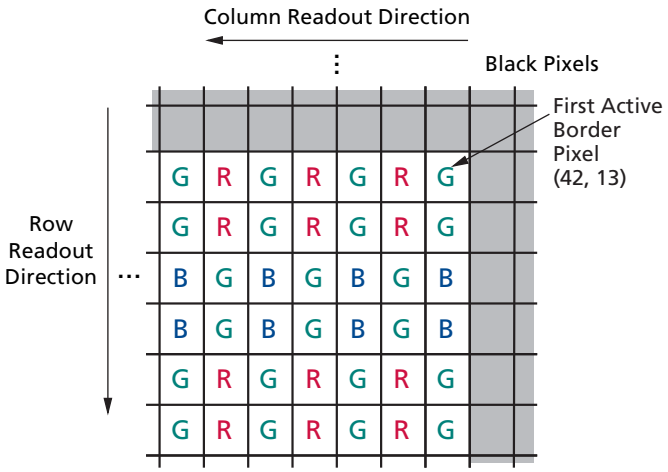
Figure 7 on page 9 illustrates the process of capturing the image. The original scene is flipped and mirrored by the sensor optics. Sensor readout starts at the lower right hand corner. The image is presented in true orientation by the output display.

Figure 7: Image Capture Example



The sensor core uses a paired RGB Bayer color pattern, as shown in Figure 8 on page 10. Row pairs consist of the following: rows 0, 1, rows 2, 3, rows 4, 5, etc. The even-numbered row pairs (0/1, 4/5, and so on) in the active array contain green and red color pixels. The odd-numbered row pairs (2/3, 6/7, and so on) contain blue and green color pixels. The odd-numbered columns contain green and blue color pixels; even-numbered columns contain red and green color pixels.

Figure 8: Pixel Color Pattern Detail (top right corner)



Output Data Format

The sensor core image data is read out in an interlaced scan order. Progressive readout—which is not supported by the color pipe—is an option, but is only intended for raw data output. Valid image data is surrounded by horizontal and vertical blanking, shown in Figure 9 on page 11.

For NTSC output, the horizontal size is stretched from 640 to 720 pixels. The vertical size is 243 pixels per field; tom of the image field.

For PAL output, the horizontal size is also stretched from 640 to 720 pixels. The vertical size is 288 pixels per field—240 image pixels with 24 dark pixels at the top of the image and 24 dark pixels at the bottom of the image field.

Figure 9: Spatial Illustration of Image Readout

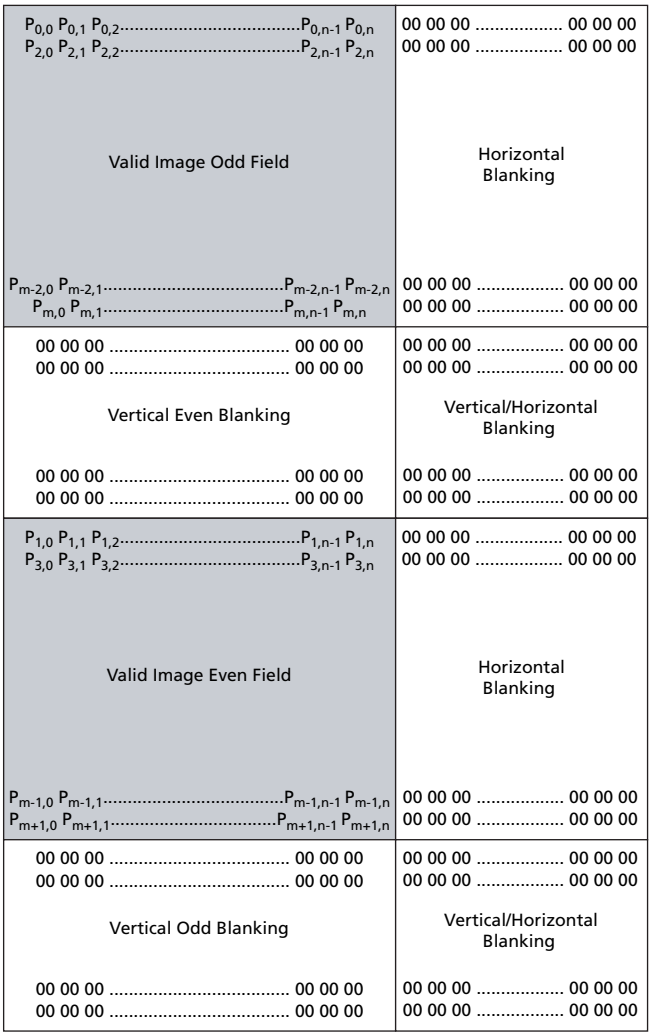


Image Flow Processor

The MT9V125 IFP consists of a color processing pipeline, and a measurement and control logic block (the camera controller). The stream of raw data from the sensor enters the pipeline and undergoes several transformations. Image stream processing starts with conditioning the black level and applying a digital gain. The lens shading block compensates for signal loss caused by the lens.

Next, the data is interpolated to recover missing color components for each pixel. The resulting interpolated RGB data passes through the current color correction matrix (CCM) as well as the gamma and saturation corrections, and is formatted for final output.

The measurement and control logic continuously accumulate image brightness and color statistics. Based on these measurements, the IFP calculates updated values for exposure time and sensor analog gains that are sent to the sensor core through the control bus.

Black Level Conditioning

The sensor core black level calibration works to maintain black pixel values at a constant level, independent of analog gain, reference current, voltage settings, and temperature conditions. If this black level is above zero, it must be reduced before color processing can begin. The black level subtraction block in the IFP re-maps the black level of the sensor to zero prior to lens shading correction. Following lens shading correction, the black level addition block provides capability for another black level adjustment. However, for good contrast, this level should be set to zero.

Digital Gain

Controlled by auto exposure logic, the input digital gain stage amplifies the raw image in low-light conditions (range: x1–x8).

Test Pattern

A built-in test pattern generator produces a test image stream that can be multiplexed with the gain stage. The test pattern can be selected through register settings.

Lens Shading Correction

Inexpensive lenses tend to attenuate image intensity near the edges of pixel arrays. Other factors also cause signal and coloration differences across the image. The net result of all these factors is known as lens shading. Lens shading correction (LC) compensates for these differences.

Typically, the profile of lens-shading-induced anomalies across the frame is different for each color component. Therefore, lens shading correction is independently calibrated for the color channels.

Interpolation and Aperture Correction

A demosaic engine converts the single-color-per-pixel Bayer data from the sensor into RGB (10-bit per color channel). The demosaic algorithm analyzes neighboring pixels to generate a best guess for the missing color components. Edge sharpness is preserved as much as possible.

Aperture correction sharpens the image by an adjustable amount. To avoid amplifying noise, sharpening can be programmed to phase out as light levels drop.

Defect Correction

This device supports 2D defect correction. In 2D defect detection/correction, pixels with values different from their neighbors by greater than a defined threshold are considered defects unless near the image boundary. The approach is termed 2D, as pixels on neighboring lines as well as neighboring pixels on the same line are considered in both detection and correction.

Color Correction

To obtain good color rendition and saturation, it is necessary to compensate for the differences between the spectral characteristics of the imager color filter array and the spectral response of the human eye. This compensation, also known as color separation, is achieved through linear transformation of the image with a 3 x 3 element color correction matrix. The optimal values for the color correction coefficients depend on the spectra of the incident illumination and can be programmed by the user.

Color Saturation Control

Both color saturation and sharpness enhancement can be set by the user, or adjusted automatically by tracking the magnitude of the gains used by the auto exposure algorithm.

Automatic White Balance

The MT9V125 has a built-in automatic white balance (AWB) algorithm designed to compensate for the effects of changing scene illumination the color rendition quality. This sophisticated algorithm consists of three major sub-modules:

- A measurement engine (ME) performing statistical analysis of the image
- A module selecting the optimal color correction matrix
- A module selecting analog color channel gains in the sensor core

While the default algorithm settings are adequate in most situations, the user can reprogram base color correction matrices and limit color channel gains. The AWB does not attempt to locate the brightest or grayest elements in the image; it performs in-depth image analysis to differentiate between changes in predominant spectra of illumination and changes in predominant scene colors. Factory defaults are suitable for most applications, however, a wide range of algorithm parameters can be overwritten by the user through the serial interface.

Auto Exposure

The auto exposure (AE) algorithm performs automatic adjustments to image brightness by controlling exposure time and analog gains in the sensor core, as well as digital gain applied to the image. The algorithm relies on the auto exposure measurement engine that tracks speed and amplitude changes in the overall luminance of selected windows in the image.

Backlight compensation is achieved by weighting the luminance in the center of the image higher than the luminance on the periphery. Other algorithm features include: fast-fluctuating illumination rejection (time averaging), response-speed control, and controlled sensitivity to small changes.

While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters as described above. The auto exposure algorithm enables compensation for a broad range of illumination intensities.

Automatic Flicker Abatement

Flicker occurs when integration time is not an integer multiple of the period of the light intensity. The automatic flicker abatement block eliminates flicker by limiting exposure times to integer multiples of the light period.

Gamma Correction

To achieve more life-like quality in an image, the IFP includes gamma correction and color saturation control. Gamma correction operates on the luminance component of the image and enables compensation for non-linear dependence of the display device output versus the driving signal (e.g., monitor brightness versus CRT voltage).

In addition, gamma correction provides range compression, converting 10-bit luminance input to 8-bit output. Pre-gamma image processing generates 10-bit luminance values ranging from 0 to 896. Piece-wise linear gamma correction utilized in this imager has ten linear intervals, with end points corresponding to the following input values:

Xi = 0…10 = {0, 16, 32, 64, 128, 256, 384, 512, 640, 768, 896}.

For each input value *Xi*, the user can program the corresponding output value *Yi*. *Yi* values must be monotonically increasing.

NTSC/PAL Encoder

The MT9V125 has an on-chip video encoder to format the data stream for composite video output in the supported NTSC or PAL formats. The encoder expects CCIR-656 interlaced NTSC or PAL data stream input. By default, the input is taken from the on-chip image stream. Input can also be taken from the external DIN port for external image processing used with the on-chip video encoder and composite output.

I/O Timing

Digital Output

By default, the MT9V135 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. The expectation is that the user captures data, FV, and LV using the rising edge of PIXCLK. The timing diagram is shown in Figure 10.

As an option, the polarity of the PIXCLK can be inverted from the default. This is achieved by programming R155:1[9] to "0."

Figure 10: Digital Output I/O Timing

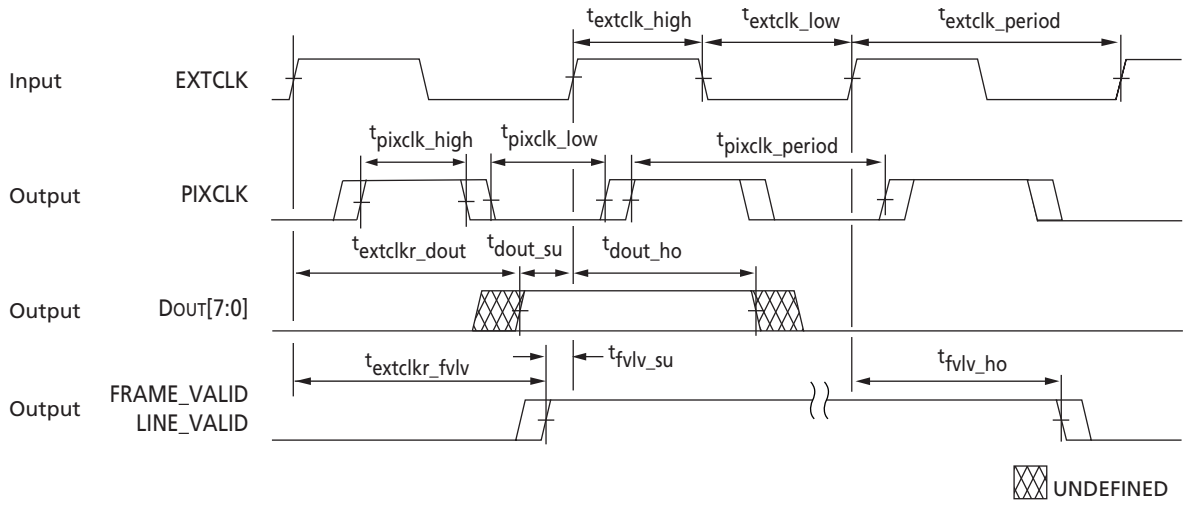


Table 5: Digital Output I/O Timing
T_A = Ambient = 25°C; VDD = 2.5–3.1V

Signal	Parameter	Condition	Minimum	Typical	Maximum	Unit
EXTCLK	t_{extclk_high}		17	–	20	ns
	t_{extclk_low}		17	–	20	ns
	t_{extclk_period}		–	37.0	–	ns
	f_{extclk}	max +/- 100 ppm		27		MHz
PIXCLK[1]	t_{pixclk_low}		14	–	22	ns
	t_{pixclk_high}		14	–	22	ns
	t_{pixclk_period}		36.7	37	37.4	ns
DATA[7:0]	$t_{extclkr\_dout}$		8	14	18	ns
	t_{dout_su}		14	18.5	23	ns
	t_{dout_ho}		14	18.5	23	ns
FV/LV	$t_{extclkr\_fvlv}$		8	14	18	ns
	t_{fvlv_su}		14	18.5	23	ns
	t_{fvlv_ho}		14	18.5	23	ns

Notes: 1. PIXCLK may be inverted by programming register R155:1[9] = 0.

Electrical Specifications

Table 6: Electrical Characteristics and Operating Conditions
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter[1]	Condition	Minimum	Typical	Maximum	Unit
I/O and core digital voltage (V_{DD})	n/a	2.5	2.8	3.1	V
LVDS PLL voltage	n/a	2.5	2.8	3.1	V
Video DAC voltage	n/a	2.5	2.8	3.1	V
Analog voltage (V_{AA})	n/a	2.5	2.8	3.1	V
Pixel supply voltage (V_{AAPIX})	n/a	2.5	2.8	3.1	V
Leakage current	STANDBY, EXTCLK: HIGH or LOW			10	µA
Imager operating temperature	n/a	–40		+85	°C
Functional operating temperature	n/a	–40		+105	°C
Storage temperature	n/a	–40		+125	°C

Notes: 1. V_{DD}, V_{AA}, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.

Table 7: Video DAC Electrical Characteristics
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter	Condition	Minimum	Typical	Maximum	Unit
Resolution		–	10	–	bits
DNL	Single-ended mode	–	0.8	1.1	bits
INL	Single-ended mode	–	5.7	8.1	bits
Output local oad	Single-ended mode, output pad (DAC_POS)	–	75	–	Ω
	Single-ended mode, unused output (DAC_NEG)	–	0	–	Ω
Output voltage	Single-ended mode, code 000h	–	0.02	–	V
	Single-ended mode, code 3FFh	–	1.42	–	V
Output current	Single-ended mode, code 000h	–	0.6	–	mA
	Single-ended mode, code 3FFh	–	37.9	–	mA
DNL	Differential mode	–	0.7	1	bits
INL	Differential mode	–	1.4	3	bits
Output local load	Differential mode per pad (DAC_POS and DAC_NEG)	–	37.5	–	Ω
Output voltage	Differential mode, code 000h, pad dacp	–	0.37	–	V
	Differential mode, code 000h, pad dacn	–	1.07	–	V
	Differential mode, code 3FFh, pad dacp	–	1.07	–	V
	Differential mode, code 3FFH, pad dacn	–	0.37	–	V
Output voltage	Differential mode, code 000h, pad dacp	–	0.6	–	mA
	Differential mode, code 000h, pad dacn	–	37.9	–	mA
	Differential mode, code 3FFh, pad dacp	–	37.9	–	mA
	Differential mode, code 3FFH, pad dacn	–	0.6	–	mA
Differential output, mid level	Differential mode	–	0.72	–	V
Supply current	Estimate	–	–	55	mA

Table 8: Digital I/O Parameters
T_A = Ambient = 25°C; All supplies at 2.8V

Signal Type	Parameter	Definition	Condition	Minimum	Typical	Maximum	Unit
All Outputs		Load capacitance		1	–	30	pF
		Output signal slew	2.8V, 30pF load	–	0.72	–	V/ns
			2.8V, 5pF load	–	1.25	–	V/ns
	V_{OH}	Output high voltage		2.5	2.8	3.1	V
	V_{OL}	Output low voltage		–0.3	–	0.3	V
	I_{OH}	Output high current	V_{DD} = 2.8V, V_{OH} = 2.4V	16	–	26.5	mA
	I_{OL}	Output low current	V_{DD} = 2.8V, V_{OL} = 0.4V	15.9	–	21.3	mA
All Inputs	V_{IH}	Input high voltage	V_{DD} = 2.8V	1.48	–	–	V
	V_{IL}	Input low voltage	V_{DD} = 2.8V	–	–	1.43	V
	I_{IN}	Input leakage current		–2	–	2	µA
	Signal CAP	Input signal capacitance		–	3.5	–	pF

Power Consumption

Table 9: Power Consumption
T_A = Ambient = 25°C; All supplies at 2.8V

Mode	Sensor (mW)	Image Flow Processor (mW)	I/Os (mW)[1]	DAC (mW)	LVDS (mW)	Total (mW)
Active mode [2]	60	100	10	150	80	400
Standby						0.56

Notes: 1. 10pF nominal.
2. (NTSC or PAL) and LVDS should not be operated at the same time.

NTSC Signal Parameters

Table 10: NTSC Signal Parameters

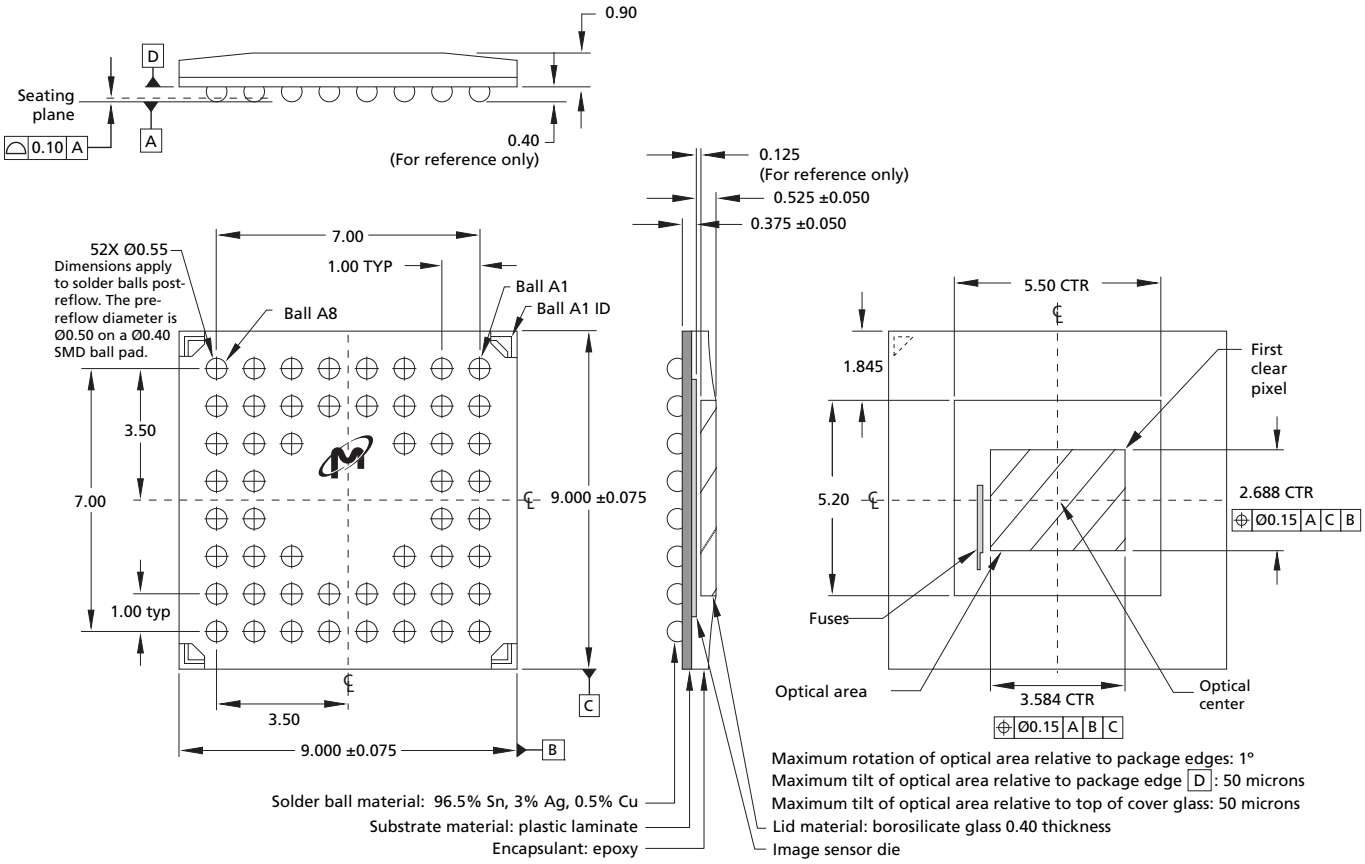
T_A = Ambient = 25°C; All supplies at 2.8V

Parameter	Condition	Minimum	Typical	Maximum	Unit	Notes
Line Frequency		15730	15735	15740	Hz	
Field Frequency		59.00	59.94	60.00	Hz	
Sync Rise Time		120	164	170	ns	
Sync Fall Time		120	167	170	ns	
Sync Width		4.60	4.74	4.80	µS	
Sync Level		37	39.9	43	IRE	2, 4
Burst Level		37	39.7	43	IRE	2, 4
Sync to Setup (with pedestal off)		9.10	9.40	9.40	µS	
Sync to Burst Start		5.00	5.31	5.60	µS	
Front Porch		1.40	1.40	1.60	µS	
Burst Width		8.0	8.5	10.0	cycles	
Black Level		6.5	7.5	8.5	IRE	1, 2, 4
White Level		90	100	110	IRE	1, 2, 3, 4

Notes:
1. Black and white levels are referenced to the blanking level.
2. NTSC convention standardized by the IRE (1 IRE = 7.14mV).
3. Encoder contrast setting R0x011 = R0x001 = 0.
4. DAC ref = 2.8kΩ, load = 37.5Ω

Package and Die Dimensions

Figure 11: 52-Ball iBGA Package Outline Drawing



Notes: 1. All dimensions in millimeters.

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