

ADVANCED LINEAR CHARGE MANAGEMENT IC FOR SINGLE- AND TWO-CELL LITHIUM-ION AND LITHIUM-POLYMER

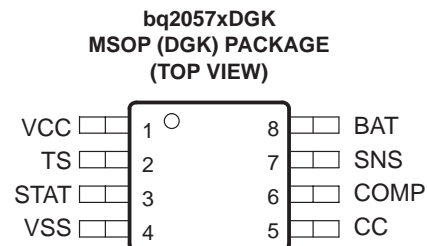
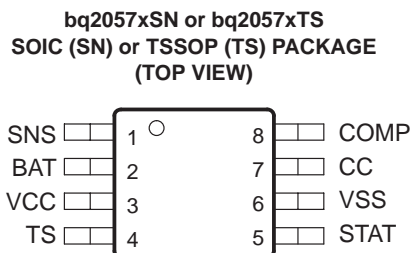
FEATURES

- Ideal for Single (4.1 V or 4.2 V) and Dual-Cell (8.2 V or 8.4 V) Li-Ion or Li-Pol Packs
- Requires Small Number of External Components
- 0.3 V Dropout Voltage for Minimizing Heat Dissipation
- Better Than $\pm 1\%$ Voltage Regulation Accuracy With Preset Voltages
- AutoComp™ Dynamic Compensation of Battery Pack's Internal Impedance to Reduce Charge Time
- Optional Cell-Temperature Monitoring Before and During Charge
- Integrated Voltage and Current Regulation With Programmable Charge-Current and High- or Low-Side Current Sensing
- Integrated Cell Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage Of Charge
- Charge Status Output for Single or Dual Led or Host Processor Interface
- Automatic Battery-Recharge Feature
- Charge Termination by Minimum Current
- Automatic Low-Power Sleep Mode When V_{CC} Is Removed
- EVMs Available for Quick Evaluation
- Packaging: 8-Pin SOIC, 8-Pin TSSOP, 8-Pin MSOP

DESCRIPTION

The BENCHMARK bq2057 series advanced Lithium-Ion (Li-Ion) and Lithium-Polymer (Li-Pol) linear charge-management ICs are designed for cost-sensitive and compact portable electronics. They combine high-accuracy current and voltage regulation, battery conditioning, temperature monitoring, charge termination, charge-status indication, and AutoComp charge-rate compensation in a single 8-pin IC. MSOP, TSSOP, and SOIC package options are offered to fit a wide range of end applications.

The bq2057 continuously measures battery temperature using an external thermistor. For safety, the bq2057 inhibits charge until the battery temperature is within user-defined thresholds. The bq2057 then charges the battery in three phases: conditioning, constant current, and constant voltage. If the battery voltage is below the low-voltage threshold, $V_{(min)}$, the bq2057 precharges using a low current to condition the battery. The conditioning charge rate is approximately 10% of the regulation current. The conditioning current also minimizes heat dissipation in the external pass-element during the initial stage of the charge. After conditioning, the bq2057 applies a constant current to the battery. An external sense-resistor sets the current. The sense-resistor can be on either the high or low side of the battery without additional components. The constant-current phase continues until the battery reaches the charge-regulation voltage.



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bq2057, bq2057C bq2057T, bq2057W

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DESCRIPTION (continued)

The bq2057 then begins the constant-voltage phase. The accuracy of the voltage regulation is better than $\pm 1\%$ over the operating-temperature and supply-voltage ranges. For single and dual cells, the bq2057 is offered in four fixed-voltage versions: 4.1 V, 4.2 V, 8.2 V, and 8.4 V. Charge stops when the current tapers to the charge termination threshold, $I_{(TERM)}$. The bq2057 automatically restarts the charge if the battery voltage falls below the $V_{(RCH)}$ threshold.

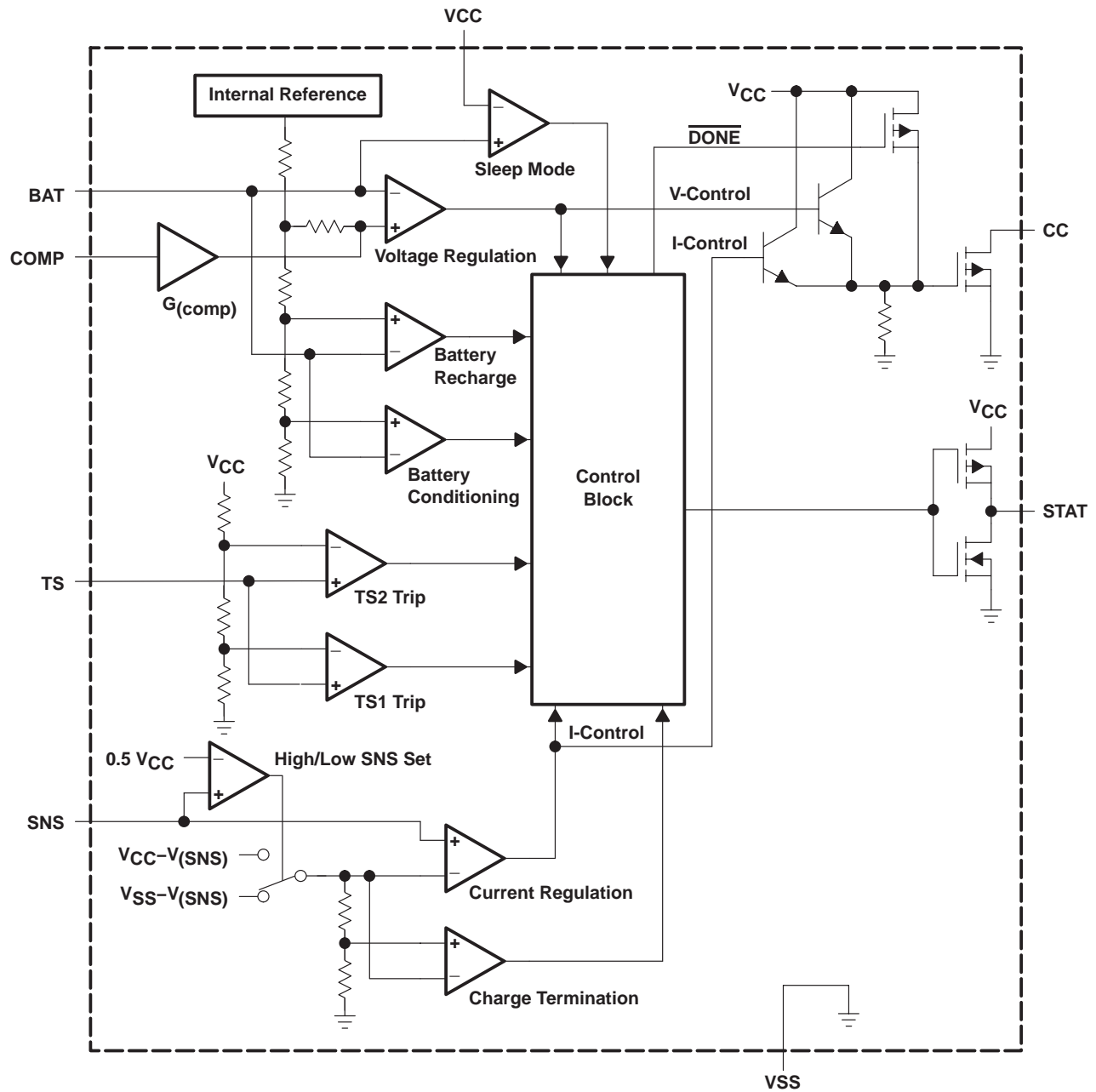
The designer also may use the AutoComp feature to reduce charging time. This proprietary technique allows safe and dynamic compensation for the internal impedance of the battery pack during charge.

AVAILABLE OPTIONS

| T _A | PACKAGE | | | |
|----------------|---------------------------|---------------|------------|---------------|
| | CHARGE REGULATION VOLTAGE | SOIC (SN) | TSSOP (TS) | MSOP† (DGK) |
| -20°C to 70°C | 4.1 V | Not available | bq2057TS | bq2057DGK |
| | 4.2 V | bq2057CSN | bq2057CTS | bq2057CDGK |
| | 8.2 V | Not available | bq2057TTS | Not available |
| | 8.4 V | bq2057WSN | bq2057WTS | |

† Note the difference in pinout for this package.

function block diagram



Terminal Functions

| TERMINAL | | | I/O | DESCRIPTION |
|----------|--------------------------|------------|-----|---|
| NAME | NO. | | | |
| | SOIC (SN) and TSSOP (TS) | MSOP (DGK) | | |
| BAT | 2 | 8 | I | Voltage sense input |
| CC | 7 | 5 | O | Charge control output |
| COMP | 8 | 6 | I | Charge-rate compensation input (AutoComp) |
| SNS | 1 | 7 | I | Current sense input |
| STAT | 5 | 3 | O | Charge status output |
| TS | 4 | 2 | I | Temperature sense input |
| VCC | 3 | 1 | I | Supply voltage |
| VSS | 6 | 4 | | Ground |

detailed description

current-sense input

Battery current is sensed via the voltage developed on this pin by an external sense resistor. The external resistor can be placed on either the high or low side of the battery. (See schematics for details.)

battery-voltage input

Voltage sense-input tied directly to the positive side of the battery.

temperature sense input

Input for an external battery-temperature monitoring circuit. Connecting this input to VCC/2 disables this feature.

charge-status output

3-state indication of charge in progress, charge complete, and temperature fault or sleep mode.

charge-control output

Source-follower output that drives an external pass-transistor (PNP or P-channel MOSFET) for current and voltage regulation.

charge-rate compensation input

Sets the charge-rate compensation level. The voltage-regulation output may be programmed to vary as a function of the charge current delivered to the battery.

supply voltage input

Power supply input and current reference for high-side sensing configuration.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|--------------------------|
| Supply voltage (V_{CC} with respect to GND) | -0.3 to +18 V |
| Input voltage, SNS, BAT, TS, COMP (all with respect to GND) | -0.3 V to $V_{CC}+0.3$ V |
| Sink current (STAT pin) not to exceed P_D | 20 mA |
| Source current (STAT pin) not to exceed P_D | 10 mA |
| Output current (CC pin) not to exceed P_D | 40 mA |
| Total power dissipation, P_D (at 25°C) | 300mW |
| Operating free-air temperature range, T_A | -20°C to 70°C |
| Storage temperature range, T_{stg} | -40°C to 125°C |
| Lead temperature (soldering, 10 s) | 300°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|---|--|
| DGK | 3.4 mW/°C | 424 mW | 271 mW |

recommended operating conditions

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| Supply voltage, V_{CC} | 4.5 | 15 | V |
| Operating free-air temperature range, T_A | -20 | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-------|------|-------|---------------|
| $I(V_{CC})$ V_{CC} Current | $V_{CC} > V_{CC(\text{min})}$, Excluding external loads | | 2 | 4 | mA |
| $I(V_{CCS})$ V_{CC} Sleep current | For bq2057 and bq2957C, $V(\text{BAT}) \geq V(\text{min})$, $V(\text{BAT}) - V_{CC} \geq 0.8$ V | | 3 | 6 | μA |
| | For bq2057T and bq2957W, $V(\text{BAT}) \geq V(\text{min})$, $V(\text{BAT}) - V_{CC} \geq 0.8$ V | | | 10 | |
| $I_{\text{B}}(\text{BAT})$ Input bias current on BAT pin | $V(\text{BAT}) = V(\text{REG})$ | | | 1 | μA |
| $I_{\text{B}}(\text{SNS})$ Input bias current on SNS pin | $V(\text{SNS}) = 5$ V | | | 5 | μA |
| $I_{\text{B}}(\text{TS})$ Input bias current on TS pin | $V(\text{TS}) = 5$ V | | | 5 | μA |
| $I_{\text{B}}(\text{COMP})$ Input bias current on COMP pin | $V(\text{COMP}) = 5$ V | | | 5 | μA |
| BATTERY VOLTAGE REGULATION | | | | | |
| $V_{\text{O}}(\text{REG})$ Output voltage | bq2057, See Notes 1, 2, 3 | 4.059 | 4.10 | 4.141 | V |
| | bq2057C, See Notes 1, 2, 3 | 4.158 | 4.20 | 4.242 | |
| | bq2057T, See Notes 1, 2, 3 | 8.119 | 8.20 | 8.282 | |
| | bq2057W, See Notes 1, 2, 3 | 8.317 | 8.40 | 8.484 | |

NOTES: 1. For high-side current sensing configuration
 2. For low-side current sensing configuration, the tolerance is $\pm 1\%$ for $T_A = 25^\circ\text{C}$ and $\pm 1.2\%$ for $-20^\circ\text{C} \geq T_A \geq 70^\circ\text{C}$
 3. $V(\text{BAT})+0.3$ V $\leq V_{CC} \leq V_{CC(\text{max})}$

bq2057, bq2057C
bq2057T, bq2057W

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---|---|---|-----------------------------|-----------------------------|-----------------------------|------------------|-----|
| CURRENT REGULATION | | | | | | | |
| V(SNS) | Current regulation threshold | bq2057 and bq2057C, High-side current sensing configuration | 95.4 | 105 | 115.5 | mV | |
| | | bq2057T and bq2057W, High-side current sensing configuration | 113.6 | 125 | 137.5 | | |
| | | bq2057 and bq2057C, Low-side current sensing configuration | 100 | 110 | 121 | | |
| | | bq2057T and bq2057W, Low-side current sensing configuration | 118.1 | 130 | 143 | | |
| CHARGE TERMINATION DETECTION | | | | | | | |
| I(TERM) | Charge termination current detect threshold | Voltage at pin SNS, relative to V _{CC} for high-side sensing, and to V _{SS} for low-side sensing, 0°C ≤ T _A ≤ 50°C | | -24 | -14 | -4 | mV |
| TEMPERATURE COMPARATOR | | | | | | | |
| V(TS1) | Lower temperature threshold | TS pin voltage | 29.1 | 30 | 30.9 | %V _{CC} | |
| V(TS2) | Upper temperature threshold | | 58.3 | 60 | 61.8 | | |
| PRECHARGE COMPARATOR | | | | | | | |
| V(min) | Precharge threshold | bq2057 | 2.94 | 3 | 3.06 | V | |
| | | bq2057C | 3.04 | 3.1 | 3.16 | | |
| | | bq2057T | 5.98 | 6.1 | 6.22 | | |
| | | bq2057W | 6.18 | 6.3 | 6.43 | | |
| PRECHARGE CURRENT REGULATION | | | | | | | |
| I(PRECHG) | Precharge current regulation | Voltage at pin SNS, relative to V _{CC} for high-side sensing, and to V _{SS} for low-side sensing, 0°C ≤ T _A ≤ 50°C | | | 13 | mV | |
| | | Voltage at pin SNS, relative to V _{CC} for high-side sensing, 0°C ≤ T _A ≤ 50°C, V _{CC} = 5 V | | 3 | 13 | 22 | mV |
| VRCH COMPARATOR (Battery Recharge Threshold) | | | | | | | |
| V(RCH) | Recharge threshold | bq2057 and bq2057C | V _{O(REG)} -98 mV | V _{O(REG)} -100 mV | V _{O(REG)} -102 mV | V | |
| | | bq2057T and bq2057W | V _{O(REG)} -196 mV | V _{O(REG)} -200 mV | V _{O(REG)} -204 mV | | |
| CHARGE-RATE COMPENSATION (AutoComp) | | | | | | | |
| G(COMP) | AutoComp gain | V(BAT)+0.3 V ≤ V _{CC} ≤ V _{CC(max)} , bq2057, bq2057C, bq2057T, bq2057W | | 1.87 | 2.2 | 2.53 | V/V |
| | | V(BAT)+0.3 V ≤ V _{CC} ≤ V _{CC(max)} , bq2057T and bq2057W in low-side sensing configuration | | 2.09 | 2.4 | 2.76 | |
| STAT PIN | | | | | | | |
| V _{OL(STAT)} | Output (low) voltage | I _{OL} = 10 mA | | | 0.7 | V | |
| V _{OH(STAT)} | Output (high) voltage | I _{OH} = 5 mA | | V _{CC} -0.5 | | | |
| CC PIN | | | | | | | |
| V _{OL(CC)} | Output low voltage | I _{O(CC)} = 5 mA (sink) | | | 1.5 | V | |
| I _{O(CC)} | Sink current | Not to exceed power rating specification (P _D) | | 5 | 40 | mA | |

APPLICATION INFORMATION

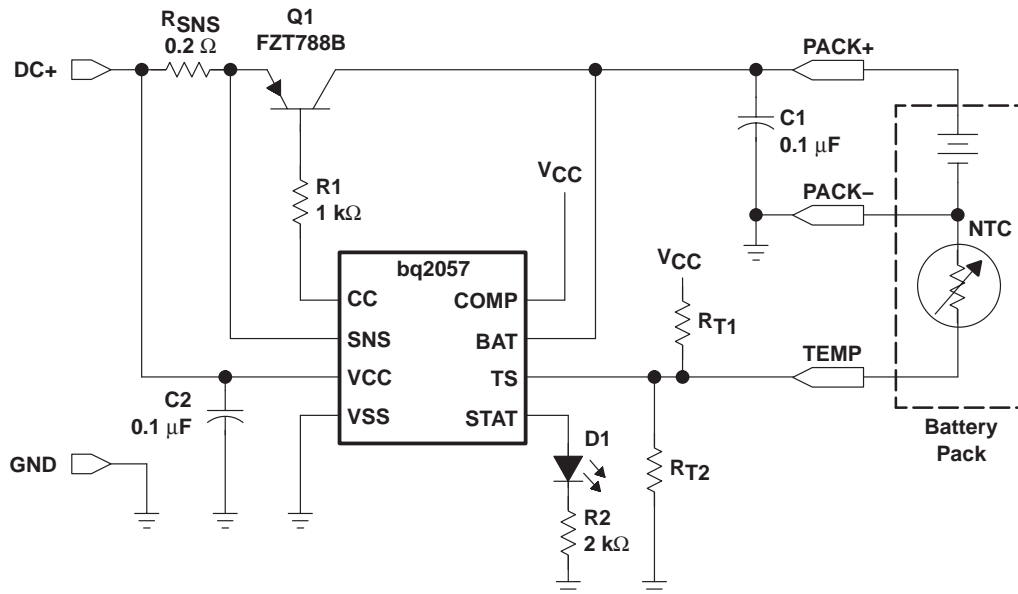


Figure 1. Low Dropout Single- or Two-Cell Li-Ion/Li-Pol Charger

functional description

The bq2057 is an advanced linear charge controller for single or two-cell Li-Ion or Li-Pol applications. Figure 1 shows the schematic of charger using a PNP pass transistor. Figure 2 is an operational state diagram, and Figure 3 is a typical charge profile. Figure 4 shows the schematic of a charger using P-channel MOSFET.

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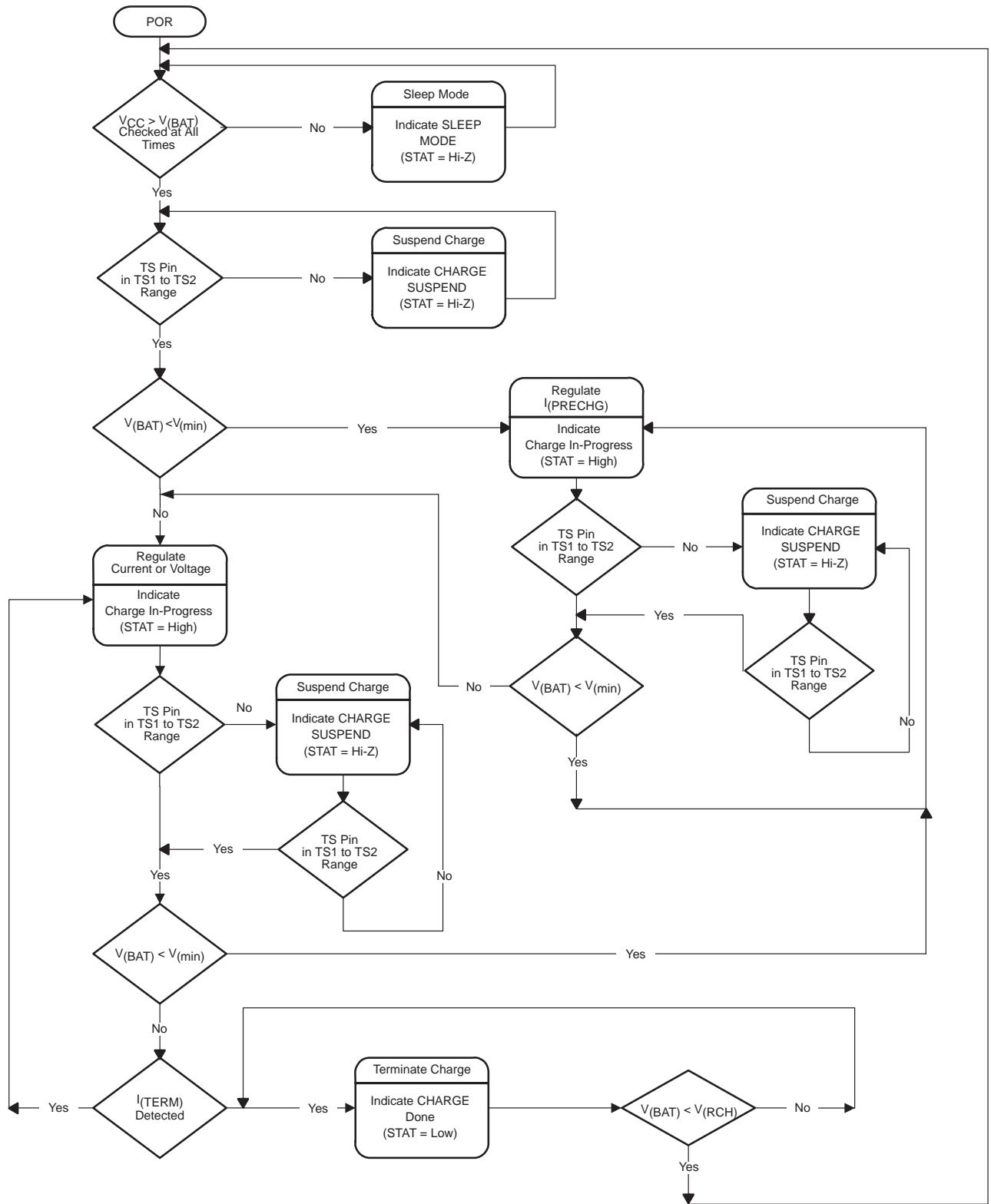


Figure 2. Operation Flowchart

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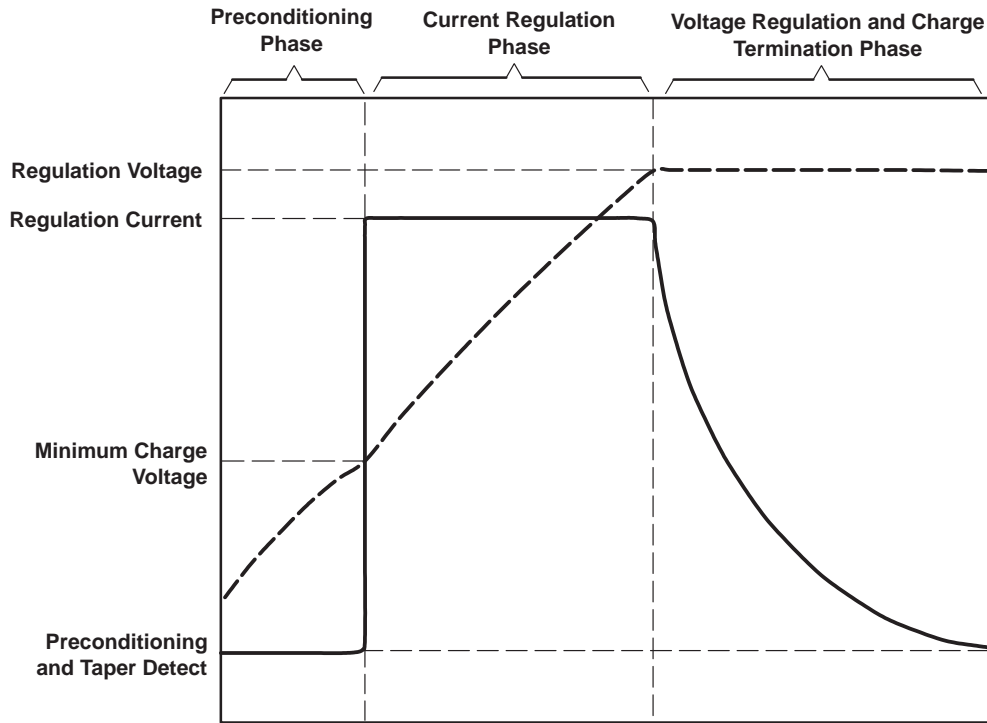


Figure 3. Typical Charge Profile

qualification and precharge

When power is applied, the bq2057 starts a charge-cycle if a battery is already present or when a battery is inserted. Charge qualification is based on battery temperature and voltage. The bq2057 suspends charge if the battery temperature is outside the $V_{(TS1)}$ to $V_{(TS2)}$ range and suspends charge until the battery temperature is within the allowed range. The bq2057 also checks the battery voltage. If the battery voltage is below the precharge threshold $V_{(min)}$, the bq2057 uses precharge to condition the battery. The conditioning charge rate $I_{(PRECHG)}$ is set at approximately 10% of the regulation current. The conditioning current also minimizes heat dissipation in the external pass-element during the initial stage of charge. See Figure 3 for a typical charge-profile.

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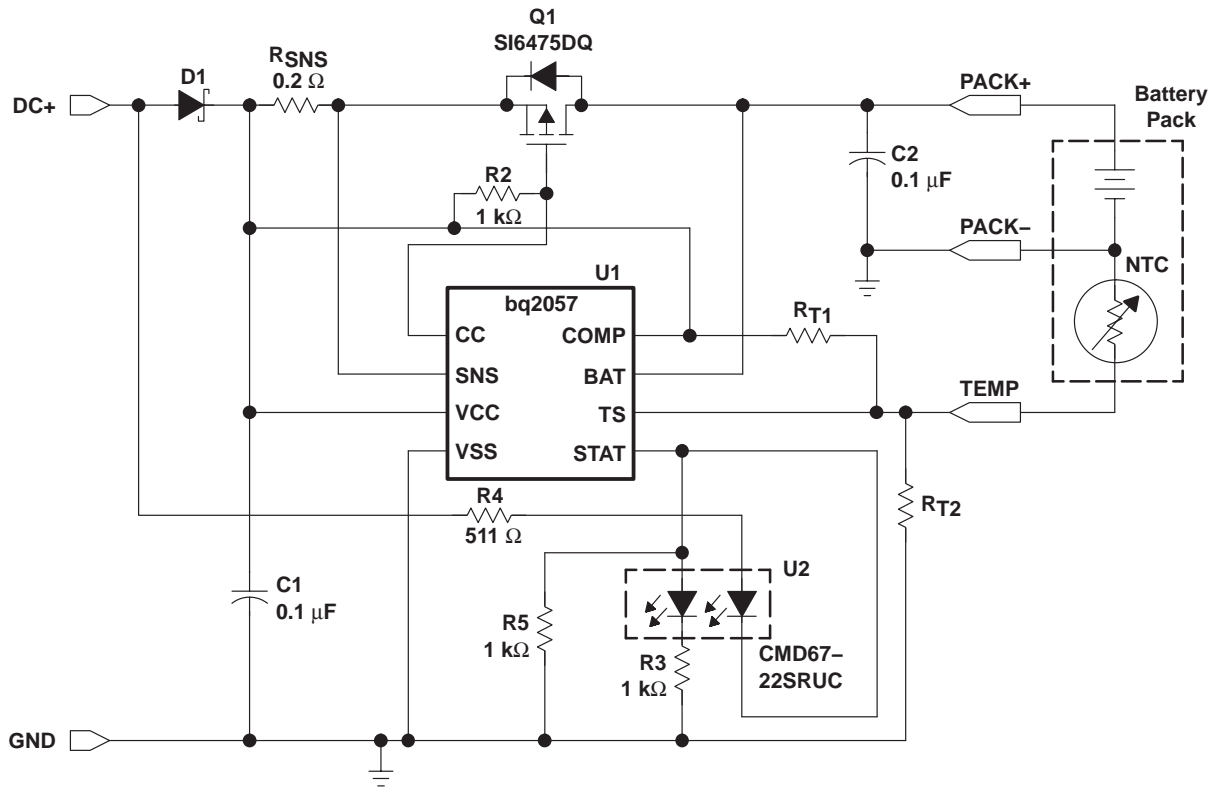


Figure 4. 0.5-A Charger Using P-Channel MOSFET

current regulation phase

The bq2057 regulates current while the battery-pack voltage is less than the regulation voltage, $V_{O(REG)}$. The bq2057 monitors charge current at the SNS input by the voltage drop across a sense-resistor, R_{SNS} , in series with the battery pack. In high-side current sensing configuration (Figure 5), R_{SNS} is between the VCC and SNS pins, and in low-side sensing (Figure 6) the R_{SNS} is between VSS (battery negative) and SNS (charger ground) pins. Charge-current feedback, applied through pin SNS, maintains a voltage of $V_{(SNS)}$ across the current sense resistor. The following formula calculates the value of the sense resistor:

$$R_{SNS} = \frac{V_{(SNS)}}{I_{O(REG)}} \tag{1}$$

Where $I_{O(REG)}$ is the desired charging current.

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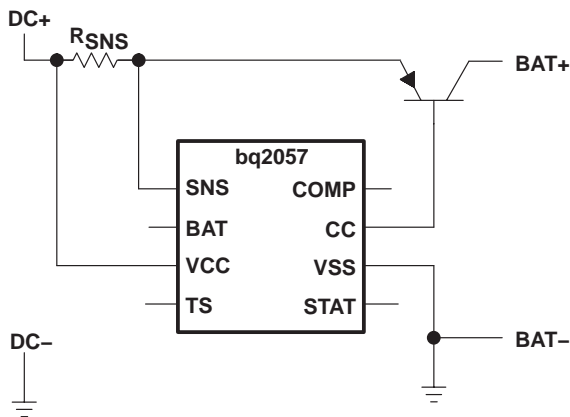


Figure 5. High-Side Current Sensing

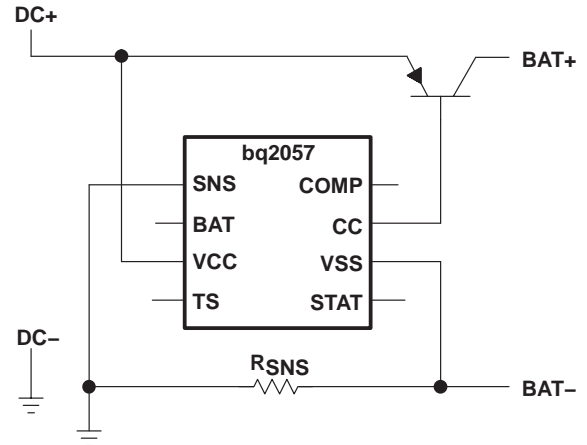


Figure 6. Low-Side Current Sensing

voltage regulation phase

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bq2057 monitors the battery-pack voltage between the BAT and VSS pins. The bq2057 is offered in four fixed-voltage versions: 4.1 V, 4.2 V, 8.2 V and 8.4 V.

Other regulation voltages can be achieved by adding a voltage divider between the positive and negative terminals of the battery pack and using bq2057T or bq2057W. The voltage divider presents scaled battery-pack voltage to BAT input. (See Figure 7 and Figure 8.) The resistor values RB1 and RB2 for the voltage divider are calculated by the following equation:

$$\frac{R_{B1}}{R_{B2}} = \left(N \times \frac{V_{(CELL)}}{V_{O(REG)}} \right) - 1 \tag{2}$$

Where:

N = Number of cells in series

V_(CELL) = Desired regulation voltage per cell

APPLICATION INFORMATION

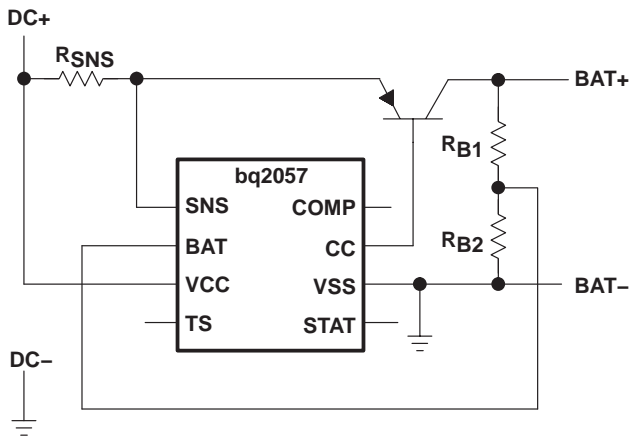


Figure 7. Optional Voltage Divider for Nonstandard Regulation Voltage, (High-Side Current Sensing)

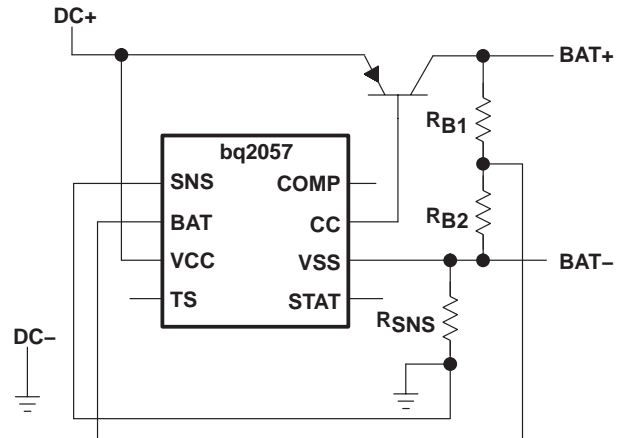


Figure 8. Optional Voltage Divider for Nonstandard Regulation Voltage, (Low-Side Current Sensing)

charge termination and recharge

The bq2057 monitors the charging current during the voltage-regulation phase. The bq2057 declares a done condition and terminates charge when the current tapers off to the charge termination threshold, $I_{(TERM)}$. A new charge cycle begins when the battery voltage falls below the $V_{(RCH)}$ threshold.

battery temperature monitoring

The bq2057 continuously monitors temperature by measuring the voltage between the TS and VSS pins. A negative- or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage. (See Figure 9.) The bq2057 compares this voltage against its internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed. (See Figure 10.) The temperature sensing circuit is immune to any fluctuation in V_{CC} , since both the external voltage divider and the internal thresholds ($V_{(TS1)}$ and $V_{(TS2)}$) are referenced to V_{CC} .

The resistor values of $R_{(T1)}$ and $R_{(T2)}$ are calculated by the following equations:

For NTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TC} - R_{TH})} \tag{3}$$

$$R_{T2} = \frac{5 \times R_{TH} \times R_{TC}}{[(2 \times R_{TC}) - (7 \times R_{TH})]} \tag{4}$$

APPLICATION INFORMATION

battery temperature monitoring (continued)

For PTC Thermistors

$$R_{T1} = \frac{5 \times R_{TH} \times R_{TC}}{3 \times (R_{TH} - R_{TC})} \tag{5}$$

$$R_{T2} = \frac{5 \times R_{TH} \times R_{TC}}{[(2 \times R_{TH}) - (7 \times R_{TC})]} \tag{6}$$

Where $R_{(TC)}$ is the cold temperature resistance and $R_{(TH)}$ is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted if only one temperature (hot or cold) setting is required. Applying a voltage between the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to pin TS disables the temperature-sensing feature.

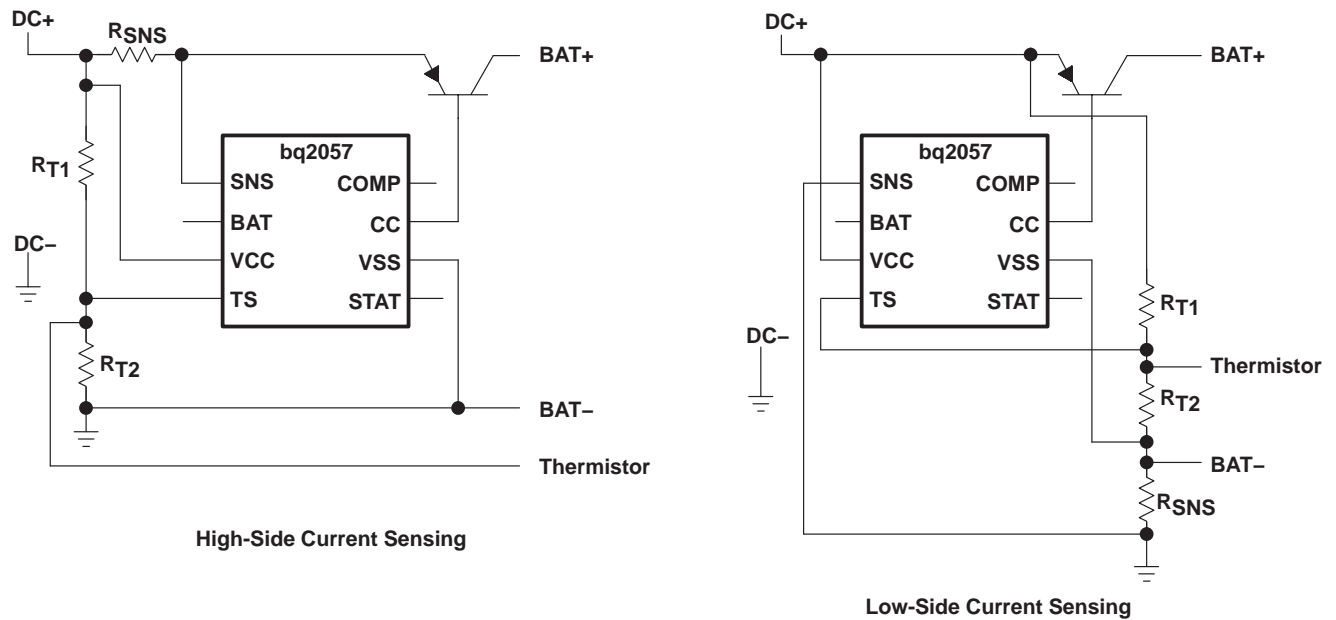


Figure 9. Temperature Sensing Circuits

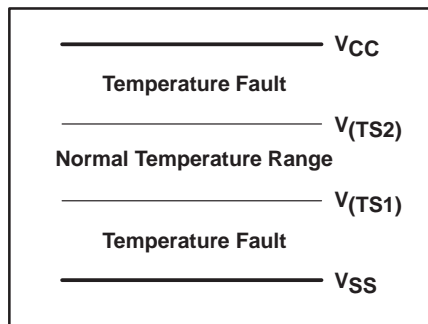


Figure 10. bq2057 TS Input Thresholds

APPLICATION INFORMATION

charge inhibit function

The TS pin can be used as charge-inhibit input. The user can inhibit charge by connecting the TS pin to VCC or VSS (or any level outside the $V_{(TS1)}$ to $V_{(TS2)}$ thresholds). Applying a voltage between the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to pin TS returns the charger to normal operation.

charge status indication

The bq2057 reports the status of the charger on the 3-state STAT pin. The following table summarized the operation of the STAT pin.

| CONDITION | STAT PIN |
|-----------------------------------|----------|
| Battery conditioning and charging | High |
| Charge complete (Done) | Low |
| Temperature fault or sleep mode | Hi-Z |

The STAT pin can be used to drive a single LED (Figure 1), dual-chip LEDs (Figure 4) or for interface to a host or system processor (Figure 11). When interfacing the bq2057 to a processor, the user can use an output port, as shown in Figure 11, to recognize the high-Z state of the STAT pin. In this configuration, the user needs to read the input pin, toggle the output port and read the STAT pin again. In a high-Z condition, the input port always matches the signal level on the output port.

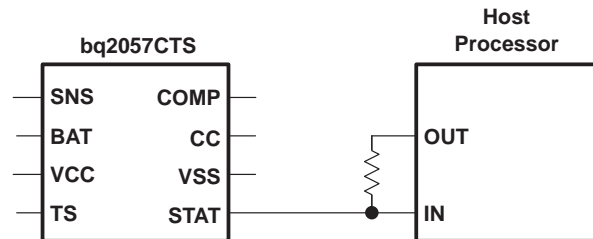


Figure 11. Interfacing the bq2057 to a Host Processor

low-power sleep mode

The bq2057 enters the sleep mode if the VCC falls below the voltage at the BAT input. This feature prevents draining the battery pack during the absence of VCC.

APPLICATION INFORMATION

selecting an external pass-transistor

The bq2057 is designed to work with both PNP transistor and P-channel MOSFET. The device should be chosen to handle the required power dissipation, given the circuit parameters, PCB layout and heat sink configuration. The following examples illustrate the design process for either device:

PNP transistor:

Selection steps for a PNP bipolar transistor: Example: $V_I = 4.5\text{ V}$, $I_{(\text{REG})} = 1\text{ A}$, 4.2-V single-cell Li-Ion (bq2057C). V_I is the input voltage to the charger and $I_{(\text{REG})}$ is the desired charge current (see Figure 1).

- Determine the maximum power dissipation, P_D , in the transistor.
The worst case power dissipation happens when the cell voltage, $V_{(\text{BAT})}$, is at its lowest (typically 3 V at the beginning of current regulation phase) and V_I is at its maximum.
Where V_{CS} is the voltage drop across the current sense resistor.

$$\begin{aligned} P_D &= (V_I - V_{\text{CS}} - V_{(\text{BAT})}) \times I_{\text{REG}} & (7) \\ P_D &= (4.5 - 0.1 - 3) \times 1\text{ A} \\ P_D &= 1.4\text{ W} \end{aligned}$$

- Determine the package size needed in order to keep the junction temperature below the manufacturer's recommended value, $T_{(\text{J})\text{max}}$. Calculate the total theta, θ_{JC} ($^{\circ}\text{C}/\text{W}$), needed.

$$\begin{aligned} \theta_{\text{JC}} &= \frac{(T_{(\text{J})\text{max}} - T_{\text{A(max)}})}{P_D} & (8) \\ \theta_{\text{JC}} &= \frac{(150 - 40)}{1.4} \\ \theta_{\text{JC}} &= 78^{\circ}\text{C}/\text{W} \end{aligned}$$

Now choose a device package with a theta at least 10% below this value to account for additional thetas other than the device. A SOT223 package, for instance, has typically a theta of $60^{\circ}\text{C}/\text{W}$.

- Select a collector-emitter voltage, $V_{(\text{CE})}$, rating greater than the maximum input voltage. A 15-V device will be adequate in this example.
- Select a device that has at least 50% higher drain current I_C rating than the desired charge current $I_{(\text{REG})}$.
- Using the following equation, calculate the minimum beta (β or h_{FE}) needed:

$$\begin{aligned} \beta_{\text{min}} &= \frac{I_{\text{C MAX}}}{I_{\text{B}}} & (9) \\ \beta_{\text{min}} &= \frac{1}{0.035} \\ \beta_{\text{min}} &= 28 \end{aligned}$$

where $I_{\text{max(C)}}$ is the maximum collector current (in this case same as $I_{(\text{REG})}$), and I_{B} is the base current (chosen to be 35 mA in this example).

NOTE:

The beta of a transistor drops off by a factor of 3 over temperature and also drops off with load. Therefore, note the beta of device at $I_{(\text{REG})}$ and the minimum ambient temperature when choosing the device. This beta should be larger than the minimum required beta.

Now choose a PNP transistor that is rated for $V_{(\text{CE})} \geq 15\text{ V}$, $\theta_{\text{JC}} \leq 78^{\circ}\text{C}/\text{W}$, $I_C \geq 1.5\text{ A}$, $\beta_{\text{min}} \geq 28$ and that is in a SOT223 package.

APPLICATION INFORMATION

selecting an external pass-transistor (continued)

P-channel MOSFET:

Selection steps for a P-channel MOSFET: Example: $V_I = 5.5$ V, $I_{(REG)} = 500$ mA, 4.2-V single-cell Li-Ion (bq2057C). V_I is the input voltage to the charger and $I_{(REG)}$ is the desired charge current. (See Figure 4.)

1. Determine the maximum power dissipation, P_D , in the transistor.

The worst case power dissipation happens when the cell voltage, $V_{(BAT)}$, is at its lowest (typically 3 V at the beginning of current regulation phase) and V_I is at its maximum.

Where V_D is the forward voltage drop across the reverse-blocking diode (if one is used), and V_{CS} is the voltage drop across the current sense resistor.

$$\begin{aligned} P_D &= (V_I - V_D - V_{(CS)} - V_{(BAT)}) \times I_{(REG)} & (10) \\ P_D &= (5.5 - 0.4 - 0.1 - 3) \times 0.5 \text{ A} \\ P_D &= 1 \text{ W} \end{aligned}$$

2. Determine the package size needed in order to keep the junction temperature below the manufacturer's recommended value, T_{JMAX} . Calculate the total theta, $\theta(^{\circ}\text{C}/\text{W})$, needed.

$$\begin{aligned} \theta_{JC} &= \frac{(T_{\max(J)} - T_{A(\max)})}{P_D} & (11) \\ \theta_{JC} &= \frac{(150 - 40)}{1} \\ \theta_{JC} &= 110^{\circ}\text{C}/\text{W} \end{aligned}$$

Now choose a device package with a theta at least 10% below this value to account for additional thetas other than the device. A TSSOP-8 package, for instance, has typically a theta of $70^{\circ}\text{C}/\text{W}$.

3. Select a drain-source voltage, $V_{(DS)}$, rating greater than the maximum input voltage. A 12 V device will be adequate in this example.
4. Select a device that has at least 50% higher drain current (I_D) rating than the desired charge current $I_{(REG)}$.
5. Verify that the available drive is large enough to supply the desired charge current.

$$\begin{aligned} V_{(GS)} &= (V_D + V_{(CS)} + V_{OL(CC)}) - V_I & (12) \\ V_{(GS)} &= (0.4 + 0.1 + 1.5) - 5.5 \\ V_{(GS)} &= -3.5 \end{aligned}$$

Where $V_{(GS)}$ is the gate-to-source voltage, V_D is the forward voltage drop across the reverse-blocking diode (if one is used), and V_{CS} is the voltage drop across the current sense resistor, and $V_{OL(CC)}$ is the CC pin output low voltage specification for the bq2057.

Select a MOSFET with gate threshold voltage, $V_{(GSth)}$, rating less than the calculated $V_{(GS)}$.

Now choose a P-channel MOSFET transistor that is rated for $V_{DS} \leq -15$ V, $\theta_{JC} \leq 110^{\circ}\text{C}/\text{W}$, $I_D \geq 1$ A, $V_{(GSth)} \geq -3.5$ V and in a TSSOP package.

APPLICATION INFORMATION

automatic charge-rate compensation (continued)

AutoComp setup requires the following information:

- Total impedance of battery pack ($Z_{(PACK)}$)
- Maximum charging current ($I_{(REG)}$)

The voltage drop across the internal impedance of battery pack, $V_{(Z)}$, can then be calculated using the following equation:

$$V_{(Z)} = Z_{(PACK)} \times I_{(REG)} \tag{13}$$

The required compensation is then calculated using the following equations:

$$V_{(COMP)} = \frac{V_{(Z)}}{G_{(COMP)}} \tag{14}$$

$$V_{(PACK)} = V_{O(REG)} + (G_{(COMP)} \times V_{(COMP)})$$

Where $V_{(COMP)}$ is the voltage on COMP pin. This voltage is referenced to VCC in high-side current sensing configuration and to VSS for low-side sensing. $V_{(PACK)}$ is the voltage across the battery pack.

The values of $R_{(COMP1)}$ and $R_{(COMP2)}$ can be calculated using the following equation:

$$\frac{V_{(COMP)}}{V_{(SNS)}} = \frac{R_{COMP2}}{R_{COMP1} + R_{COMP2}} \tag{15}$$

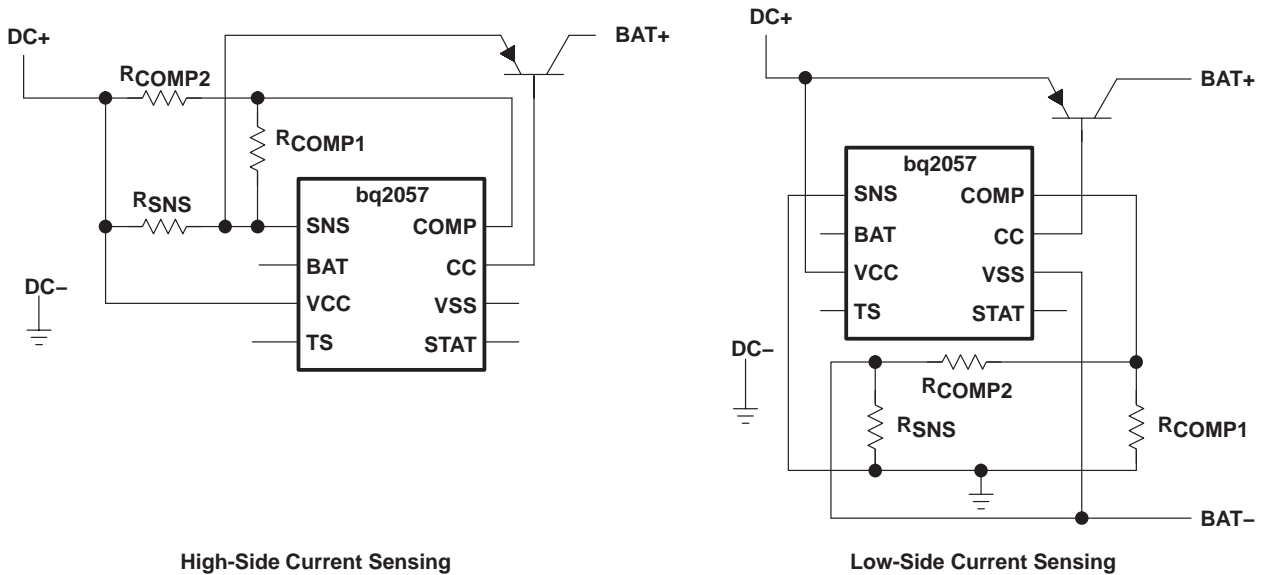


Figure 13. AutoComp Circuits

APPLICATION INFORMATION

automatic charge-rate compensation (continued)

The following example illustrates these calculations:

Assume $Z_{(PACK)} = 100 \text{ m}\Omega$, $I_{(REG)} = 500 \text{ mA}$, high-side current sensing bq2057C

$$V_{(Z)} = Z_{(PACK)} \times I_{(REG)} \quad (16)$$

$$V_{(Z)} = 0.1 \times 0.5$$

$$V_{(Z)} = 50 \text{ mV}$$

$$V_{(COMP)} = \frac{V_{(Z)}}{G_{(COMP)}} \quad (17)$$

$$V_{(COMP)} = \frac{0.05}{2.2}$$

$$V_{(COMP)} = 22.7 \text{ mV}$$

Let $R_{COMP2} = 10 \text{ k}\Omega$

$$R_{COMP1} = \frac{R_{COMP2} \times (V_{(SNS)} - V_{(COMP)})}{V_{(COMP)}} \quad (18)$$

$$R_{COMP1} = 10\text{k} \times \frac{(105 \text{ mV} - 22.7 \text{ mV})}{22.7 \text{ mV}}$$

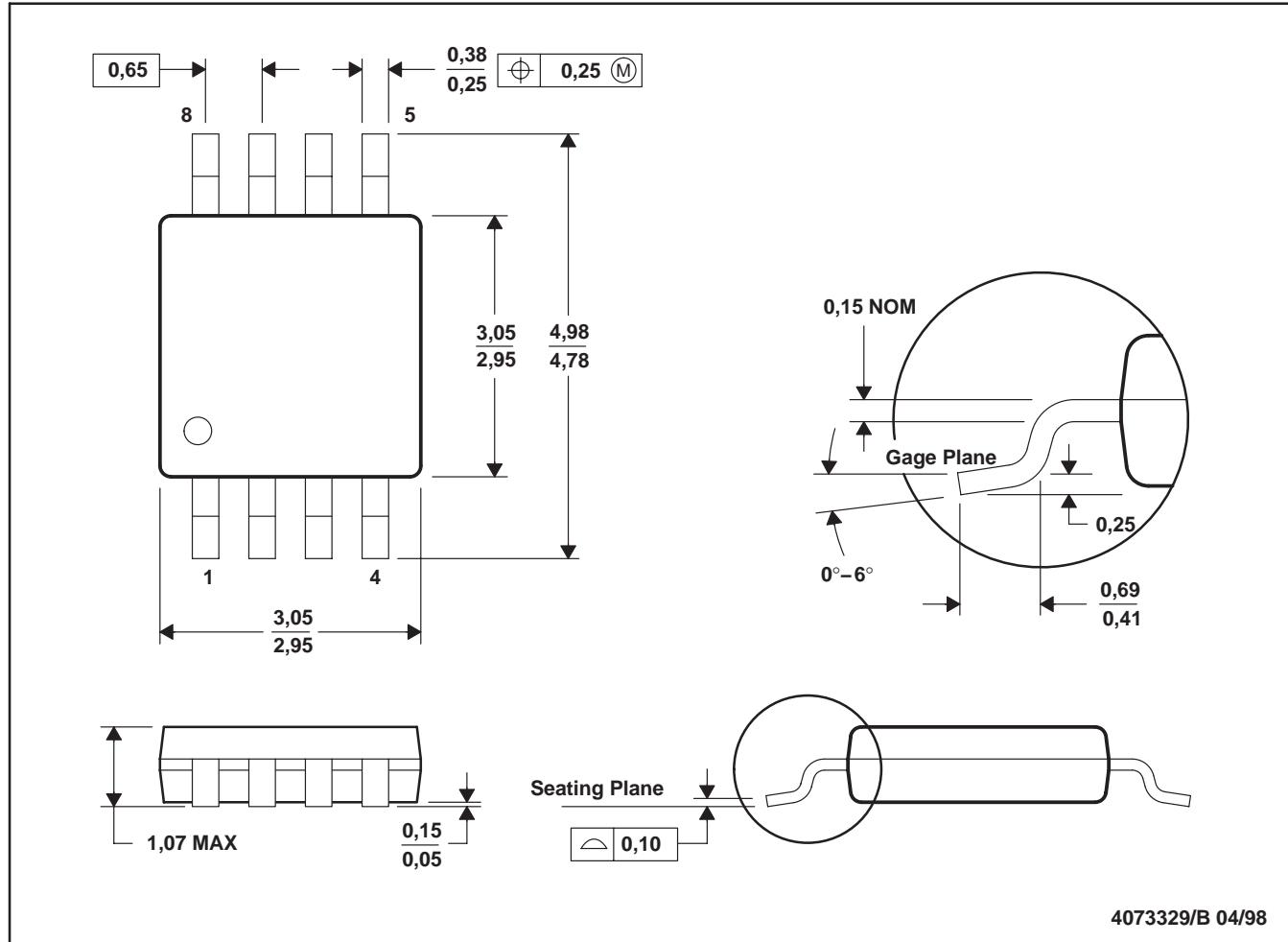
$$R_{COMP1} = 36.25 \text{ k}\Omega$$

Use the closest standard value (36.0 k Ω) for R_{COMP1}

MECHANICAL DATA

DGK (R-PDSO-G8)

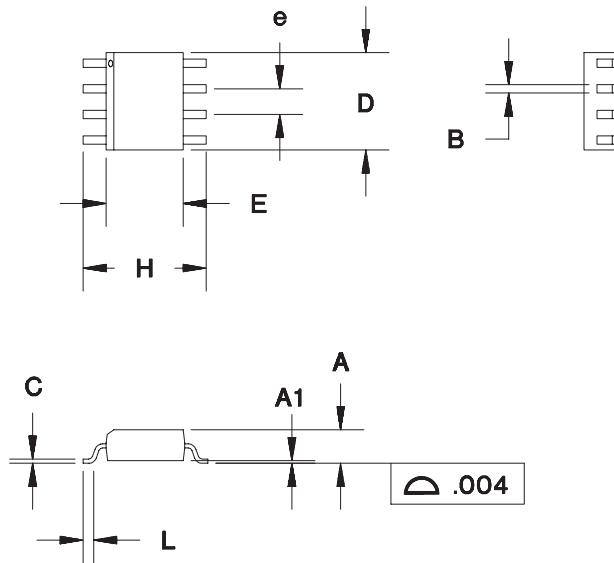
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-187

MECHANICAL DATA

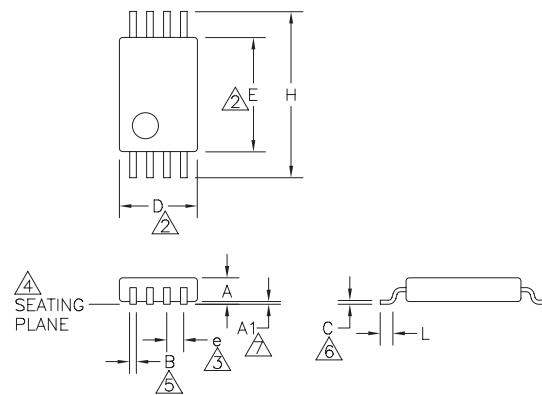
8-Pin SOIC Narrow (SN)



8-Pin SN (0.150" SOIC)

| Dimension | Inches | | Millimeters | |
|-----------|--------|-------|-------------|------|
| | Min. | Max. | Min. | Max. |
| A | 0.060 | 0.070 | 1.52 | 1.78 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.007 | 0.010 | 0.18 | 0.25 |
| D | 0.185 | 0.200 | 4.70 | 5.08 |
| E | 0.150 | 0.160 | 3.81 | 4.06 |
| e | 0.045 | 0.055 | 1.14 | 1.40 |
| H | 0.225 | 0.245 | 5.72 | 6.22 |
| L | 0.015 | 0.035 | 0.38 | 0.89 |

TS: 8-Pin TSSOP



| Dimension | Inches | | Millimeters | |
|-----------|-----------|-------|-------------|------|
| | Min. | Max. | Min. | Max. |
| A | - | 0.043 | - | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| B | 0.007 | 0.012 | 0.18 | 0.30 |
| C | 0.004 | 0.007 | 0.09 | 0.18 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| E | 0.169 | 0.176 | 4.30 | 4.48 |
| e | 0.0256BSC | | 0.65BSC | |
| H | 0.246 | 0.256 | 6.25 | 6.50 |

Notes:

1. Controlling dimension: millimeters. Inches shown for reference only.
2. 'D' and 'E' do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0,15 mm per side.
3. Each lead centerline shall be located within $\pm 0,10$ mm of its exact true position.
4. Leads shall be coplanar within 0,08 mm at the seating plane.
5. Dimension 'B' does not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed 'B' maximum by more than 0,08 mm.
6. Dimension applies to the flat section of the lead between 0,10 mm and 0,25 mm from the lead tip.
7. A1' is defined as the distance from the seating plane to the lowest point of the package body (base plane).

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| BQ2057CDGK | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CDGKG4 | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CDGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CSN | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057CSNG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057CSNTR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057CSNTRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057CTS | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CTSG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CTSTR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057CTSTRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057DGK | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057DGKG4 | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057DGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057DGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057PDGK | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057PDGKG4 | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057PDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057PDGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057SN | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057SNG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057SNTRG4 | ACTIVE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| BQ2057TS | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057TSG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| BQ2057TSN | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057TSNTRG4 | ACTIVE | SOIC | D | 8 | | TBD | Call TI | Call TI |
| BQ2057TSTRG4 | ACTIVE | TSSOP | PW | 8 | | TBD | Call TI | Call TI |
| BQ2057TTS | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057TTSG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057TTSTR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057TTSTRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057WSN | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057WSNG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057WSNTR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057WSNTRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| BQ2057WTS | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057WTSG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057WTSTR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ2057WTSTRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

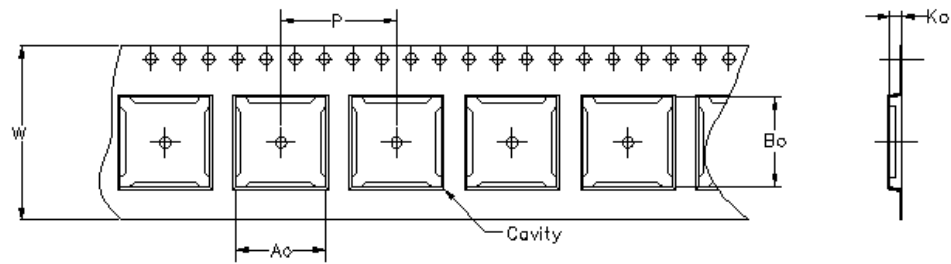
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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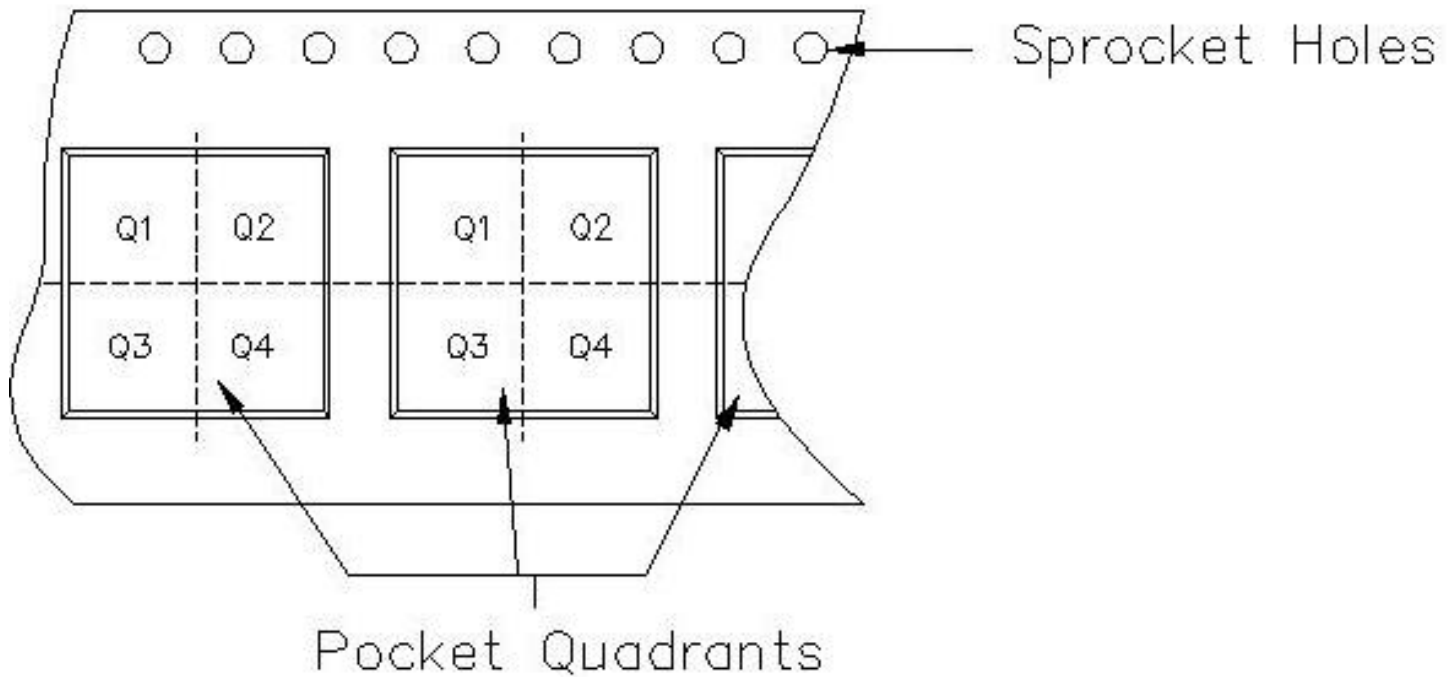
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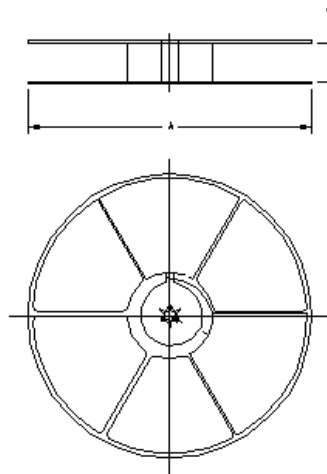
Carrier tape design is defined largely by the component length, width, and thickness.

| |
|--|
| A_o = Dimension designed to accommodate the component width. |
| B_o = Dimension designed to accommodate the component length. |
| K_o = Dimension designed to accommodate the component thickness. |
| W = Overall width of the carrier tape. |
| P = Pitch between successive cavity centers. |



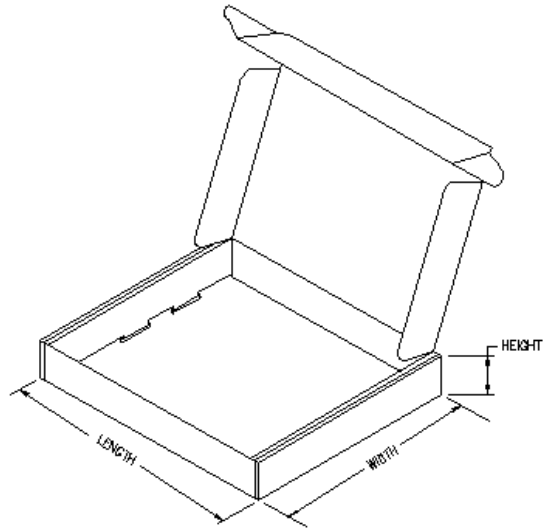
TAPE AND REEL INFORMATION

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|---------|------|------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| BQ2057CDGKR | DGK | 8 | MLA | 330 | 12 | 5.3 | 3.4 | 1.4 | 8 | 12 | Q1 |
| BQ2057CSNTR | D | 8 | MLA | 330 | 12 | 6.9 | 5.4 | 2.0 | 8 | 12 | Q1 |
| BQ2057CTSTR | PW | 8 | MLA | 330 | 12 | 7.0 | 3.6 | 1.6 | 8 | 12 | Q1 |
| BQ2057DGKR | DGK | 8 | MLA | 330 | 12 | 5.3 | 3.4 | 1.4 | 8 | 12 | Q1 |
| BQ2057PDGKR | DGK | 8 | MLA | 330 | 12 | 5.3 | 3.4 | 1.4 | 8 | 12 | Q1 |
| BQ2057TTSTR | PW | 8 | MLA | 330 | 12 | 7.0 | 3.6 | 1.6 | 8 | 12 | Q1 |
| BQ2057WSNTR | D | 8 | MLA | 330 | 12 | 6.9 | 5.4 | 2.0 | 8 | 12 | Q1 |
| BQ2057WSNTRG4 | D | 8 | MLA | 330 | 12 | 6.9 | 5.4 | 2.0 | 8 | 12 | Q1 |
| BQ2057WTSTR | PW | 8 | MLA | 330 | 12 | 7.0 | 3.6 | 1.6 | 8 | 12 | Q1 |



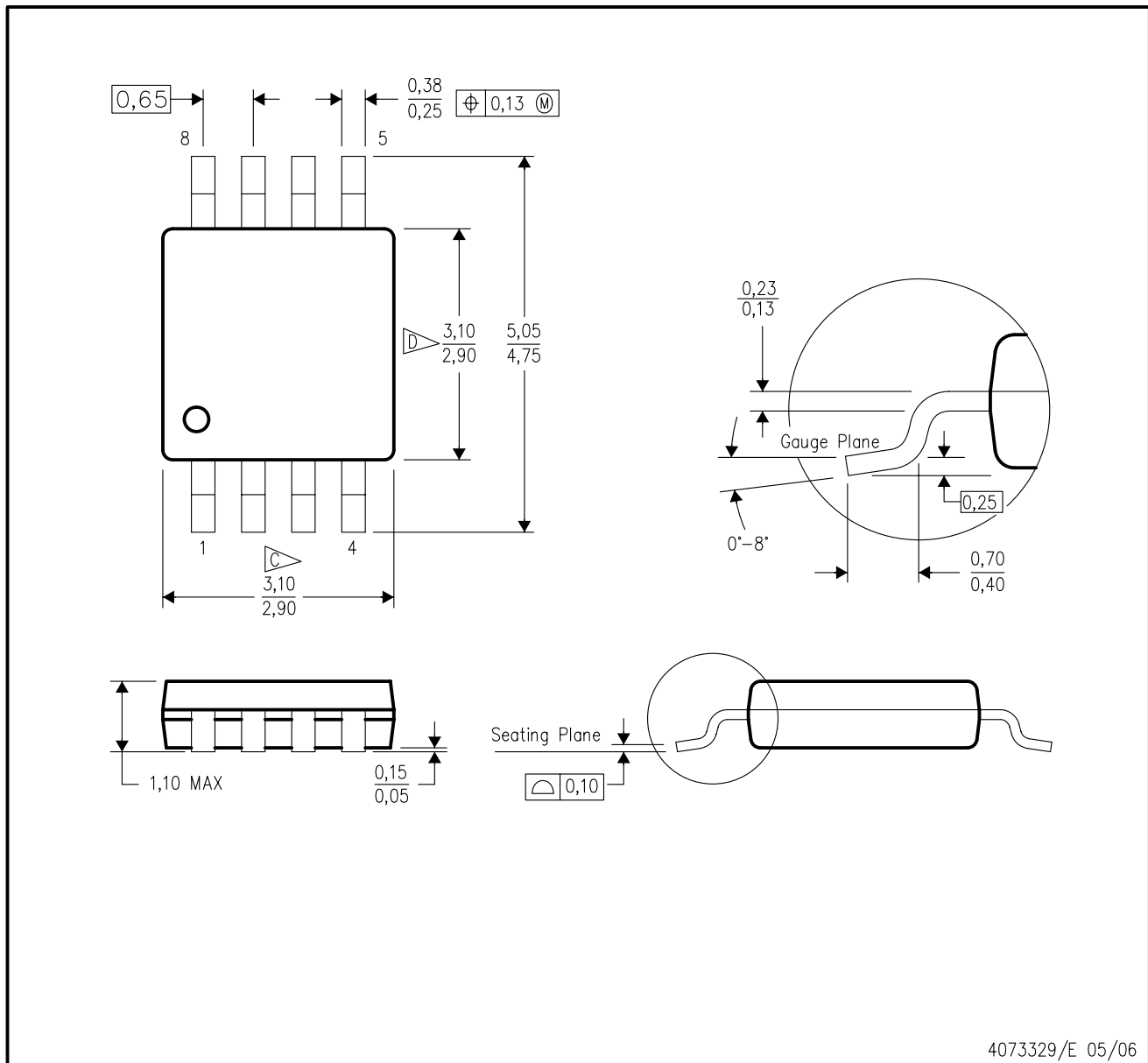
TAPE AND REEL BOX INFORMATION

| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---------------|---------|------|------|-------------|------------|-------------|
| BQ2057CDGKR | DGK | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057CSNTR | D | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057CTSTR | PW | 8 | MLA | 552.0 | 346.0 | 36.0 |
| BQ2057DGKR | DGK | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057PDGKR | DGK | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057TTSTR | PW | 8 | MLA | 552.0 | 346.0 | 36.0 |
| BQ2057WSNTR | D | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057WSNTRG4 | D | 8 | MLA | 346.0 | 346.0 | 29.0 |
| BQ2057WTSTR | PW | 8 | MLA | 552.0 | 346.0 | 36.0 |



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

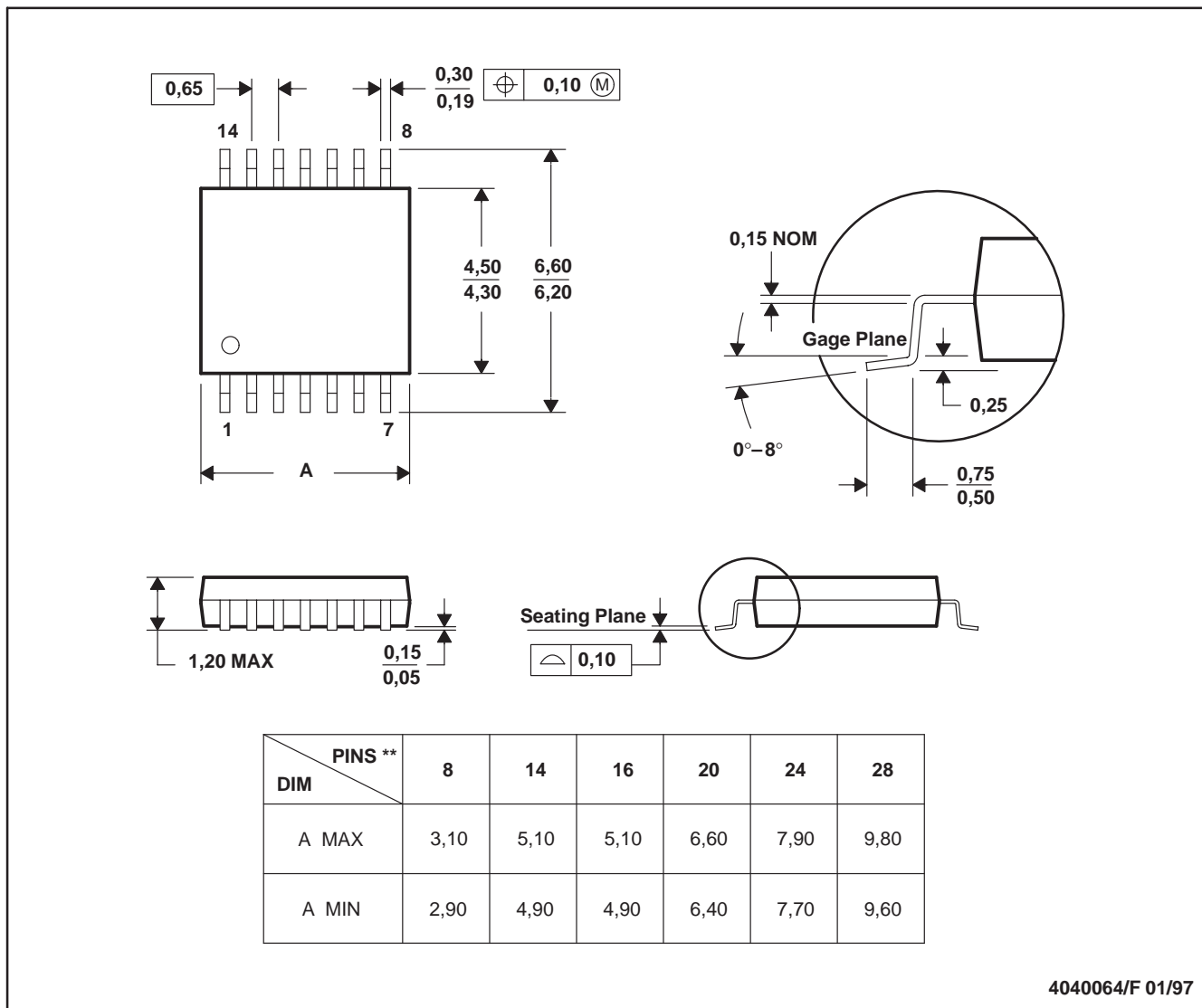


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - Falls within JEDEC MO-187 variation AA, except interlead flash.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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