Micropower, Single and Dual Supply Rail-to-Rail Instrumentation Amplifier

AD627

FEATURES

Micropower, 85 μA Max Supply Current
Wide Power Supply Range (+2.2 V to ±18 V)
Easy to Use
  Gain Set with One External Resistor
  Gain Range 5 (No Resistor) to 1,000
Higher Performance than Discrete Designs
Rail-to-Rail Output Swing
High Accuracy DC Performance
  0.10% Gain Accuracy (G = +5) (AD627A)
  10 ppm Gain Drift (G = +5)
  125 μV Max Input Offset Voltage (AD627B)
  200 μV Max Input Offset Voltage (AD627A)
  1 μV/°C Max Input Offset Voltage Drift (AD627B)
  3 μV/°C Max Input Offset Voltage Drift (AD627A)
  10 nA Max Input Bias Current
Noise: 38 nV/√Hz RTI Noise @ 1 kHz (G = +100)
Excellent AC Specifications
  77 dB Min CMRR (G = +5) (AD627A)
  83 dB Min CMRR (G = +5) (AD627B)
  80 kHz Bandwidth (G = +5)
  135 μs Settling Time to 0.01% (G = +5, 5 V Step)

APPLICATIONS

4 mA-to-20 mA Loop Powered Applications
Low Power Medical Instrumentation—ECG, EEG
Transducer Interfacing
Thermocouple Amplifiers
Industrial Process Controls
Low Power Data Acquisition
Portable Battery Powered Instruments

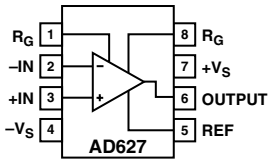
PRODUCT DESCRIPTION

The AD627 is an integrated, micropower, instrumentation amplifier that delivers rail-to-rail output swing on single and dual (+2.2 V to ±18 V) supplies. The AD627 provides the user with excellent ac and dc specifications while operating at only 85 μA max.

The AD627 offers superior user flexibility by allowing the user to set the gain of the device with a single external resistor, and by conforming to the 8-lead industry standard pinout configuration. With no external resistor, the AD627 is configured for a gain of 5. With an external resistor, it can be programmed for gains of up to 1000.

FUNCTIONAL BLOCK DIAGRAM

8-Lead Plastic DIP (N) and SOIC (R)



Wide supply voltage range (+2.2 V to ±18 V), and micropower current consumption make the AD627 a perfect fit for a wide range of applications. Single supply operation, low power consumption and rail-to-rail output swing make the AD627 ideal for battery powered applications. Its rail-to-rail output stage maximizes dynamic range when operating from low supply voltages. Dual supply operation (±15 V) and low power consumption make the AD627 ideal for industrial applications, including 4 mA-to-20 mA loop-powered systems.

The AD627 does not compromise performance, unlike other micropower instrumentation amplifiers. Low voltage offset, offset drift, gain error, and gain drift keep dc errors to a minimum in the users system. The AD627 also holds errors over frequency to a minimum by providing excellent CMRR over frequency. Line noise, as well as line harmonics, will be rejected, since the CMRR remains high up to 200 Hz.

The AD627 provides superior performance, uses less circuit board area and does it for a lower cost than micropower discrete designs.

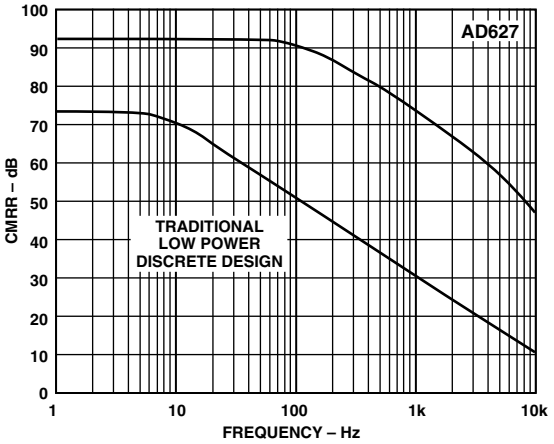


Figure 1. CMRR vs. Frequency, ±5 V_S, Gain = +5

REV. B

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AD627–SPECIFICATIONS

SINGLE SUPPLY (Typical @ 25°C Single Supply, V_S = 3 V and 5 V and R_L = 20 kΩ, unless otherwise noted.)

Model Specification	Conditions	AD627A Min	 Typ	 Max	AD627B Min	 Typ	 Max	Unit
GAIN	G = +5 + (200 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = (–V_S) + 0.1 to (+V_S) – 0.15							
G = +5			0.03	0.10		0.01	0.06	%
G = +10			0.15	0.35		0.10	0.25	%
G = +100			0.15	0.35		0.10	0.25	%
G = +1000			0.50	0.70		0.25	0.35	%
Nonlinearity								
G = +5			10	100		10	100	ppm
G = +100			20	100		20	100	ppm
Gain vs. Temperature[1]								
G = +5			10	20		10	20	ppm/°C
G > 5			–75			–75		ppm/°C
VOLTAGE OFFSET								
Input Offset, V_{OSI}[2]			50	250		25	150	µV
Over Temperature	V_{CM} = V_{REF} = +V_S/2			445			215	µV
Average TC			0.1	3		0.1	1	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Over Temperature				1650			1150	µV
Average TC			2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSRR)								
G = +5		86	100		86	100		dB
G = +10		100	120		100	120		dB
G = +100		110	125		110	125		dB
G = +1000		110	125		110	125		dB
INPUT CURRENT								
Input Bias Current			3	10		3	10	nA
Over Temperature				15			15	nA
Average TC			20			20		pA/°C
Input Offset Current			0.3	1		0.3	1	nA
Over Temperature				2			2	nA
Average TC			1			1		pA/°C
INPUT								
Input Impedance								
Differential			20‖2			20‖2		GΩ‖pF
Common-Mode			20‖2			20‖2		GΩ‖pF
Input Voltage Range[3]	V_S = 2.2 V to 36 V	(–V_S) – 0.1		(+V_S) – 1	(–V_S) – 0.1		(+V_S) – 1	V
Common-Mode Rejection[3]								
Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{REF} = V_S/2							
G = +5	V_S = 3 V, V_{CM} = 0 V to 1.9 V	77	90		83	96		dB
G = +5	V_S = 5 V, V_{CM} = 0 V to 3.7 V	77	90		83	96		dB
OUTPUT								
Output Swing	R_L = 20 kΩ	(–V_S) + 25		(+V_S) – 70	(–V_S) + 25		(+V_S) – 70	mV
	R_L = 100 kΩ	(–V_S) + 7		(+V_S) – 25	(–V_S) + 7		(+V_S) – 25	mV
Short-Circuit Current	Short-Circuit to Ground		±25			±25		mA
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth								
G = +5			80			80		kHz
G = +100			3			3		kHz
G = +1000			0.4			0.4		kHz
Slew Rate			+0.05/–0.07			+0.05/–0.07		V/µs
Settling Time to 0.01%	V_S = 3 V, 1.5 V Output Step							
G = +5			65			65		µs
G = +100			290			290		µs
Settling Time to 0.01%	V_S = 5 V, 2.5 V Output Step							
G = +5			85			85		µs
G = +100			330			330		µs
Overload Recovery	50% Input Overload		3			3		µs

NOTES
[1]Does not include effects of external resistor R_G.
[2]See Table III for total RTI errors.
[3]See Applications section for input range, gain range and common-mode range.

Specifications subject to change without notice.

DUAL SUPPLY (Typical @ 25°C Dual Supply, V_S = ±5 V and ±15 V and R_L = 20 kΩ, unless otherwise noted.)

Model / Specification	Conditions	AD627A Min	AD627A Typ	AD627A Max	AD627B Min	AD627B Typ	AD627B Max	Unit
GAIN	G = +5 + (200 kΩ/R_G)							
Gain Range		5		1000	5		1000	V/V
Gain Error[1]	V_{OUT} = (–V_S) + 0.1 to (+V_S) – 0.15							
G = +5			0.03	0.10		0.01	0.06	%
G = +10			0.15	0.35		0.10	0.25	%
G = +100			0.15	0.35		0.10	0.25	%
G = +1000			0.50	0.70		0.25	0.35	%
Nonlinearity								
G = +5	V_S = ±5 V/±15 V		10/25	100		10/25	100	ppm
G = +100	V_S = ±5 V/±15 V		10/15	100		10/15	100	ppm
Gain vs. Temperature[1]								
G = +5			10	20		10	20	ppm/°C
G > 5			–75			–75		ppm/°C
VOLTAGE OFFSET	Total RTI Error = V_{OSI} + $V_{OSO/G}$							
Input Offset, V_{OSI}[2]			25	200		25	125	µV
Over Temperature	V_{CM} = V_{REF} = 0 V			395			190	µV
Average TC			0.1	3		0.1	1	µV/°C
Output Offset, V_{OSO}				1000			500	µV
Over Temperature				1700			1100	µV
Average TC			2.5	10		2.5	10	µV/°C
Offset Referred to the Input vs. Supply (PSRR)								
G = +5		86	100		86	100		dB
G = +10		100	120		100	120		dB
G = +100		110	125		110	125		dB
G = +1000		110	125		110	125		dB
INPUT CURRENT								
Input Bias Current			2	10		2	10	nA
Over Temperature				15			15	nA
Average TC			20			20		pA/°C
Input Offset Current			0.3	1		0.3	1	nA
Over Temperature				5			5	nA
Average TC			5			5		pA/°C
INPUT								
Input Impedance								
Differential			20‖2			20‖2		GΩ‖pF
Common-Mode			20‖2			20‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±1.1 V to ±18 V	(–V_S) – 0.1		(+V_S) – 1	(–V_S) – 0.1		(+V_S) – 1	V
Common-Mode Rejection[3]								
Ratio DC to 60 Hz with 1 kΩ Source Imbalance								
G = +5–1000	V_S = ±5 V, V_{CM} = –4 V to +3.0 V	77	90		83	96		dB
G = +5–1000	V_S = ±15 V, V_{CM} = –12 V to +10.9 V	77	90		83	96		dB
OUTPUT								
Output Swing	R_L = 20 kΩ	(–V_S) + 25		(+V_S) – 70	(–V_S) + 25		(+V_S) – 70	mV
	R_L = 100 kΩ	(–V_S) + 7		(+V_S) – 25	(–V_S) + 7		(+V_S) – 25	mV
Short-Circuit Current	Short Circuit to Ground		±25			±25		mA
DYNAMIC RESPONSE								
Small Signal –3 dB Bandwidth								
G = +5			80			80		kHz
G = +100			3			3		kHz
G = +1000			0.4			0.4		kHz
Slew Rate			+0.05/–0.06			+0.05/–0.06		V/µs
Settling Time to 0.01%	V_S = ±5 V, +5 V Output Step							
G = +5			135			135		µs
G = +100			350			350		µs
Settling Time to 0.01%	V_S = ±15 V, +15 V Output Step							
G = +5			330			330		µs
G = +100			560			560		µs
Overload Recovery	50% Input Overload		3			3		µs

NOTES
[1]Does not include effects of external resistor R_G.
[2]See Table III for total RTI errors.
[3]See Applications section for input range, gain range and common-mode range.

Specifications subject to change without notice.

AD627–SPECIFICATIONS

BOTH DUAL AND SINGLE SUPPLIES

Model Specification	Conditions	AD627A Min	 Typ	 Max	AD627B Min	 Typ	 Max	Unit
NOISE								
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(eni)^2 + (eno/_G)^2}$							
Input, Voltage Noise, eni			38			38		nV/√Hz
Output, Voltage Noise, eno			177			177		nV/√Hz
RTI, 0.1 Hz to 10 Hz								
G = +5			1.2			1.2		µV p-p
G = +1000			0.56			0.56		µV p-p
Current Noise	f = 1 kHz		50			50		fA/√Hz
0.1 Hz to 10 Hz			1.0			1.0		pA p-p
REFERENCE INPUT								
R_{IN}	R_G = ∞		125			125		kΩ
Gain to Output			1			1		
Voltage Range[1]								
POWER SUPPLY								
Operating Range	Dual Supply	±1.1		±18	±1.1		±18	V
	Single Supply	2.2		36	2.2		36	V
Quiescent Current			60	85		60	85	µA
Over Temperature			200			200		nA/°C
TEMPERATURE RANGE								
For Specified Performance		–40		+85	–40		+85	°C

NOTES
[1]See Applications section for input range, gain range and common-mode range.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package (N) . . . . . 1.3 W
  Small Outline Package (R) . . . . . 0.8 W
–IN, +IN . . . . . $–V_S$ – 20 V to $+V_S$ + 20 V
Common-Mode Input Voltage . . . $–V_S$ – 20 V to $+V_S$ + 20 V
Differential Input Voltage (+IN – (–IN)) . . . . . $+V_S – (–V_S)$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range N, R . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic DIP Package: θ_{JA} = 90°C/W.
8-Lead SOIC Package: θ_{JA} = 155°C/W.

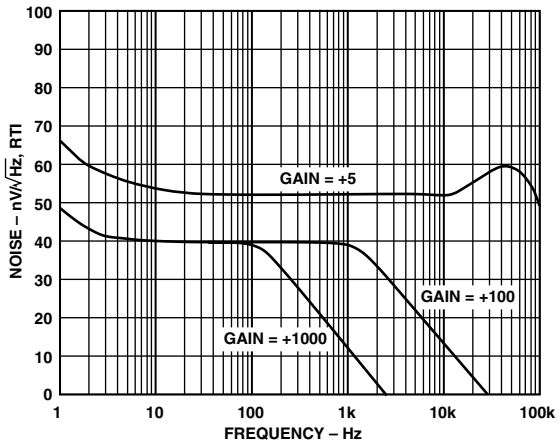
ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
AD627AN	–40°C to +85°C	Plastic DIP	N-8
AD627AR	–40°C to +85°C	Small Outline (SOIC)	SO-8
AD627AR-REEL	–40°C to +85°C	8-Lead SOIC 13" Reel	SO-8
AD627AR-REEL7	–40°C to +85°C	8-Lead SOIC 7" Reel	SO-8
AD627BN	–40°C to +85°C	Plastic DIP	N-8
AD627BR	–40°C to +85°C	Small Outline (SOIC)	SO-8
AD627BR-REEL	–40°C to +85°C	8-Lead SOIC 13" Reel	SO-8
AD627BR-REEL7	–40°C to +85°C	8-Lead SOIC 7" Reel	SO-8

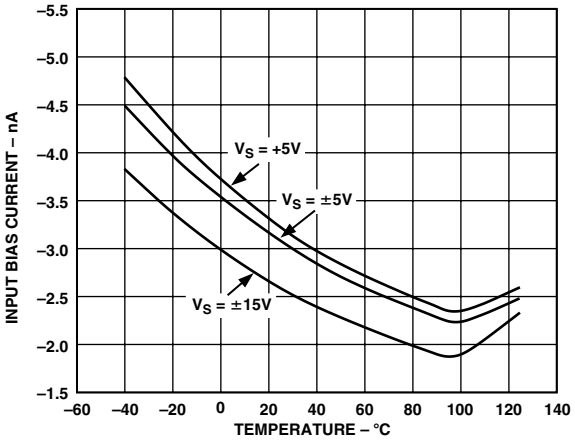
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD627 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

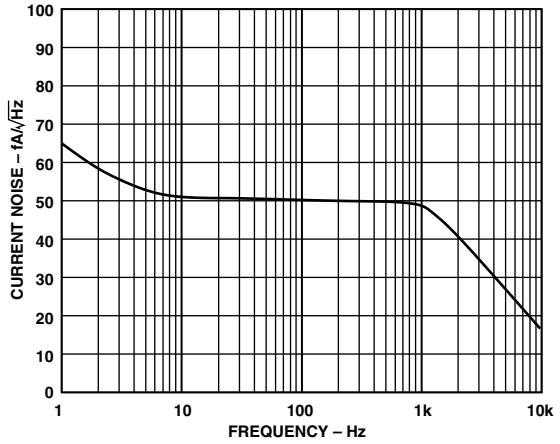
Typical Performance Characteristics (@ 25°C $V_S = \pm 5$ V, $R_L = 20\ k\Omega$ unless otherwise noted.)



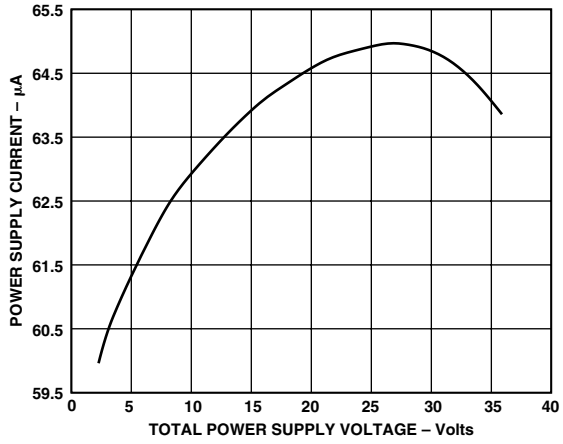
TPC 1. Voltage Noise Spectral Density vs. Frequency



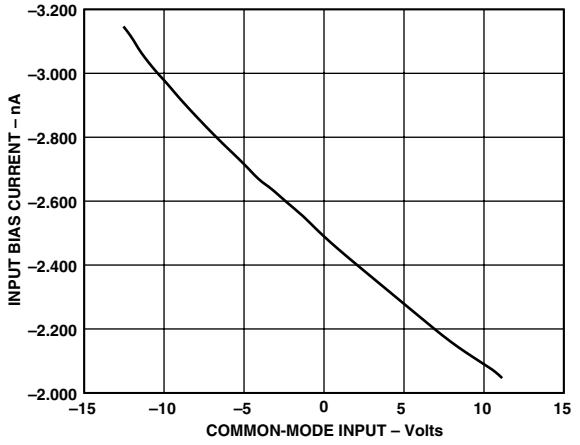
TPC 4. Input Bias Current vs. Temperature



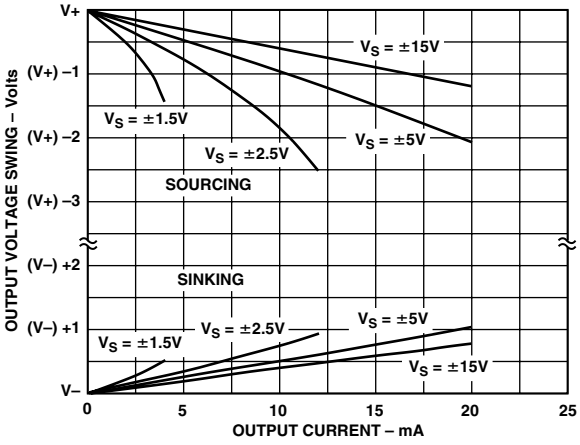
TPC 2. Current Noise Spectral Density vs. Frequency



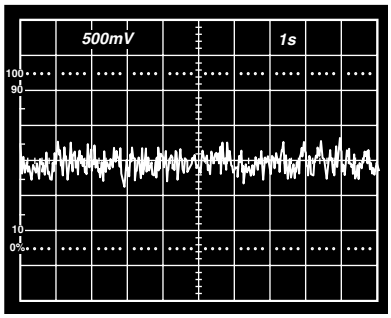
TPC 5. Supply Current vs. Supply Voltage



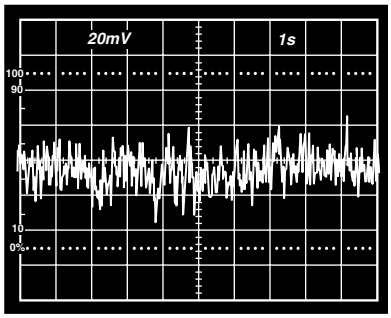
TPC 3. I_{BIAS} vs. CMV, $V_S = \pm 15$ V



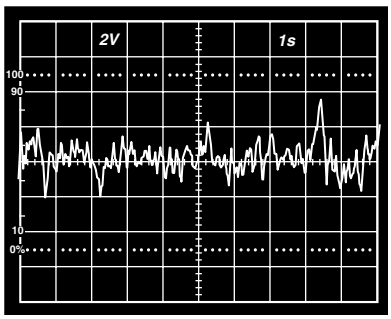
TPC 6. Output Voltage Swing vs. Output Current



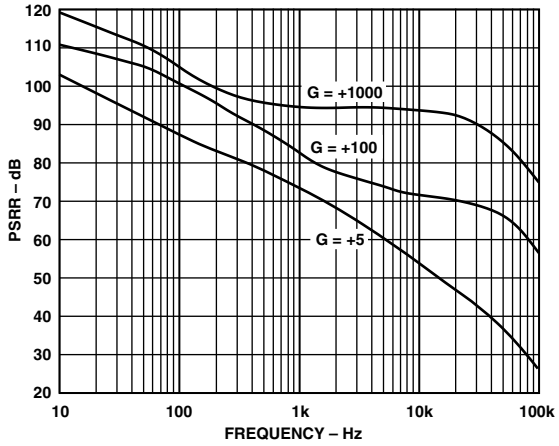
TPC 7. 0.1 Hz to 10 Hz Current Noise (0.71 pA/DIV)



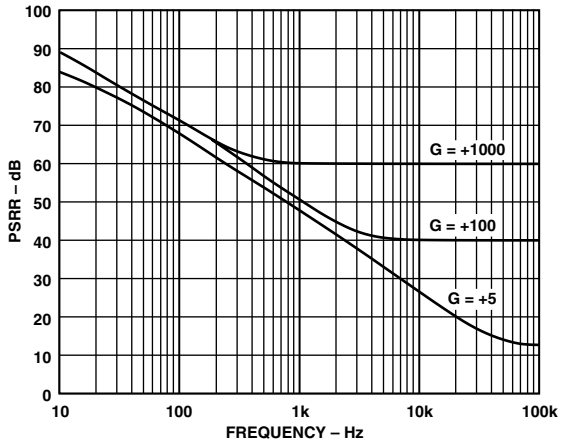
TPC 8. 0.1 Hz to 10 Hz RTI Voltage Noise (400 nV/DIV), G = +5



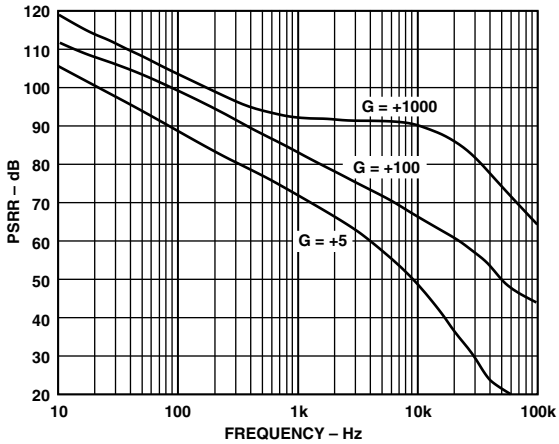
TPC 9. 0.1 Hz to 10 Hz RTI Voltage Noise (200 nV/DIV), G = +1000



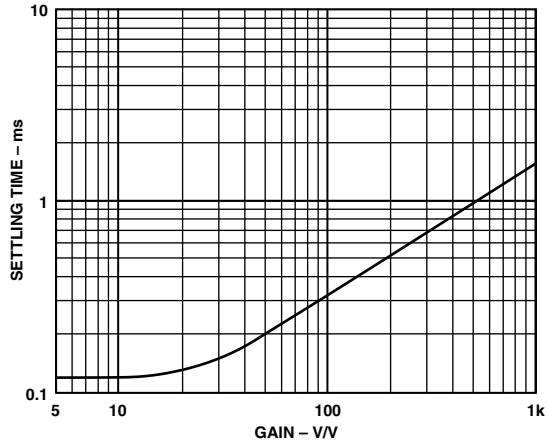
TPC 10. Positive PSRR vs. Frequency, ±5 V



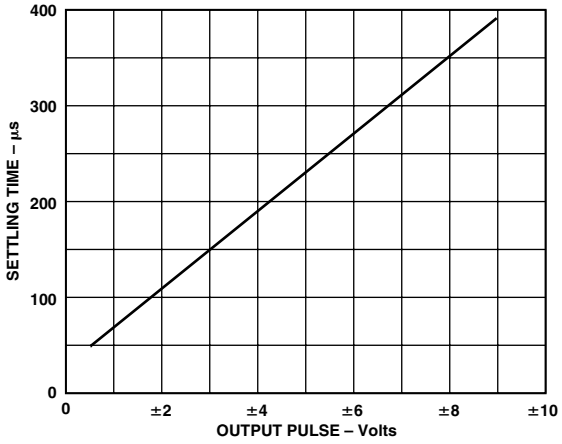
TPC 11. Negative PSRR vs. Frequency, ±5 V



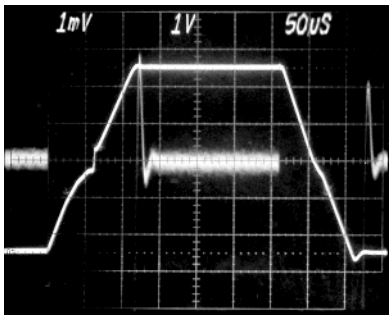
TPC 12. Positive PSRR vs. Frequency (V_S = 5 V, 0 V)



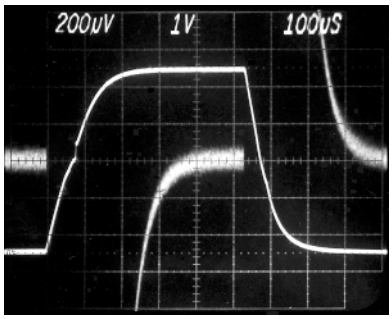
TPC 13. Settling Time to 0.01% vs. Gain for a 5 V Step at Output, R_L = 20 kΩ, C_L = 100 pF, V_S = ±5 V



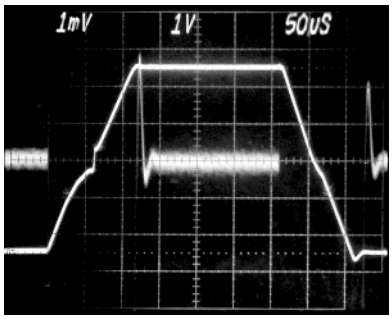
TPC 16. Settling Time to 0.01% vs. Output Swing, G = +5, R_L = 20 kΩ, C_L = 100 pF



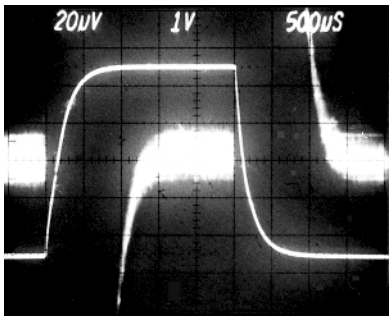
TPC 14. Large Signal Pulse Response and Settling Time, G = –5, R_L = 20 kΩ, C_L = 100 pF (1.5 mV = 0.01%)



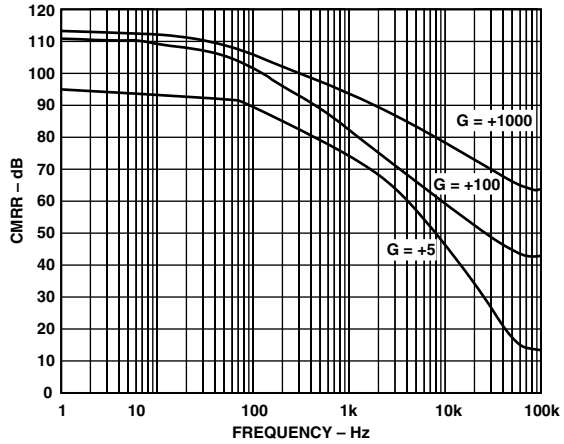
TPC 17. Large Signal Pulse Response and Settling Time, G = –100, R_L = 20 kΩ, C_L = 100 pF (100 µV = 0.01%)



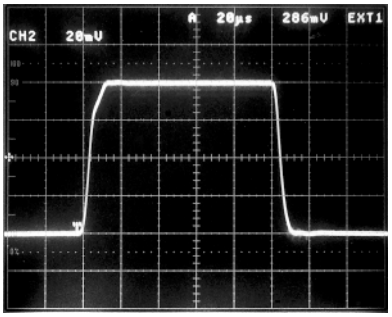
TPC 15. Large Signal Pulse Response and Settling Time, G = –10, R_L = 20 kΩ, C_L = 100 pF (1.0 mV = 0.01%)



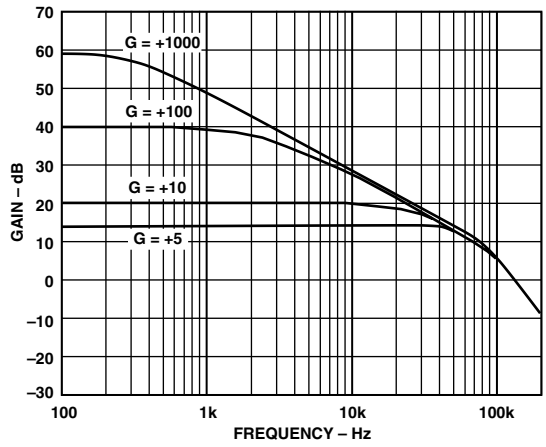
TPC 18. Large Signal Pulse Response and Settling Time, G = –1000, R_L = 20 kΩ, C_L = 100 pF (10 µV = 0.01%)



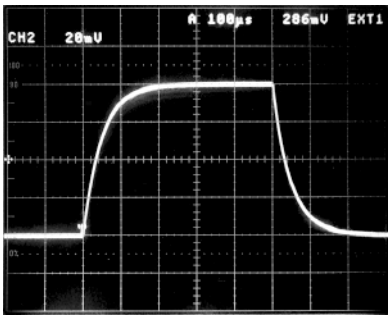
TPC 19. CMRR vs. Frequency, ±5 V_S, (CMV = 200 mV p-p)



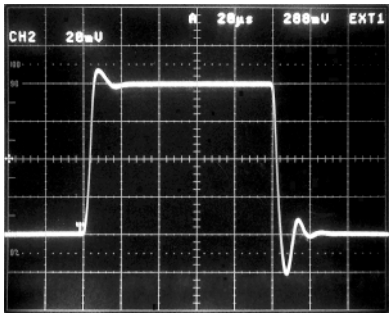
TPC 22. Small Signal Pulse Response, G = +10, R_L = 20 kΩ, C_L = 50 pF



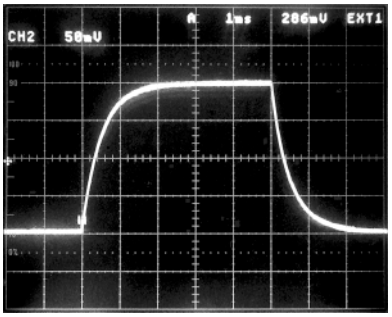
TPC 20. Gain vs. Frequency (V_S = 5 V, 0 V), V_{REF} = 2.5 V



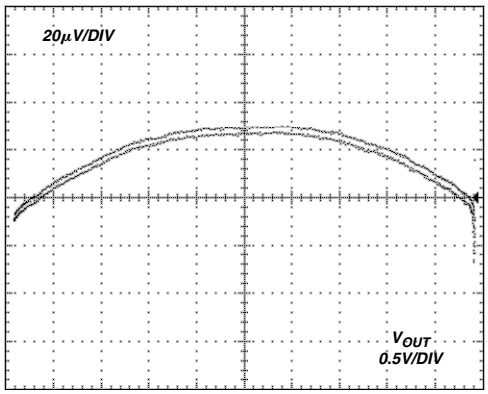
TPC 23. Small Signal Pulse Response, G = +100, R_L = 20 kΩ, C_L = 50 pF



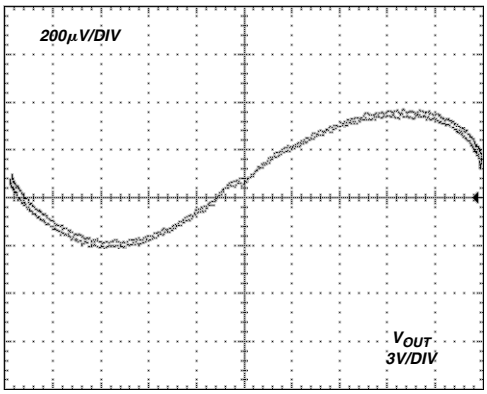
TPC 21. Small Signal Pulse Response, G = +5, R_L = 20 kΩ, C_L = 50 pF



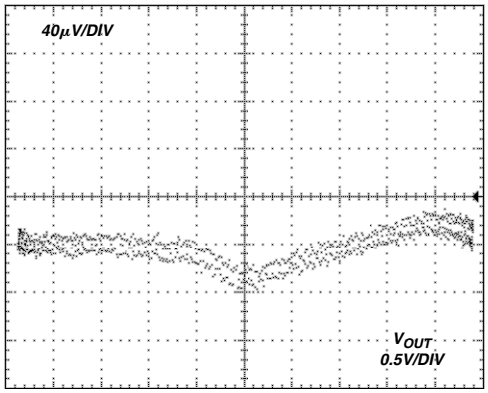
TPC 24. Small Signal Pulse Response, G = +1000, R_L = 20 kΩ, C_L = 50 pF



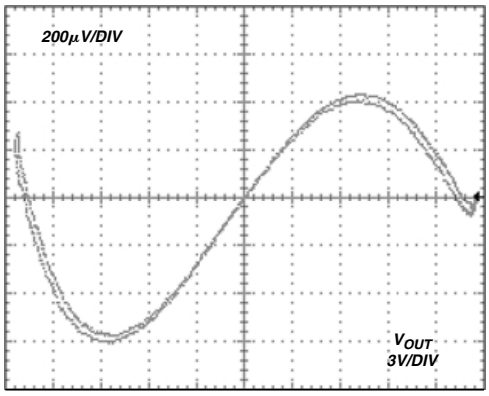
TPC 25. Gain Nonlinearity, V_S = ±2.5 V, G = +5 (4 ppm/DIV)



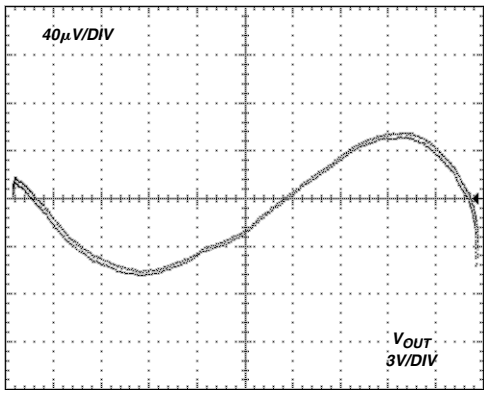
TPC 28. Gain Nonlinearity, V_S = ±15 V, G = +100 (7 ppm/DIV)



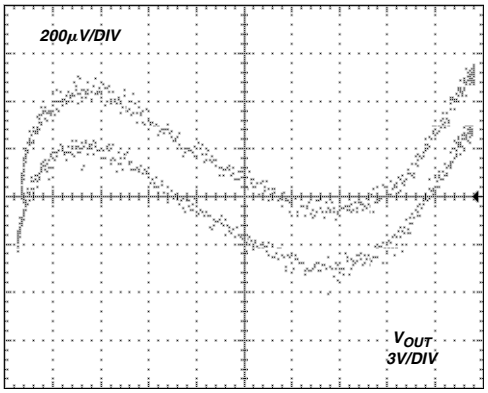
TPC 26. Gain Nonlinearity, V_S = ±2.5 V, G = +100 (8 ppm/DIV)



TPC 29. Gain Nonlinearity, V_S = ±15 V, G = +5 (7 ppm/DIV)



TPC 27. Gain Nonlinearity, V_S = ±15 V, G = +5 (1.5 ppm/DIV)



TPC 30. Gain Nonlinearity, V_S = ±15 V, G = +100 (7 ppm/DIV)

THEORY OF OPERATION

The AD627 is a true "instrumentation amplifier" built using two feedback loops. Its general properties are similar to those of the classic "two op amp" instrumentation amplifier configuration, and can be regarded as such, but internally the details are somewhat different. The AD627 uses a modified "current feedback" scheme which, coupled with interstage feedforward frequency compensation, results in a much better CMRR (Common-Mode Rejection Ratio) at frequencies above dc (notably the line frequency of 50 Hz–60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

Referring to the diagram, (Figure 2), A1 completes a feedback loop which, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume that the gain-setting resistor (R_G) is not present for the moment. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of (almost exactly) 1.25. A nearly identical feedback loop completed by A2 forces a current in Q2 which is substantially identical to that in Q1, and A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to V_{OUT} is equal to 5, whereas the gain from the output of A1 to V_{OUT} is equal to –4. The inverting terminal gain of A1, (1.25) times the gain of A2, (–4) makes the gain from the inverting and noninverting terminals equal.

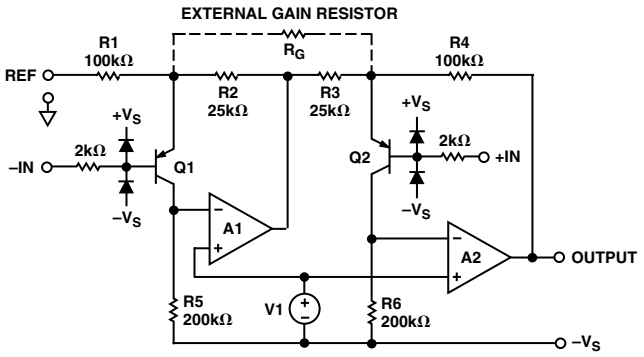


Figure 2. Simplified Schematic

The differential mode gain is equal to 1 + R4/R3, nominally five and is factory trimmed to 0.01% final accuracy. Adding an external gain setting resistor (R_G) increases the gain by an amount equal to (R4 + R1)/R_G. The output voltage of the AD627 is given by the following equation.

$$V_{OUT} = [V_{IN}(+) - V_{IN}(-)] \times (5 + 200\ k\Omega/R_G) + V_{REF}$$

Laser trims are performed on R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

USING THE AD627

Basic Connections

Figure 3 shows the basic connection circuit for the AD627. The +V_S and –V_S terminals are connected to the power supply. The supply can either be bipolar (V_S = ±1.1 V to ±18 V) or single supply (–V_S = 0 V, +V_S = +2.2 V to +36 V). The power supplies should be capacitively decoupled close to the devices power pins. For best results, use surface mount 0.1 µF ceramic chip capacitors.

The input voltage, which can be either single ended (tie either –IN or +IN to ground) or differential. The difference between the voltage on the inverting and noninverting pins is amplified by the programmed gain. The programmed gain is set by the gain resistor (see below). The output signal appears as the voltage difference between the output pin and the externally applied voltage on the REF pin (see below).

Setting the Gain

The AD627s gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The gain is set according to the equation:

$$Gain = 5 + (200\ k\Omega/R_G)$$

or

$$R_G = 200\ k\Omega/(Gain - 5)$$

It follows that the minimum achievable gain is 5 (for $R_G = \infty$). With an internal gain accuracy of between 0.05% and 0.7% depending on gain and grade, a 0.1% external gain resistor would seem appropriate to prevent significant degradation of the overall gain error. However, 0.1% resistors are not available in a wide range of values and are quite expensive. Table I shows recommended gain resistor values using 1% resistors. For all gains, the size of the gain resistor is conservatively chosen as the closest value from the standard resistor table that is higher than the ideal value. This results in a gain that is always slightly less than the desired gain. This prevents clipping of the signal at the output due to resistor tolerance.

The internal resistors on the AD627 have a negative temperature coefficient of –75 ppm/°C max for gains > 5. Using a gain resistor that also has a negative temperature coefficient of –75 ppm/°C or less will tend to reduce the overall circuit's gain drift.

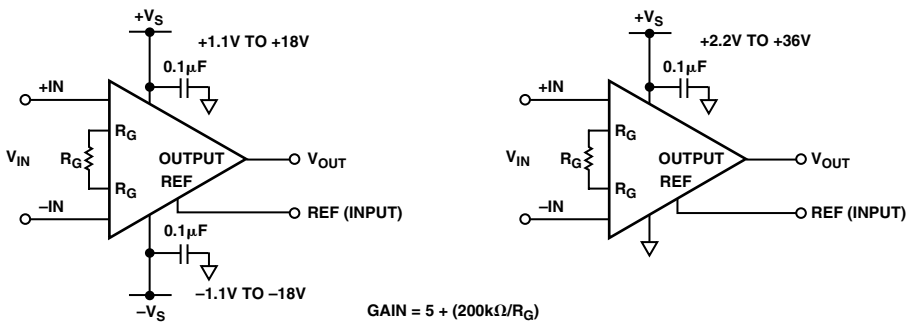


Figure 3. Basic Connections for Single and Dual Supplies

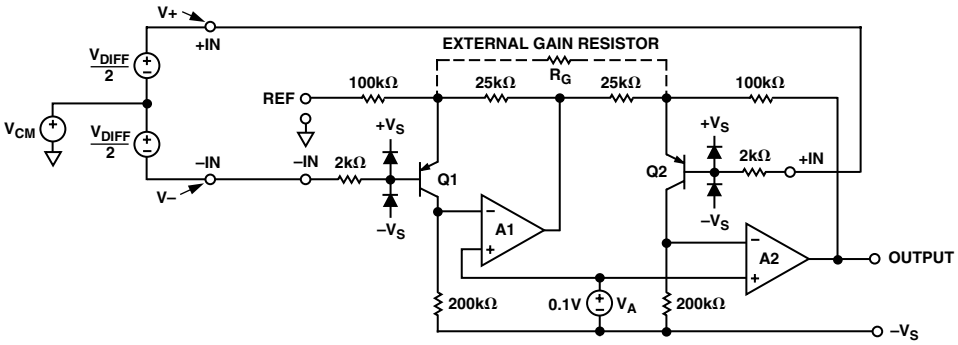


Figure 4. Amplifying Differential Signals with a Common-Mode Component

Table I. Recommended Values of Gain Resistors

Desired Gain	1% Std Table Value of R_G, Ω	Resulting Gain
5	∞	5.00
6	200 k	6.00
7	100 k	7.00
8	68.1 k	7.94
9	51.1 k	8.91
10	40.2 k	9.98
15	20 k	15.00
20	13.7 k	19.60
25	10 k	25.00
30	8.06 k	29.81
40	5.76 k	39.72
50	4.53 k	49.15
60	3.65 k	59.79
70	3.09 k	69.72
80	2.67 k	79.91
90	2.37 k	89.39
100	2.1 k	100.24
200	1.05 k	195.48
500	412	490.44
1000	205	980.61

Reference Terminal

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output. The reference terminal is also useful when bipolar signals are being amplified as it can be used to provide a virtual ground voltage.

Since the AD627 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground." The REF pin should however be tied to a low impedance point for optimal CMR.

Input Range Limitations in Single Supply Applications

In general, the maximum achievable gain is determined by the available output signal range. However, in single supply applications where the input common-mode voltage is close to or equal to zero, some limitations on the gain can be set. While the Input, Output and Reference Pins have ranges that are nominally defined on the specification pages, there is a mutual interdependence between the voltage ranges on these pins. Figure 4 shows the simplified schematic of the AD627, driven by a differential voltage V_{DIFF} which has a common-mode component, V_{CM}. The voltage on the output of op amp A1 is a function of V_{DIFF}, V_{CM}, the voltage on the REF pin and the programmed gain. This voltage is given by the equation:

$$V_{A1} = 1.25\ (V_{CM} + 0.5\ V) - 0.25\ V_{REF} - V_{DIFF}(25\ k\Omega/R_G - 0.625)$$

We can also express the voltage on A1 as a function of the actual voltages on the –IN and +IN pins (V– and V+)

$$V_{A1} = 1.25\ (V- + 0.5\ V) - 0.25\ V_{REF} - (V+ - V-)\ 25\ k\Omega/R_G$$

A1's output is capable of swinging to within 50 mV of the negative rail and to within 200 mV of the positive rail. From either of the above equations, it is clear that an increasing V_{REF}, (while it acts as a positive offset at the output of the AD627), tends to decrease the voltage on A1. Figures 5 and 6 show the maximum voltages that can be applied to the REF pin, for a gain of five for both the single and dual supply cases. Raising the input common-mode voltage will increase the voltage on the output of A1. However, in single supply applications where the common-mode voltage is low, a differential input voltage or a voltage on REF that is too high can drive the output of A1 into the ground rail. Some low side headroom is added by virtue of both inputs being shifted upwards by about 0.5 V (i.e., by the V_{BE} of Q1 and Q2). The above equations can be used to check that the voltage on amplifier A1 is within its operating range.

Table II gives values for the maximum gains for various single supply input conditions. The resulting output swings shown refer to 0 V. The voltages on the REF pins has been set to either

Table II. Maximum Gain for Low Common-Mode Single Supply Applications

V_{IN}	REF Pin	Supply Voltage	R_G (1% Tolerance)	Resulting Max Gain	Output Swing WRT 0 V
±100 mV, V_{CM} = 0 V	2 V	5 V to 15 V	28.7 kΩ	12.0	0.8 V to 3.2 V
±50 mV, V_{CM} = 0 V	2 V	5 V to 15 V	10.7 kΩ	23.7	0.8 V to 3.2 V
±10 mV, V_{CM} = 0 V	2 V	5 V to 15 V	1.74 kΩ	119.9	0.8 V to 3.2 V
V– = 0 V, V+ = 0 V to 1 V	1 V	10 V to 15 V	78.7 kΩ	7.5	1 V to 8.5 V
V– = 0 V, V+ = 0 mV to 100 mV	1 V	5 V to 15 V	7.87 kΩ	31	1 V to 4.1 V
V– = 0 V, V+ = 0 mV to 10 mV	1 V	5 V to 15 V	7.87 Ω	259.1	1 V to 3.6 V

2 V or 1 V to maximize the available gain and output swing. Note that in most cases, there is no advantage to increasing the single supply to greater than 5 V (the exception being an input range of 0 V to 1 V).

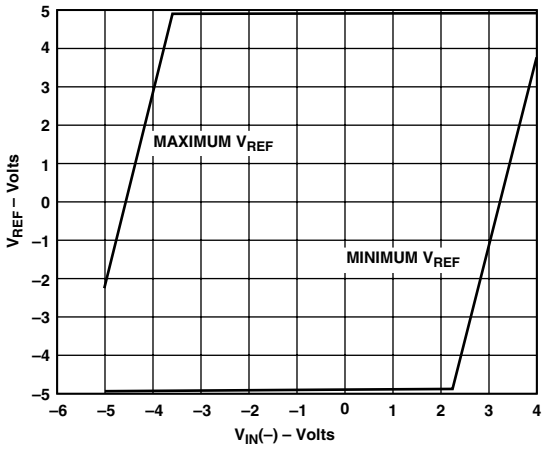


Figure 5. Reference Input Voltage vs. Negative Input Voltage, V_S = ±5 V, G = +5

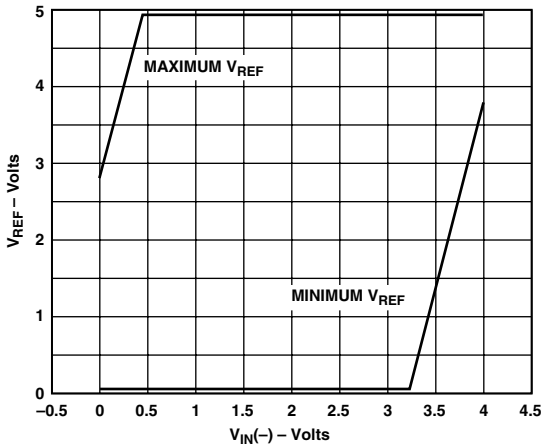


Figure 6. Reference Input Voltage vs. Negative Input Voltage, V_S = 5 V, G = +5

Output Buffering

The AD627 is designed to drive loads of 20 kΩ or greater but can deliver up to 20 mA to heavier loads at lower output voltage swings (see TPC 6). If more than 20 mA of output current is required at the output, the AD627's output should be buffered with a precision op amp such as the OP113 as shown in Figure 7 (shown for the single supply case). This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω.

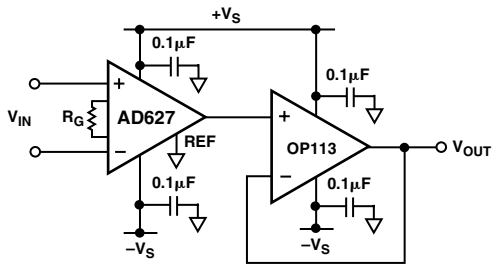


Figure 7. Output Buffering

INPUT AND OUTPUT OFFSET ERRORS

The low errors of the AD627 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total offset error for a given gain is calculated as:

Total Error RTI = Input Error + (Output Error/Gain)
Total Error RTO = (Input Error × G) + Output Error

RTI offset errors and noise voltages for different gains are shown below in Table III.

Table III. RTI Error Sources

	Max Total RTI Offset Error μV		Max Total RTI Offset Drift μV/°C		Total RTI Noise nV/√Hz
Gain	AD627A	AD627B	AD627A	AD627B	AD627A & AD627B
+5	450	250	5	3	95
+10	350	200	4	2	66
+20	300	175	3.5	1.5	56
+50	270	160	3.2	1.2	53
+100	270	155	3.1	1.1	52
+500	252	151	3	1	52
+1000	251	151	3	1	52

Make vs. Buy: A Typical Application Error Budget

The example in Figure 8 serves as a good comparison between the errors associated with an integrated and a discrete in amp implementation. A ±100 mV signal from a resistive bridge (common-mode voltage = 2.5 V) is to be amplified. This example compares the resulting errors from a discrete two op amp in amp and from the AD627. The discrete implementation uses a four-resistor precision network (1% match, 50 ppm/°C tracking).

The errors associated with each implementation are detailed in Table IV and show the integrated in amp to be more precise, both at ambient and over temperature. It should be noted that the discrete implementation is also more expensive. This is primarily due to the relatively high cost of the low drift precision resistor network.

Note, the input offset current of the discrete in amp implementation is the difference in the *bias* currents of the two op amps, not the offset currents of the individual op amps. Also, while the values of the resistor network are chosen so that the inverting and noninverting inputs of each op amp see the same impedance (about 350 Ω), the offset current of each op amp will add an additional error which must be characterized.

Errors Due to AC CMRR

In Table IV, the error due to common-mode rejection is the error that results from the common-mode voltage from the bridge 2.5 V. The ac error due to nonideal common-mode rejection cannot be calculated without knowing the size of the ac common-mode voltage (usually interference from 50 Hz/60 Hz mains frequencies).

A mismatch of 0.1% between the four gain setting resistors will determine the low frequency CMRR of a two op amp in amp. The plot in Figure 8 shows the practical results, at ambient temperature, of resistor mismatch. The CMRR of the circuit in Figure 9 (Gain = +11) was measured using four resistors which

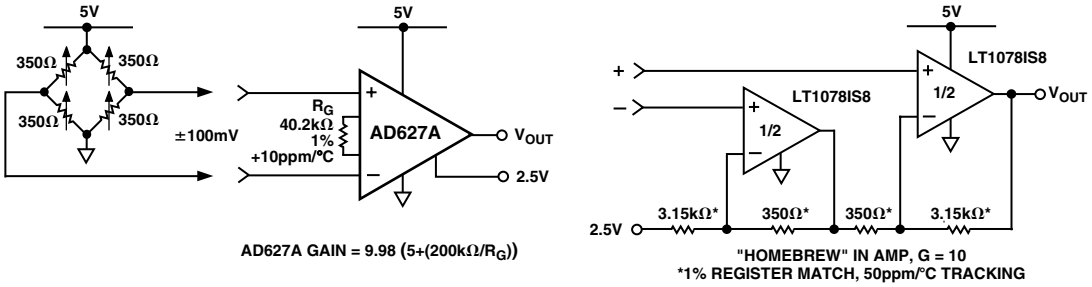


Figure 8. Make vs. Buy

Table IV. Make vs. Buy Error Budget

Error Source	AD627 Circuit Calculation	"Homebrew" Circuit Calculation	Total Error AD627-ppm	Total Error Homebrew–ppm
ABSOLUTE ACCURACY at T_A = 25°C				
Total RTI Offset Voltage, mV	(250 µV + (1000 µV/10))/100 mV	(180 µV × 2)/100 mV	3500	3600
Input Offset Current, nA	1 nA × 350 Ω/100 mV	20 nA × 350 Ω/100 mV	3.5	70
Internal Offset Current (Homebrew Only)	Not Applicable	0.7 nA × 350 Ω/100 mV		2.45
CMRR, dB	77 dB→141 ppm × 2.5 V/100 mV	(1% Match × 2.5 V)/10/100 mV	3531	25000
Gain	0.35% + 0.1%	1% Match	13500	10000
		Total Absolute Error	**20535**	**38672**
DRIFT TO 85°C				
Gain Drift, ppm/°C	(–75 + 10) ppm/°C × 60°C	50 ppm/°C × 60°C	3900	3000
Total RTI Offset Voltage, mV/°C	(3.0 µV/°C + (10 µV/°C/10)) × 60°C/100 mV	(2 × 3.5 µV/°C × 60°C)/100 mV	2600	4200
Input Offset Current, pA/°C	(16 pA/°C × 350 Ω × 60°C)/100 mV	(33 pA/°C × 350 Ω × 60°C)/100 mV	3.5	7
		Total Drift Error	**6504**	**7207**
		Grand Total Error	**27039**	**45879**

had a mismatch of almost exactly 0.1% (R1 = 9999.5 Ω, R2 = 999.76 Ω, R3 = 1000.2 Ω, R4 = 9997.7 Ω). As expected the CMRR at dc was measured at about 84 dB (calculated value is 85 dB). However, as the frequency increases, the CMRR quickly degrades. For example, a 200 mV peak-peak harmonic of the mains frequency at 180 Hz would result in an output voltage of about 800 µV. To put this in context, a 12-bit data acquisition system with an input range of 0 V to 2.5 V, has an LSB weighting of 610 µV.

By contrast, the AD627 uses precision laser trimming of internal resistors along with patented CMR trimming to yield a higher dc CMRR and a wider bandwidth over which the CMRR is flat (see TPC 19).

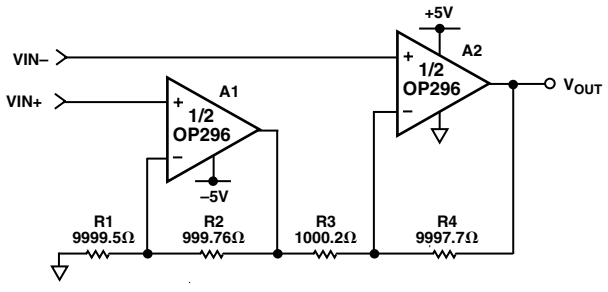


Figure 9. 0.1% Resistor Mismatch Example

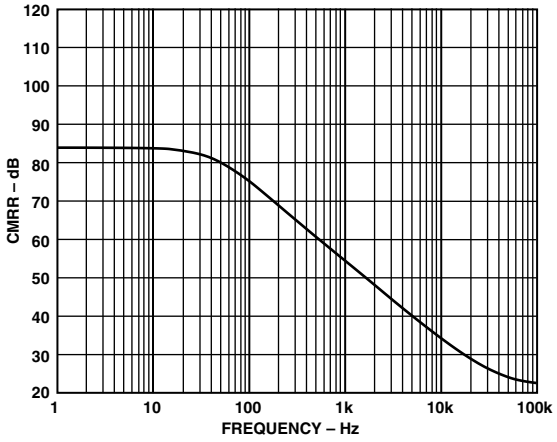


Figure 10. CMRR Over Frequency of Discrete In Amp in Figure 9

Ground Returns for Input Bias Currents

Input bias currents are those dc currents that must flow in order to bias the input transistors of an amplifier. These are usually transistor base currents. When amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a direct dc path into each input in order that the bias current can flow. Figure 11 shows how a bias current path can be provided for the case of transformer coupling, capacitive ac-coupling and for a thermocouple application.

In dc-coupled resistive bridge applications, providing this path is generally not necessary as the bias current simply flows from the bridge supply, through the bridge and into the amplifier. However, if the impedance that the two inputs see are large, and differ by a large amount (>10 kΩ), the offset current of the input stage will cause dc errors compatible with the input offset voltage of the amplifier.

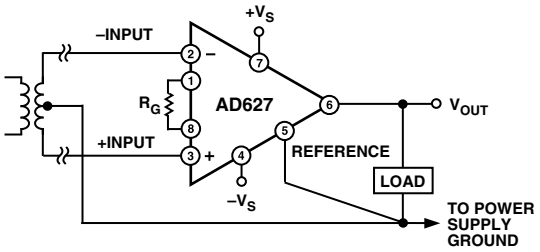


Figure 11a. Ground Returns for Bias Currents with Transformer Coupled Inputs

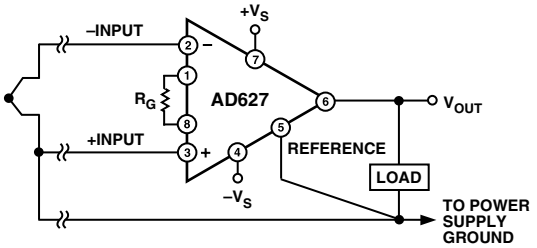


Figure 11b. Ground Returns for Bias Currents with Thermocouple Inputs

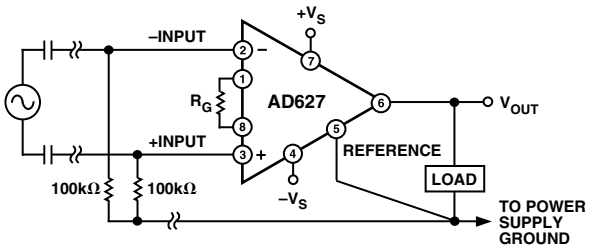


Figure 11c. Ground Returns for Bias Currents with AC Coupled Inputs

Layout and Grounding

The use of ground planes is recommended to minimize the impedance of ground returns (and hence the size of dc errors). In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground returns (Figure 12). All ground pins from mixed signal components such as analog-to-digital converters should be returned through the "high quality" analog ground plane. Digital ground lines of mixed signal components should also be returned through the analog ground plane. This may seem to break the rule of keeping analog and digital grounds separate. However, in general, there is also a requirement to keep the voltage difference between digital and analog grounds on a converter as small as possible (typically <0.3 V). The increased noise, caused by the converter's digital return currents flowing through the analog ground plane, will generally be negligible. Maximum isolation between analog and digital is achieved by connecting the ground planes back at the supplies.

If there is only a single power supply available, it must be shared by both digital and analog circuitry. Figure 13 shows the how to minimize interference between the digital and analog circuitry. As in the previous case, separate analog and digital ground planes should be used (reasonably thick traces can be used as an alternative to a digital ground plane). These ground planes should be connected at the power supply's ground pin. Separate traces (or power planes) should be run from the power supply to the supply pins of the digital and analog circuits. Ideally each device should have its own power supply trace, but these can be shared by a number of devices as long as a single trace is not used to route current to both digital and analog circuitry.

INPUT PROTECTION

As shown in the simplified schematic (Figure 2), both the inverting and noninverting inputs are clamped to the positive and negative supplies by ESD diodes. In addition to this a 2 kΩ series resistor on each input provides current limiting in the event of an overvoltage. These ESD diodes can tolerate a maximum continuous current of 10 mA. So an overvoltage, (that is the amount by which input voltage exceeds the supply voltage), of ±20 V can be tolerated. This is true for all gains, and for power on and off. This last case is particularly important since the signal source and amplifier may be powered separately.

If the overvoltage is expected to exceed 20 V, additional external series resistors current limiting resistors should be used to keep the diode current to below 10 mA.

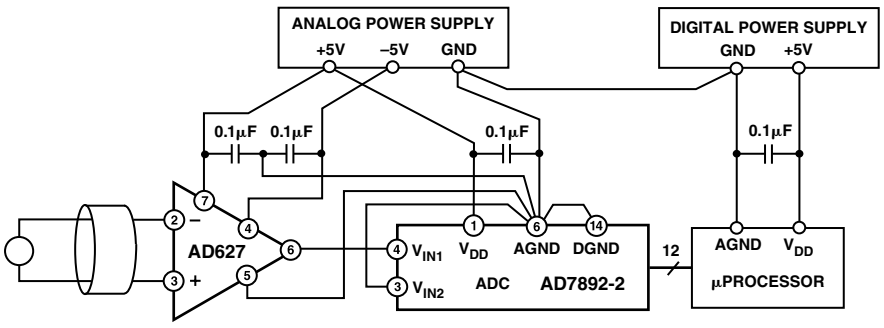


Figure 12. Optimal Grounding Practice for a Bipolar Supply Environment with Separate Analog and Digital Supplies

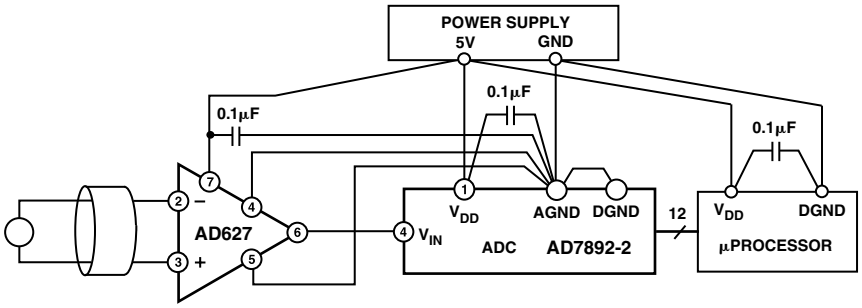


Figure 13. Optimal Ground Practice in a Single Supply Environment

RF INTERFERENCE

All instrumentation amplifiers can rectify high frequency out-of-band signals. Once rectified, these signals appear as dc offset errors at the output. The circuit of Figure 14 provides good RFI suppression without reducing performance within the in amp's passband. Resistor R1 and capacitor C1 (and likewise, R2 and C2) form a low pass RC filter that has a –3 dB BW equal to: $F = 1/(2\pi R1C1)$. Using the component values shown, this filter has a –3 dB bandwidth of approximately 8 kHz. Resistors R1 and R2 were selected to be large enough to isolate the circuit's input from the capacitors, but not large enough to significantly increase the circuit's noise. To preserve common-mode rejection in the amplifier's pass band, capacitors C1 and C2 need to be 5% mica units, or low cost 20% units can be tested and "binned" to provide closely matched devices.

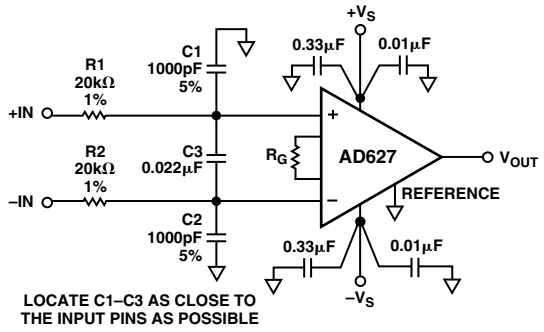


Figure 14. Circuit to Attenuate RF Interference

Capacitor C3 is needed to maintain common-mode rejection at the low frequencies. R1/R2 and C1/C2 form a bridge circuit whose output appears across the in amp's input pins. Any mismatch between C1 and C2 will unbalance the bridge and reduce common-mode rejection. C3 insures that any RF signals are common mode (the same on both in amp inputs) and are not applied differentially. This second low pass network, R1 + R2 and C3, has a –3 dB frequency equal to: $1/(2\pi (R1 + R2) (C3))$. Using a C3 value of 0.022 μF as shown, the –3 dB signal BW of this circuit is approximately 200 Hz. The typical dc offset shift over frequency will be less than 1 mV and the circuit's RF signal rejection will be better than 57 dB. The 3 dB signal bandwidth of this circuit may be increased by reducing the value of resistors R1 and R2. The performance is similar to that using 20 kΩ resistors, except that the circuitry preceding the in amp must drive a lower impedance load.

The circuit of Figure 14 should be built using a PC board with a ground plane on both sides. All component leads should be as short as possible. Resistors R1 and R2 can be common 1% metal film units but capacitors C1 and C2 need to be ±5% tolerance devices to avoid degrading the circuit's common-mode rejection. Either the traditional 5% silver mica units or Panasonic ±2% PPS film capacitors are recommended.

APPLICATIONS CIRCUITS

A Classic Bridge Circuit

Figure 15 shows the AD627 configured to amplify the signal from a classic resistive bridge. This circuit will work in either dual or single supply mode. Typically the bridge will be excited by the same voltage as is used to power the in amp. Connecting the bottom of the bridge to the negative supply of the in amp (usually either 0, –5 V, –12 V or –15 V), sets up an input common-mode voltage that is optimally located midway between the supply voltages. It is also appropriate to set the voltage on the REF pin to midway between the supplies, especially if the input signal will be bipolar. However the voltage on the REF pin can be varied to suit the application. A good example of this is when the REF pin is tied to the V_{REF} pin of an Analog-to-Digital Converter (ADC) whose input range is $(V_{REF} \pm V_{IN})$. With an available output swing on the AD627 of $(-V_S + 100\text{ mV})$ to $(+V_S - 150\text{ mV})$ the maximum programmable gain is simply this output range divided by the input range.

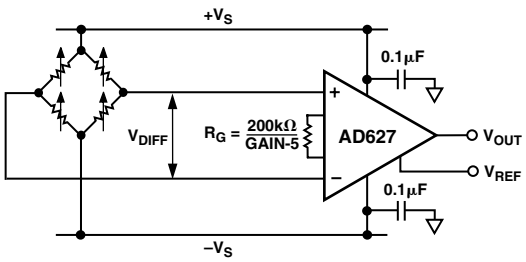


Figure 15. A Classic Bridge Circuit

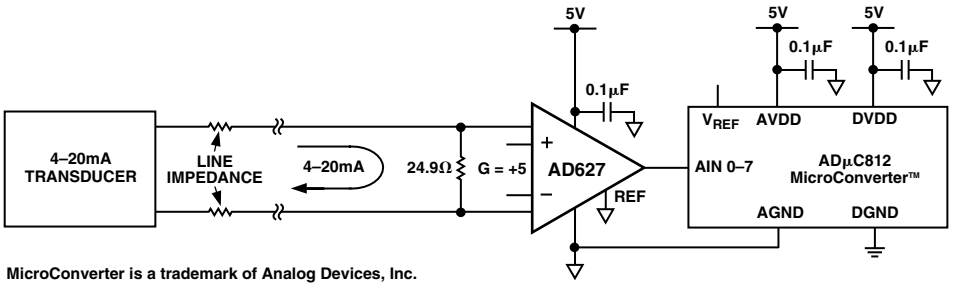


Figure 16. A 4 mA-to-20 mA Receiver Circuit

A 4 mA-to-20 mA Single Supply Receiver

Figure 16 shows how a signal from a 4 mA-to-20 mA transducer can be interfaced to the ADμC812, a 12-bit ADC with an embedded microcontroller. The signal from a 4 mA-to-20 mA transducer is single ended. This initially suggests the need for a simple shunt resistor, to convert the current to a voltage at the high impedance analog input of the converter. However, any line resistance in the return path (to the transducer) will add a current dependent offset error. So the current must be sensed differentially.

In this example, a 24.9 Ω shunt resistor generates a maximum differential input voltage to the AD627 of between 100 mV (for 4 mA in) and 500 mV (for 20 mA in). With no gain resistor present, the AD627 amplifies the 500 mV input voltage by a factor of 5, to 2.5 V, the full-scale input voltage of the ADC. The zero current of 4 mA corresponds to a code of 819 and the LSB size is 4.9 mA.

A Thermocouple Amplifier

Because the common-mode input range of the AD627 extends 0.1 V below ground, it is possible to measure small differential signals which have low, or no, common-mode component. Figure 17 shows a thermocouple application where one side of the J-type thermocouple is grounded.

Over a temperature range from –200°C to +200°C, the J-type thermocouple delivers a voltage ranging from –7.890 mV to 10.777 mV. A programmed gain on the AD627 of 100 (R_G = 2.1 kΩ) and a voltage on the AD627 REF pin of 2 V, results in the AD627's output voltage ranging from 1.110 V to 3.077 V relative to ground. For a different input range or different voltage on the REF pin, it is important to check that the voltage on internal node A1 (see Figure 4) is not driven below ground). This can be checked using the equations in the section entitled Input Range Limitations in Single Supply Applications.

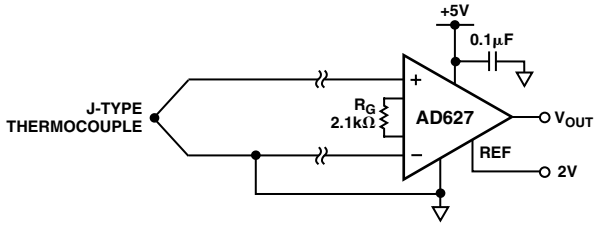
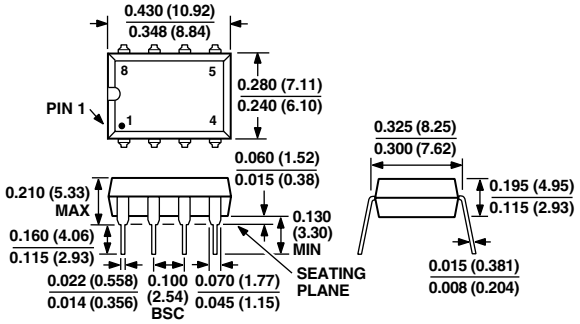


Figure 17. Amplifying Bipolar Signals with Low Common-Mode Voltage

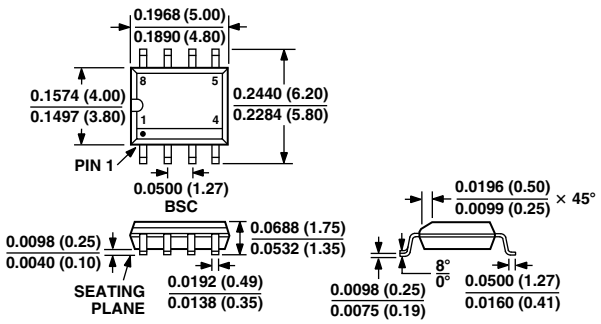
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



AD627–Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Changes to Figure 4 and Table I, Resulting Gain column	11
Change to Figure 9	13