High-Bandwidth, Low Voltage, Dual SPDT Analog Switchs

FEATURES

- Single Supply (1.8 V to 5.5 V)
- Low On-Resistance - $r_{ON:}$ 2.4 Ω
- Crosstalk and Off Isolation: -81 dB @ 1 MHz
- MSOP-10 Package

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- Low-Voltage Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Low-Voltage Data Acquisition
- ATE

DESCRIPTION

The DG2016/DG2026 are monolithic CMOS dual single-pole/double-throw (SPDT) analog switchs. They are specifically designed for low-voltage, high bandwidth applications.

The DG2016/DG2026's on-resistance (3 Ω @ 2.7 V), matching and flatness are guaranteed over the entire analog voltage range. Wide dynamic performance is achieved with better than –80 dB for both cross-talk and off-isolation at 1 MHz.

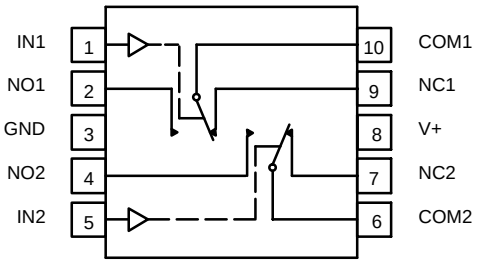
Both SPDT's operate with independent control logic, conduct equally well in both directions and block signals up to the power supply level when off. Break-before-make is guaranteed.

With fast switching speeds, low on-resistance, high bandwidth, and low charge injection, the DG2016/DG2026 are ideally suited for audio and video switching with high linearity.

Built on Vishay Siliconix's low voltage CMOS technology, the DG2016/DG2026 contain an epitaxial layer which prevents latch-up.

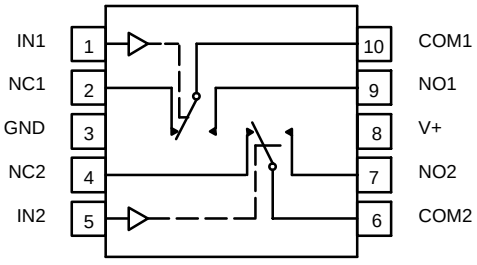
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2016DQ—MSOP-10



Top View

DG2026DQ—MSOP-10



Top View

TRUTH TABLE		
Logic	**NC1 and NC2**	**NO1 and NO2**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	MSOP-10	DG2016DQ
		DG2026DQ

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ . . . . . -0.3 to +6 V
IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) . . . . . ±50 mA
Peak Current . . . . . ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) . . . . . -65 to 150°C

Power Dissipation (Packages)[b]
MSOP-10[c] . . . . . 320 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 4.0 mW/°C above 70°C

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V I_{NO}, I_{NC} = 10 mA	Room Full		3.0	4.8 5.3	Ω
r_{ON} Flatness	r_{ON} Flatness	V+ = 2.7 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			1.6	Ω
r_{ON} Match Between Channels	Δr_{ON}		Room			0.2	Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 0.3 V/3 V V_{COM} = 3 V/0.3 V	Room Full	-1 -10		1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10		1 10	nA
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3 V	Room Full	-1 -10		1 10	nA
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance	C_{in}		Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Room Full		28	53 59	ns
Turn-Off Time	t_{OFF}		Room Full		13	38 38	ns
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 2.0 V, R_L = 50 Ω, C_L = 35 pF	Full	1			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		38		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-78		dB
Crosstalk[d]	X_{TALK}		Room		-82		dB
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		15		pF
	$C_{NC(off)}$		Room		15		pF
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		49		pF
	$C_{NC(on)}$		Room		45		pF
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+	Full		0.01	1.0	µA

Notes:

a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

SPECIFICATIONS (V+ = 5 V)

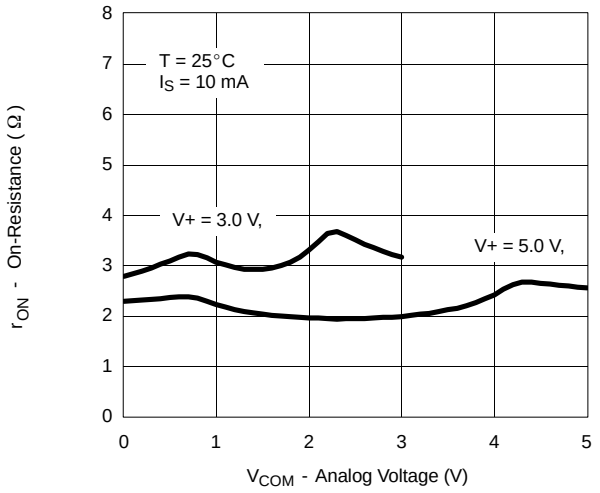
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.5 V, V_{COM} = 3 V, I_{NO}, I_{NC} = 10 mA	Room Full		2.4	4.0 4.3	Ω
r_{ON} Flatness	r_{ON} Flatness	V+ = 4.5 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			1.2	Ω
r_{ON} Match Between Channels	Δr_{ON}	V+ = 4.5 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			0.2	Ω
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	-1 -10		1 10	nA
	$I_{COM(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	-1 -10		1 10	nA
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	-1 -10		1 10	nA
Digital Control							
Input High Voltage[d]	V_{INH}		Full	2.0			V
Input Low Voltage	V_{INL}		Full			0.8	V
Input Capacitance	C_{in}		Full		5		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 50 Ω, C_L = 35 pF	Room Full		23	48 52	ns
Turn-Off Time	t_{OFF}	V_{NO} or V_{NC} = 3 V, R_L = 50 Ω, C_L = 35 pF	Room Full		8	33 35	ns
Break-Before-Make Time	t_d	V_{NO} or V_{NC} = 3 V, R_L = 50 Ω, C_L = 35 pF	Full	1			ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		79		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-81		dB
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-82		dB
Source-Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		14		pF
	$C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		14		pF
Channel-On Capacitance[d]	$C_{NO(on)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		48		pF
	$C_{NC(on)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		44		pF
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full		0.01	1.0	µA

Notes:

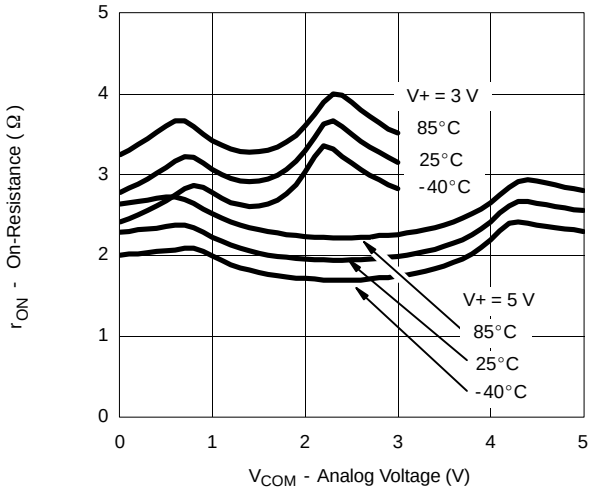
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

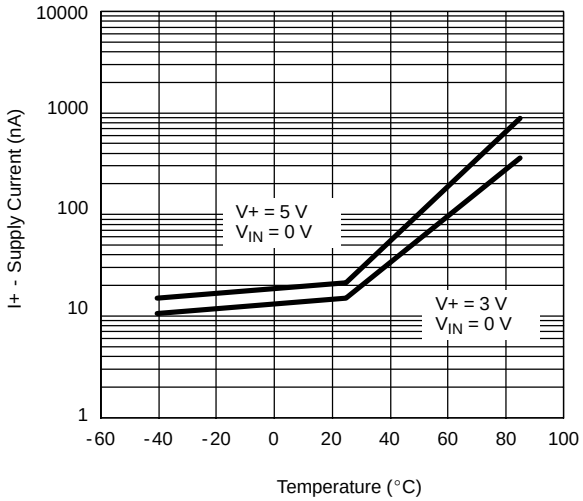
r_{ON} vs. V_{COM} and Supply Voltage



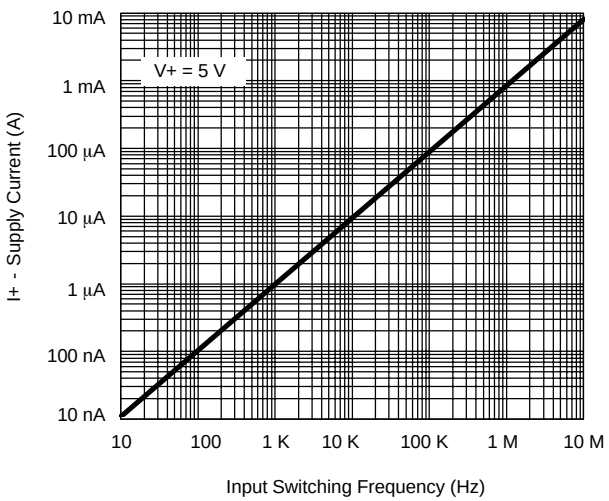
r_{ON} vs. Analog Voltage and Temperature



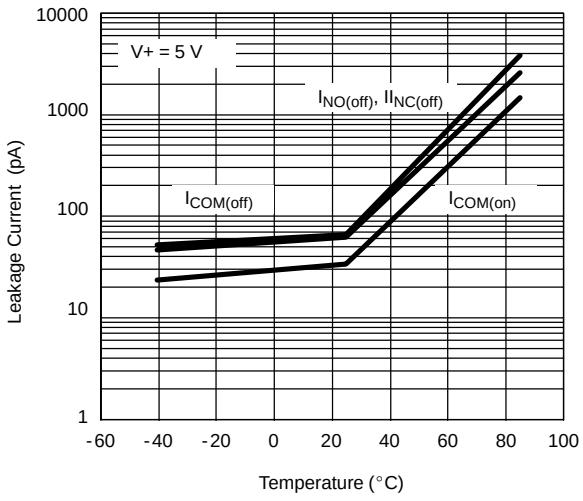
Supply Current vs. Temperature



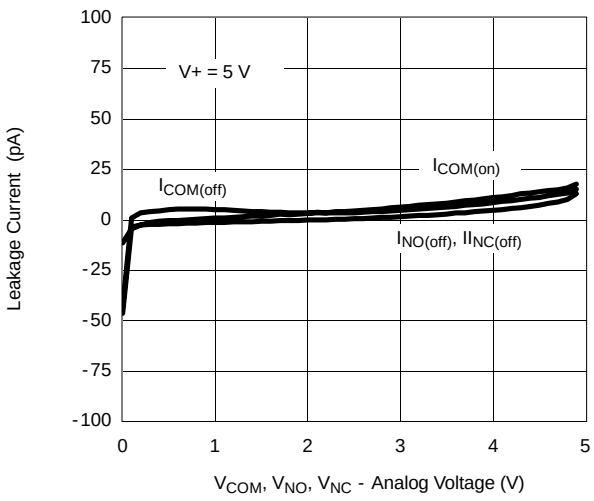
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

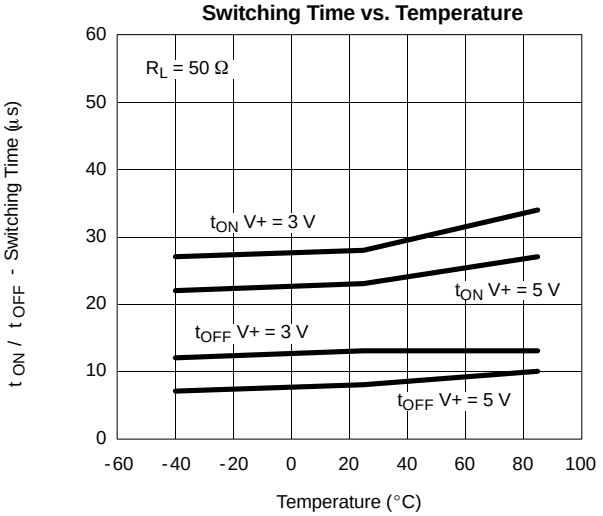


Leakage vs. Analog Voltage

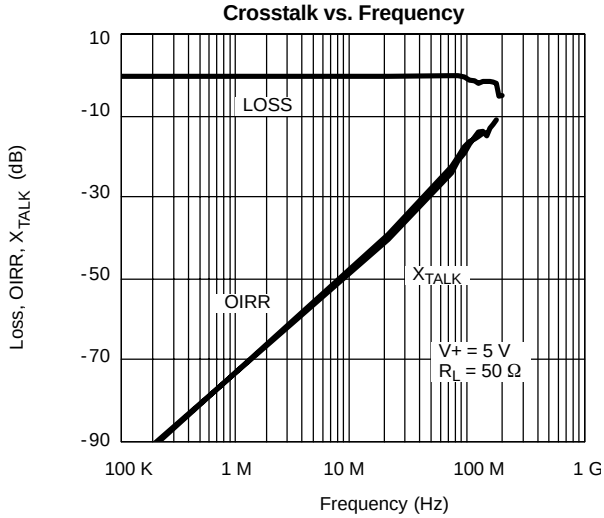


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

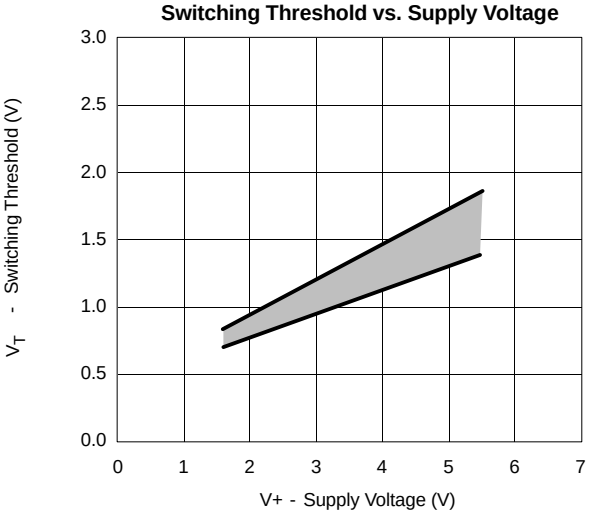
Switching Time vs. Temperature



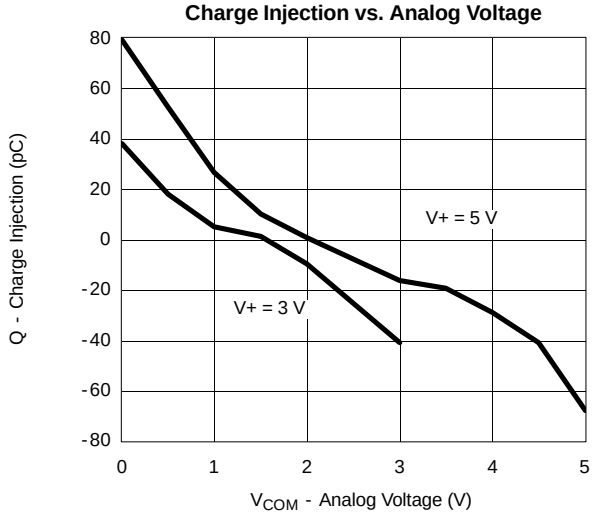
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



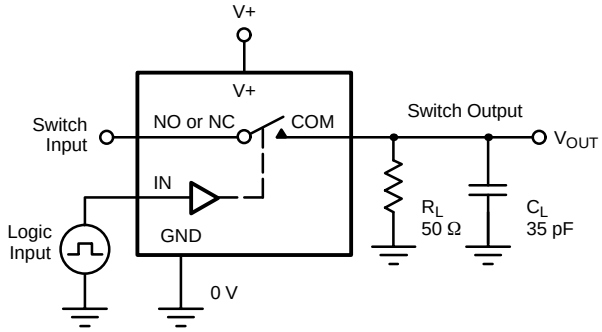
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

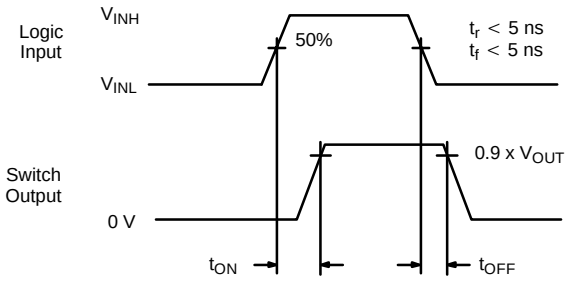


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

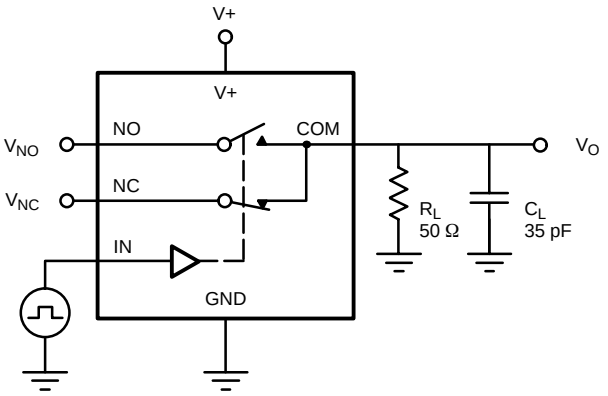
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

TEST CIRCUITS



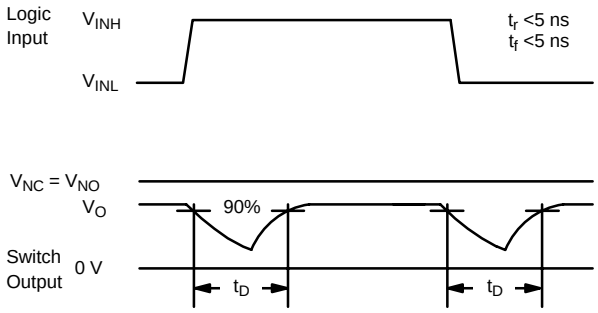
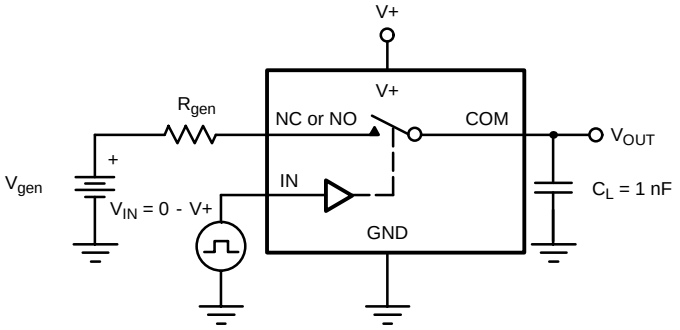
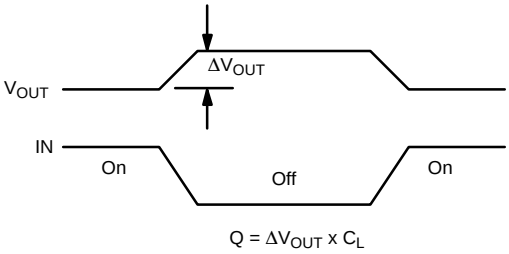


FIGURE 5. Break-Before-Make Interval





IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

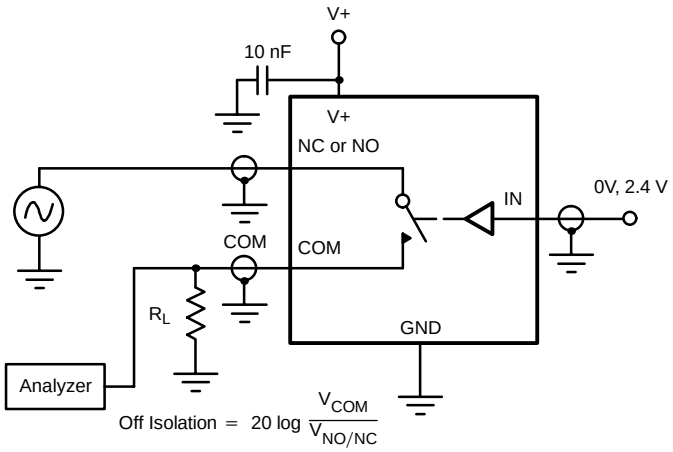


FIGURE 3. Off-Isolation

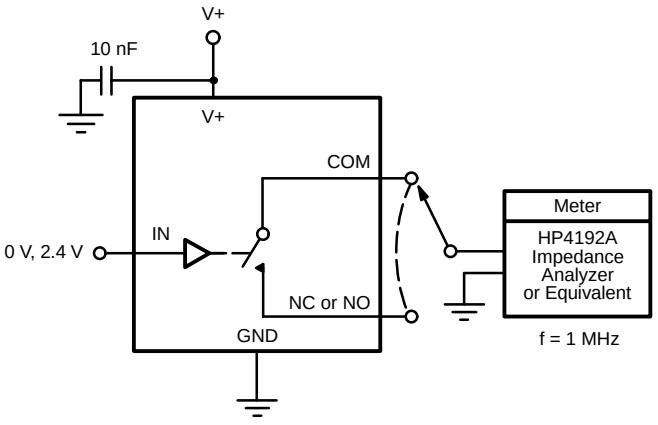


FIGURE 4. Channel Off/On Capacitance