SC1477
ADVANCED CPU POWER SUPPLY

Description

The SC1477 is a single chip high-performance Hysteretic controller. With its integrated Smart™ Driver, it powers AMD Duron and Transmeta CPUs, directly supporting on-the-fly VID changes required by these processors. The SC1477 eliminates an external multiplexer by allowing the output voltage for start-up (and sleep mode) to be set with an external resistor. The SC1477 also incorporates automatic "power-save" to prevent negative current flow in the low-side FET during light loading conditions.

A 5-bit DAC, accurate to 1%, sets the output voltage reference and implements the 0.925V to 2.00V range required by the processor. The hysteretic converter uses a comparator without an error amplifier, and therefore provides the fastest possible transient response, while avoiding the stability issues inherent to classical PWM controllers.

The SC1477 operates from 5Vdc and also features soft-start, an open-drain PWRGD signal with blanking, and an enable input. Programmable current limiting shuts the SC1477 down after 32 current limit pulses. It is available in a space saving TSSOP-24 package.

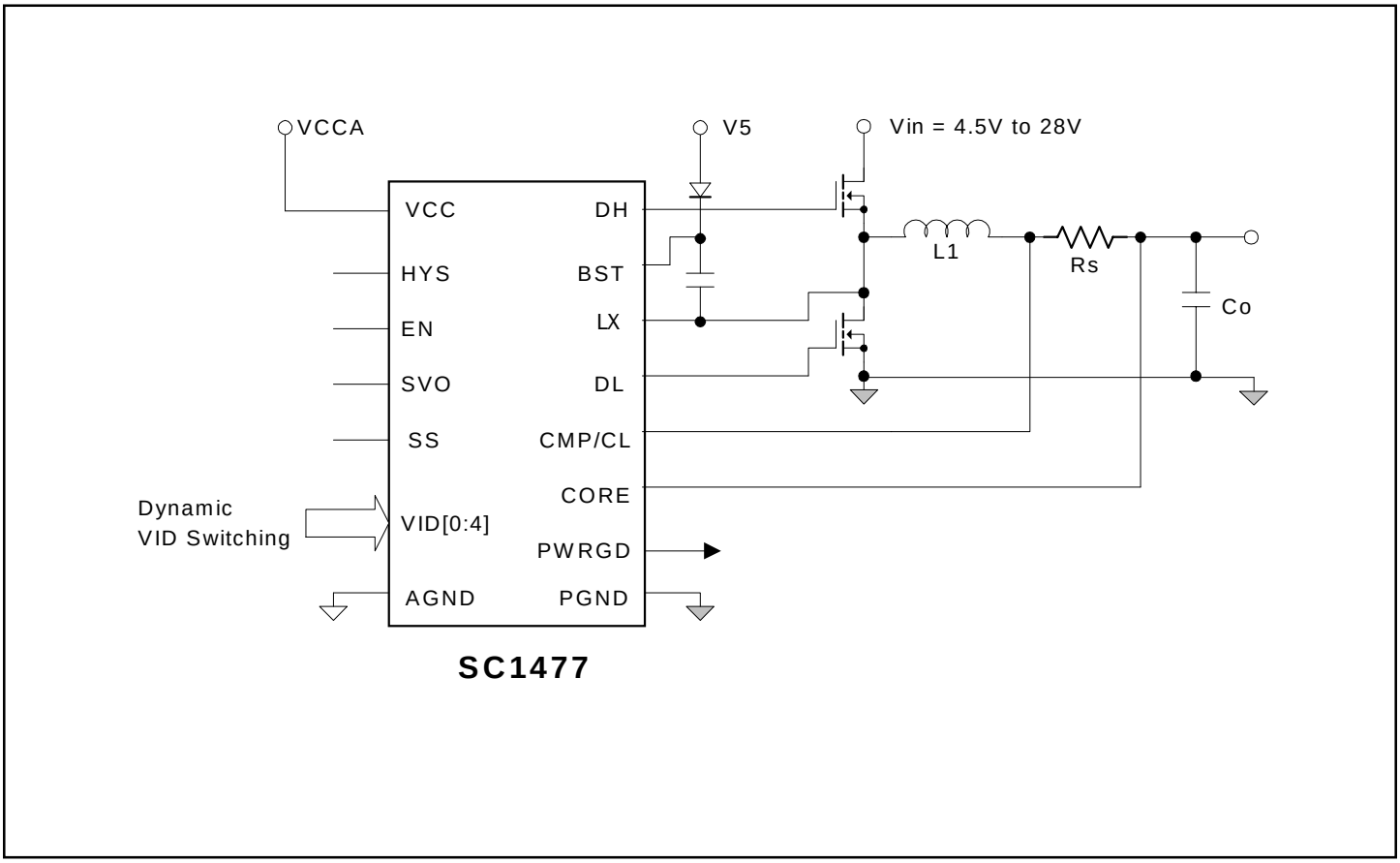
Features

- Complete single-chip Vcore solution
- 5-bit VID code (0.925V to 2.0V)
- 1% output accuracy
- Support continuous VID changes required for AMD Power Now™ and Transmeta LongRun™ operation
- High efficiency over a wide operating range
- Fast transient response
- High-speed gate drive capable of driving multiple MOSFETs (4A drive current)
- PWRGD with blanking during VID changes
- Precision current sense and Over-current protection
- Over-voltage and over-temperature shutdown

Applications

- Notebook Computer CPUs
- Internet appliances
- Network server power supplies
- Power PC CPUs

Conceptual Application Circuit



Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MAXIMUM / UNITS
$V_{CCA,}$ V5	Supply Voltage	-0.3V to +7V
$V_{VSLP,}$ $V_{SVO,}$ $V_{VID(0..4),}$ $V_{DAC,}$ $V_{CMP,}$ $V_{HYS,}$ $V_{CORE,}$ $V_{CL,}$ $V_{CLRF,}$ $V_{PWRGD,}$ V_{DL}	Input and Output voltages	-0.3V, V_{CCA}+0.3V
V_{EN}	EN	-0.3V to +7V
	BST to PGND	-0.3V to 36V DC 40V Transient, 100ns
	BST to LX	-0.3V to 7V
	LX to PGND	-2V to 30V DC -2V to 34V Transient, 100ns
	DH	-2V to BST+0.3V
T_j	Junction Temperature	-40°C to 125°C
ϕ_{ja}	Thermal Impedance (junction to ambient)	75.5°C/W

Electrical Characteristics

Unless otherwise noted: V_{CCA} = 5V, V_5 = 5V (refer to Figure 1)

$-40^{\circ}C < T_A < 85^{\circ}C$

Circuit = Typical Application Circuit

PARAMETER	NAME	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY, BIAS, UVLO, VID REGULATOR AND POWERGOOD						
Supply (V_{CCA}, V_5, GND)						
V_5 Supply Voltage Range	V_5		4.3	5.0	6.0	V
V_{CCA} Supply Voltage Range	V_{CCA}		4.3	5.0	6.0	V
V_{CCA} Quiescent Current	I_{CCQ}	EN is low			10	µA
		EN is high, and V_{CCA} in UVLO		400		
V_{CCA} Operating Current (Static)	I_{CC}			5		mA
UnderVoltage Lock Out Circuit						
Threshold (V_{CCA} falling)	V_{HV5}		3.9	4.1	4.3	V
V_{CCA} Hysteresis	V_{HYST_V5}		100	200	300	mV

Electrical Characteristics

PARAMETER	NAME	CONDITIONS		MIN	TYP	MAX	UNITS
Enable Input (EN)							
Input High	V_{EN_IH}			2			V
Input Low	V_{EN_IL}					0.8	V
Vcore Power Good Generator (PWRGD)							
Input Threshold	V_{TH_CORE}	V_{DAC}=0.925V - 2.000V. Note that during UVLO, the output level of this signal is undefined.	Upper threshold	2.30	2.35	2.40	V
			Lower threshold		0.85	0.875	
			Hysteresis	1	2	3	%
Output Voltage Note: During the latency time of any VID code change, the PWRGD output signal is not valid.	V_{PWRGD}	Pull-up with External 680 Ω to 1.4V.	$V_{CORE} = V_{DAC}$		0.95*V_{CORE}		V
			V_{CORE} < 0.8V			0.4	
			EN is high but UVLO condition			0.8	
CORE CONVERTER CONTROLLER							
Core Converter Softstart (SS)							
V_{ss} Softstart Termination Threshold	V_{SS_TERM}			1.9	2	2.1	V
Core Converter Softstart Current Note: Softstart cap is not discharged until Enable goes low or UVLO cuts in. To enable bias and soft-start, Vss has to drop below V_{SS_EN}.	I_{SS}	Core Charge (Souce) Current, V_{SS} = 0V		5	8	11	µA
		Discharge (Sink) Current, V_{SS_CORE} = 1.7V		0.30	2		mA
V_{SS} Enable Threshold	V_{SS_EN}				150	400	mV
DAC VID [0..4]							
VID Input Threshold	V_{VID_IH}			2			V
	V_{VID_IL}					0.8	
DAC Output Voltage Accuracy	V_{DAC_ERR}	0 < T_A <85°C I_{DAC}=0		-1		+1	%
		-40 < T_A <85°C I_{DAC}=0		-1.25		+1.25	%

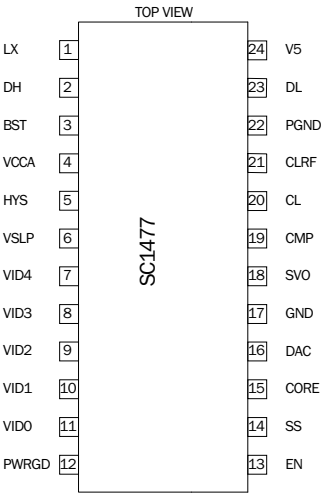
Electrical Characteristics

PARAMETER	NAME	CONDITIONS		MIN	TYP	MAX	UNITS
Settling Time (guaranteed by Design)	$T_{SET\_VID\_DAC}$	C_{DAC}=1000pF, R_{DAC}=100KΩ VID is set to change V_{CORE} from 1.30V to 1.40V or 1.40V to 1.30V. Measured from VID[0..4] code transient to V_{DAC} settling within + 1% of its steady state value				35	µS
Soft VID Override							
Input Offset Voltage	$\lvert V_{VSLP}-V_{DAC}\rvert$	V_{VSLP} = 1.4V			0	± 3	%
CORE Comparator (CMP, CMPRF, HYS)							
Input Bias Current	I_{CMP}	V_{CMP} = 1.4V				± 2	µA
Input Offset Voltage	$\lvert V_{CMP}-V_{DAC}\rvert$	V_{DAC} = 1.4V			± 1.5	± 3	mV
Hysteresis Settling Current	I_{CMP}	R_{HYS} = open				± 1.5	µA
		R_{HYS} = 17 kΩ		+ 85	+ 100	+ 115	
		R_{HYS} = 170 kΩ		+ 7	+ 10	+ 13	
Propagation Delay Time (guaranteed by Characterization)	$T_{PD\ CMP\_DL}$	V_{DAC} = 1.4V ΔV_{CMP} = 40mV input step with 20mV overdrive. Measured at device pins, from the trip point to 10% of DL transition	T_A= 25°C			40	ns
			T_A= Full Range			50	
Current Limit Comparator (CL, CLRF, CLSET)							
Input Bias Current	$\lvert I_{CL}\rvert$	V_{CL}=1.3V				± 5	µA
Current Limit Setting Current	$\lvert I_{CLREF}\rvert$	R_{HYS} = 17 kΩ	$V_{CLREF}-V_{CL}$ = 10mV		300		µA
			$V_{CLREF}-V_{CL}$ = - 10mV		200		µA
		R_{HYS} = 170 kΩ	$V_{CLREF}-V_{CL}$ = 10mV		30		µA
			$V_{CLREF}-V_{CL}$ = - 10mV		20		µA

Electrical Characteristics

PARAMETER	NAME	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$\lvert V_{CLREF-} V_{CL} \rvert$	$V_{CLREF = 1.3V}$		$\lvert \pm 4 \rvert$	$\lvert \pm 6 \rvert$	mV
POWERSAVE						
Offset Voltage			-2	3	8	mV
DRIVERS						
High-Side Driver (DH)						
Peak Output Current	I_{PKH}	Cl=3nF, V_{BST}=V_{DRN}=4.6V		2		A
Output Resistance	R_{SRC}			1		Ω
	R_{SINK}			0.7		
Rise Time	t_{r_TG}			14	23	ns
Fall Time	t_{f_TG}			12	19	
Propagation Delay Time , TG going high				20	32	ns
Propagation Delay Time , TG going low				15	24	
Low-Side Driver (DL)						
Peak Output Current	I_{PKH}	Cl=3nF, V_{V5}=4.6V		4		A
Output Resistance	R_{SRC}			1		Ω
	R_{SINK}			0.5		
Rise Time	t_{r_BG}			15		ns
Fall Time	t_{f_BG}			13		
Propagation Delay Time , TG going high				12		
Propagation Delay Time , TG going low				7		

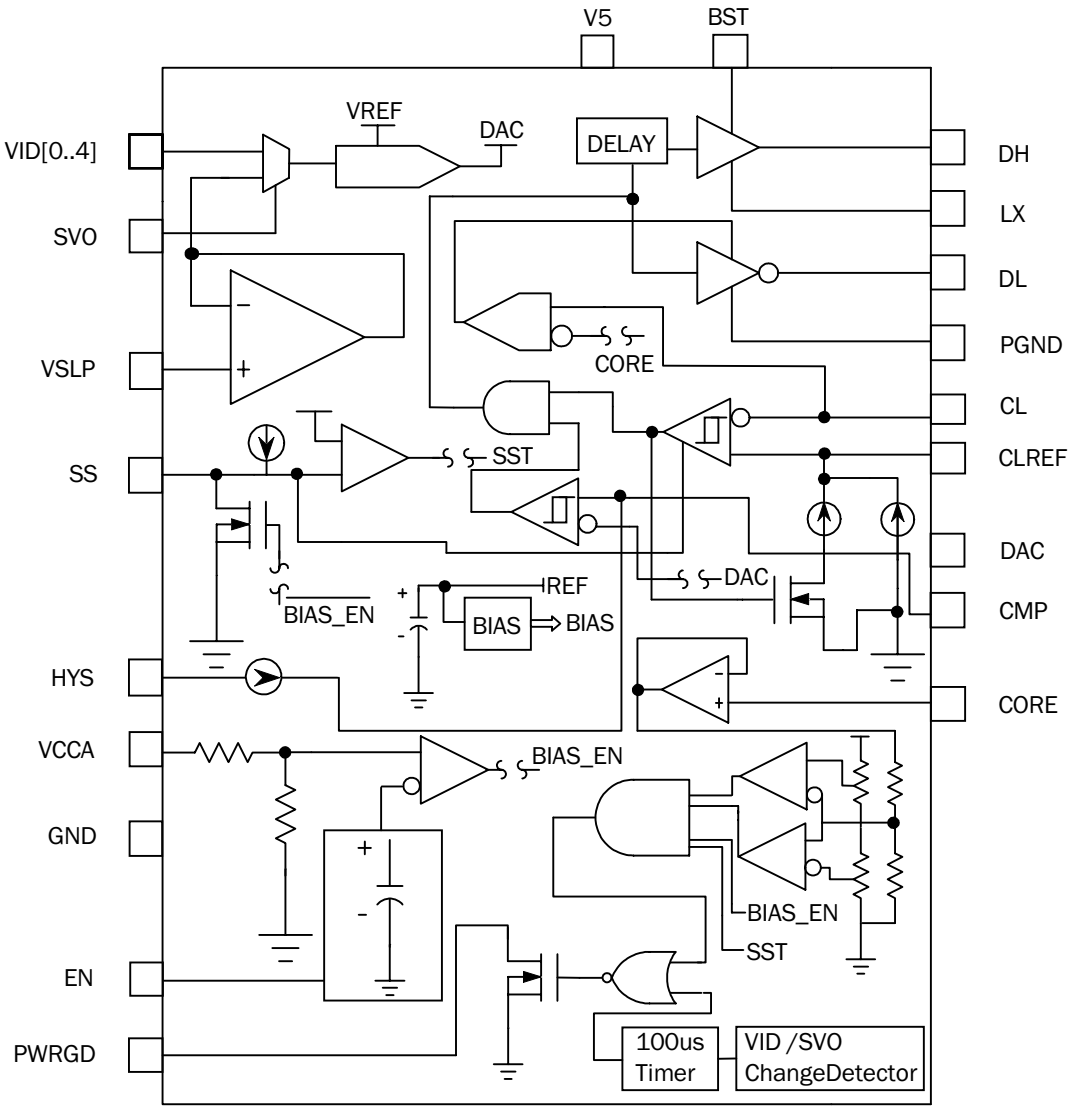
Pin Configuration



Ordering Information

DEVICE	PACKAGE	TEMP. (T_a)
SC1477ITSTR	TSSOP-24	-40 - +85°C

Block Diagram



Pin Description

Pin #	Pin Name	Pin Function
1	LX	This pin connects to the junction of the switching and synchronous MOSFETs.
2	DH	Output gate drive for the switching (high-side) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and LX pins to develop the floating bootstrap voltage for the high-side MOSFET.
4	VCCA	5V supply for precision analog circuitry.
5	HYS	Core Comparator Hysteresis. Connects to ground via an external resistor, called RHYS. Hysteresis current is established by an internal VREF voltage, 1.7V, divided by RHYS.
6	VSLP	The voltage on this pin sets the DAC output during Soft Vid Override mode.
7	VID4	VID most significant bit main controller voltage programming DAC input.
8	VID3	VID input
9	VID2	VID input
10	VID1	VID input
11	VID0	VID least significant bit main controller voltage programming DAC input.
12	PWRGD	Power Good - open drain output. When the Main Converter Output approaches and stays >0.9V and <2.3V and the soft-start period has terminated, this signal is pulled high by an external resistor.
13	EN	Enable - active high. This is capable of accepting a 5.0V signal level.
14	SS	Main controller CORE output Soft Start. An external cap defines the soft start ramp.
15	CORE	Main CORE Converter Output Feedback to the power-good generator. A small RC filter should be used to filter out any HF component to prevent faulty trip condition.
16	DAC	Main controller Digital-to-Analog Output.
17	GND	Ground.
18	SVO	Soft Vid Override signal. In SVO mode, the DAC output is set by the VSLP pin.
19	CMP	Core Comparator input pin.
20	CL	Current Limit Input Pin.
21	CLRF	Current Limit Reference Input Pin.
22	PGND	Power ground. Connect to the synchronous FET power ground.
23	DL	Output drive for the synchronous (low-side) FET.
24	V5	5V supply. A capacitor should be connected from V5 to PGND.

Functional Description

SUPPLY

The chip is optimized to operate from a 5.0 V ± 5% rail but also designed to work up to 6V maximum supply voltage.

Under Voltage Lock-Out Circuit

The Under-Voltage-Lock-Out Circuit consists of a comparator which monitors the V_{CCA} voltage level. The SC1477 is in UVLO mode whilst the supply has not ramped above the upper threshold or has dropped below the lower threshold.

Power Good Generator

If the chip is enabled but not in UVLO condition, and the core voltage is greater than 0.875V and less than 2.3V then a high level Power Good signal is generated on the PWRGD pin to trigger the processor power up sequence. If the chip is either disabled or enabled but in UVLO condition, then PWRGD is undefined. This is an open-drain output and will be pulled-up externally by a 680Ω resistor.

During soft start, PWRGOOD stays low independently from the status of Vcore voltage. During VID code change latency time or a soft vid override transition, PWRGOOD is forced high (open drain).

Over-Voltage Protection

If the CORE voltage is greater than 2.35V the SC1477 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch.

Thermal Shutdown

The device will be disabled when the internal junction temperature reaches approximately 160°C and will not restart until the temperature has dropped by about 10°C.

Protection Mode

Protection Mode	When Active	latched?	Driver Status	SS status
Supply UVLO (VCCA)	always	no	all low	low
32 cycle current limit	SS has terminated and PWRGD is low (during blanking, is inactive)	yes	DH low	sawtooth ramp
2.35V Vcore OVP	always	yes	DL high	high
Thermal Shutdown	always	no	all low	high

Band Gap Reference

A ± 1% precision Band Gap Reference acts as the internal reference voltage standard of the chip, which all critical biasing voltages and currents are derived from. All references to V_{REF} in the equations to follow will assume V_{REF}=1.7V.

CORE CONVERTER CONTROLLER

Precision VID DAC Reference

This 5-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by CMOS logic level VID code applied to the DAC inputs. The VID code vs. the DAC output is shown in table 1. below. The accuracy of the VID DAC is maintained on the same level as of the Band Gap Reference.

VID control

Startup

On start-up, the VID inputs are ignored, and the output voltage is set according to the voltage level at the VSLP pin. Start-up is signaled via assertion of the SVO signal.

Normal Operation

During normal operation, the VID Management block detects a VID change by continuously comparing the current VID code to the last value stored, and changing the DAC output accordingly. If the SVO signal is asserted during normal operation, the VID inputs are ignored, and the output voltage is set according to the voltage level on the VSLP pin.

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of about 20ns at a 20mV overdrive. Its hysteresis is determined by the ratio of the high accuracy internal reference voltage, V_{REF}, divided by R_{HYS}.

Current Limit Comparator

The Current Limit Comparator monitors the core converter output current in each phase and turns the high side switch off when the current exceeds the upper current limit threshold, V_{HCL} and re-enabled only if the load current drops below the lower current limit with the core converter inductor threshold, V_{LCL}.

The current is sensed by monitoring the voltage drop across the current sense resistor, R_{CS} connected in series

Current limit Latch

If the CORE voltage goes lower than 0.85V (i.e. out of the powergood window), then sustained current limiting (32 current limit pulses) will cause the part to permanently latch off. The latch is inhibited during soft-start.

Core Converter Soft Start Timer

The primary purpose of this block is to reduce the initial inrush current on the core input voltage (battery) rail. The circuitry consists of an internal current source, external soft-start timing capacitor, an internal switch across the capacitor, and a comparator monitoring the capacitor voltage.

Functional Description

VID TRANSITIONING

Powergood blanking

On any VID change or assertion of the SVO signal, the PowerGood signal is blanked for 32 switching cycles (approx. 100us) to prevent glitching on the PowerGood during the transition.

Soft Vid Override

When SVO is high, the DAC is set by the voltage on the VSLP pin. On a SVO transition, the PWRGD pin is forced high (blanked) for 32 switching cycles.

POWER-SAVE

A zero-crossing comparator detects when the current through the external sense resistor reverses. At this point, the bottom FET is latched off. The latch is reset when the controller decides to switch on the top FET. This prevents excessive switching at light loads and hence saves switching power losses. Power save is inhibited during VID or SVO transition.

DRIVERS

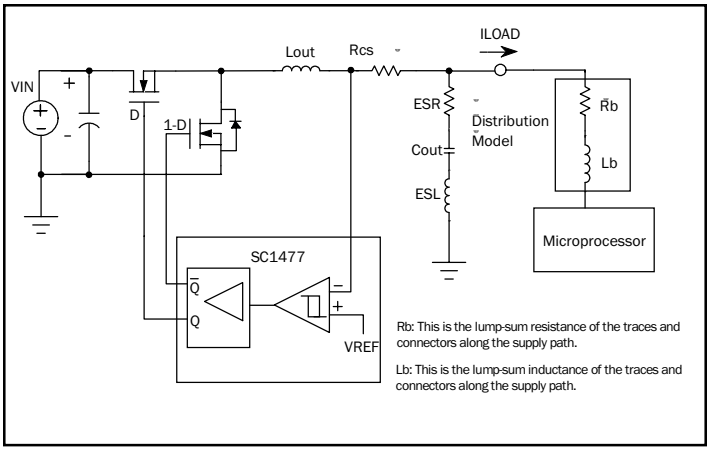
The DL output drives between the V5 supply and PGND to provide a 5V signal. In its pull-down state, the DL pin is capable of sinking 4A peak.

The DH output drives between the BST supply and LX to provide a 5V signal.

Applications Information

The basics of Hysteretic Controller

The major advantage of using a hysteretic controller is that it provides the fastest transient response among all power supply controllers and it is inherently stable due to the fact that there are no reactive elements in the control circuit to provide the phase shift required for the classical stability problems. Compared to all the other PWM controllers, hysteretic controller has no bandwidth-limited error amplifier, only a comparator which has hysteresis.



The comparator is to keep the output voltage and ripple within the hysteresis window. However, the ripple is slightly higher in reality due to the delays from the comparator and the driver circuitry. Any transient which takes the voltage out of the hysteretic range forces the converter immediately into the proper response since there is no error voltage to slew, and no maximum or minimum duty cycle limits to slow the transient responses as in most other control schemes.

Design Procedure

Requirements:

The 1st step in designing any converter is in defining the requirements, which can come from many sources. For the SC1477, the minimum and maximum voltage comes from the battery and AC adapter characteristics. The processor determines other requirements; they are

(1) Min & Max Output Voltage
(2) Min & Max Output Current
(3) Maximum Transient Current
(4) Transient Voltage Requirement

The SC1477 directly supports the AMD PowerNow!™and Transmeta LongRun™Power. The numbers in the sample calculation are taken from Mobile AMD Duron™ Processor Model 7 Datasheet.

The critical processor requirements are listed in the table below. The system requirements are:

1. $V_{ADAPTERMAX}$ = 24V

2. $V_{BATTMIN}$ = 6V

	Performance
$V_{CCMAXDC}$	1.50V
$V_{CCNOMDC}$	1.40V
$V_{CCMINDC}$	1.35V
$V_{CCMAXAC}$	1.55V
$V_{CCMINAC}$	1.30V
I_{CCMAX}	17.14A
I_{CCMIN}	1.53A
dI_{CC}/dt	30A/µS

The DC and AC tolerance values above apply at the processor pins, and are inclusive of controller and external component DC accuracies, ripple, load and temperature variations.

DC (Static) Analysis

The worst case DC tolerance on DAC over process and temperature is ± 1.25%. Taking into consideration of the drooping effect caused by the current sense resistor R_{CS} and lump-sum resistance of the traces and connectors along the supply path R_B, We add a no-load offset to counter that effect. This also gives us increased headroom for load transient, allowing us to reduce the amount of output capacitance, therefore reducing BOM cost. The amount of offset is determined by the following equation:

$$Voffset := Icc\_max \cdot (Rcs + Rb)$$

$$Rcs := 2 \cdot 10^{-3} \cdot \Omega$$

$$Rb := 1 \cdot 10^{-3} \Omega$$

The no-load voltage is computed as follows:

$$Vcore\_nl := Vcore\_nom \cdot \left(\frac{Roh + Roffset}{Roffset} \right)$$

Where,

$$Roh := 750\Omega$$

$$Roffset := 80.6 \cdot 10^{3} \Omega$$

$$Vcore\_nl = 1.413\ V$$

At full load, the voltage is computed as follows:

$$Vcore\_fl := Vcore\_nom \cdot \left(\frac{Roh + Roffset}{Roffset} \right) - Icc\_max \cdot (Rcs + Rb)$$

$$Vcore\_fl = 1.362\ V$$

$$Rhys := 49.9 \cdot 10^{3} \Omega$$

$$Vhys := 2 \cdot Vref \cdot \frac{Roh}{Rhys}$$

$$Vripple := 1 \cdot Vhys$$

$$Vripple = 0.051\ V$$

This calculation shows the amount of ripple at the 'input' to the current sense resistor; the actual amount of ripple current at the converter output will be a function of the current sense resistor value, and the output cap ESR. To calculate the amount of required output capacitance and maximum ESR, we must analyze the transient requirement. We will then go back and recalculate the actual output ripple.

AC (Transient) Analysis

The AC limits for V_{CC} are asymmetrical around the 1.4V DC nominal level, allowing 150mV for a positive voltage excursion, and 100mV for a negative excursion. The no-load offset we established provides an additional headroom for the effects of load-step. Likewise, the droop provided by the sense resistor adds an additional (negative) offset at full load, which helps the case of a load release.

Next step is to identify the worst case transient condition. The transient is caused by the load-current transition when the inductor current reached the new steady-state current level. The inductor current slew rate is dependent on the voltage applied to the inductor. This voltage is equal to (Vin -Vout) during a load-current step-up, or to Vout during a load current step-down. For most application, usually (Vin-Vout) is greater than Vout which identifies the worst case situation being the load current step-down transition. The lower voltage Vout, lowers the inductor current slew rate. Therefore, the load-current step down must be optimized first; then after the output filter selection, the load current step-up transient must be verified to meet the requirement.

For a negative load-step the maximum amount of ESR is determined by:

$$Esr\_neg\_load := \frac{Vcore\_max\_ac - Vcore\_fl}{Icc\_max - Icc\_min}$$

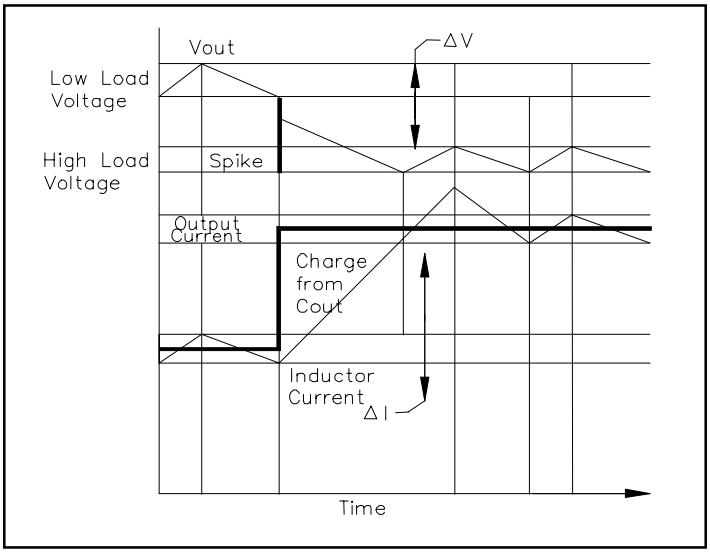
$$Esr\_neg\_load = 0.012\ \Omega$$

For a positive load step, the maximum ESR requirement is determined by the following equation:

$$Esr\_pos\_load := \frac{Vcore\_nl - Vcore\_min\_ac}{Icc\_max - Icc\_min}$$

$$Esr\_pos\_load = 7.002 \times 10^{-3} \Omega$$

Output capacitance and ESR values are a function of transient requirements and output inductor value. Fig. TBD illustrated the response of a hysteretic converter to a positive transient.



To find out the required output capacitance , we need to know the inductor value, which is a function of the highest desired switching frequency. The maximum frequency occurs at the highest input voltage; for the following we will calculate the inductance required for a 350kHz desired switching frequency.

$$dmin := \frac{Vcore\_nom}{Vin\_max}$$

$$Fs := 350\ 10^{3}\,Hz$$

$$Lmin := dmin \cdot \frac{(Vin\_max - Vcore\_nom) \cdot (Esr\_neg\_load + Rcs + Rb)}{Fs \cdot Vripple}$$

$$Lmin = 1.105 \times 10^{-6}\,H$$

This value of inductance is required up to maximum load. Inductors with a “swinging choke” characteristic, where the zero current value of inductance is much less than the full load current inductance can be used, as long as the above restriction is met. A value of 1.5uH is recommended to allow tolerances. Then, the worst-case (low input voltage) response time (the time for the current to reach the new transient value) is:

$$dT := L \cdot \frac{(Icc\_max - Icc\_min)}{Vin\_min - Vcore\_nom}$$

$$dT = 5.264 \times 10^{-6}\,s$$

Add ~100ns for the propagation delay from a change at the output to the MOSFET switch turning on in reaction. For negative load steps, the capacitance has to be large enough to absorb the energy in the inductance. Note that the worst case maximum current consists of the maximum DC current plus 1/2 of the ripple current. For the purpose of this calculation, we assume the initial (starting) voltage as the nominal value of $V_{CCNOMDC}$ at full load, and the final value to be the maximum AC (positive) transient value:

$$Cmin\_n := \frac{\left[\left(Icc\_max + \frac{dI}{2}\right)^{2} - Icc\_min^{2}\right]}{\left(Vcore\_max\_ac^{2} - Vcore\_fl^{2}\right)} \cdot Lmin$$

$$Cmin\_n = 6.8 \times 10^{-4}\,F$$

Using Sanyo POSCAPS, the 2R5TPC220M, specified as 150uF at 2.5V with 45mOhm maximum ESR, we see that 6 caps are needed to meet the minimum output capacitance requirements, however 7 caps are necessary to meet the ESR requirements, and . An alternative would be the Panasonic SP Caps, p/n EEFUE0D271R, specified at 270uF at 2V and 15mOhm ESR. 2 of these caps are sufficient to meet the ESR requirements, but 3 are required to meet the minimum capacitance requirements.
Next, calculation is done to verify that load-current step-up transient meet the requirements.

$$Cmin\_p := \frac{(Icc\_max - Icc\_min) \cdot \left(dT + 10^{-7}\,s\right)}{2 \cdot (Vcore\_nl - Vcore\_min\_ac)}$$

$$Cmin\_p = 3.83 \times 10^{-4}\,F$$

Therefore, the load current step-down design is sufficient for both step-down and step-up requirements.

Next is to verify the output ripple by using the following equation:

$$Vripple := \frac{(Vin\_max - Vcore\_nom) \cdot (Esr\_neg\_load + Rcs + Rb) \cdot dmin}{Fs \cdot L}$$

$$Vripple = 0.037\ V$$

Current Sense

As a compromise between current sensing accuracy, efficiency, and availability, a current sense resistor of 2mΩ is used. The power dissipation is I^2xR, or 1058mW, so choose a resistor greater than 1W for design margin.

The connection to CL, and CLREF (pins 20 and 21) is one differential pair connected to the current sense resistor. In order to cancel out common-mode noise, resistor pair R2-R4 should be equal. For the time being, assume R2 = R4 = 750Ω. These values may be adjusted later if required.

Current Limit

The current limit is a function of peak current and should be set at about 125% of the peak to allow overshoot of inductor current during transients. For L=1.5uH, and F=350kHz:

$$dI := \frac{(Vin\_max - Vcore\_nom) \cdot dmin}{Fs \cdot L}$$

$$Ipeak := Icc\_max + \frac{1}{2} \cdot dI$$

$$Ic\_lim := 1.25 \cdot Ipeak$$

$$Ic\_lim = 22.998\ A$$

The peak current limit (V_{HCL}) is defined by R_{HYS}, R_{CLOH} and R_{CS}. In essence, three times the hysteresis current appears on the CLRF pin. This current is forced through the R_{CLOH} resistor and sets the high V_{CLRF} reference voltage (with respect to V_{CORE}).

$$Vhcl := Ic\_lim \cdot Rcs$$

$$Iclrf := \frac{Vhcl}{Rcloh}$$

$$Rhys := 3 \cdot \frac{1.7V}{Iclrf}$$

$$Rcloh := 909\Omega$$

Therefore, in order to use 2mΩ current sense resistor and R_{HYS} = 100KΩ, R_{CLOH} is calculated to be 909Ω.
If the CL pin exceeds the V_{HCL} voltage (with respect to V_{CORE}), the DH driver is disabled. The CLRF current now switches to two times the hysteresis current and the DH driver is only re-enabled when the CL pin falls below the low trip point V_{LCL}:
Therefore, during a sustained short, the output current will ripple between I_hi_lim and I_low_lim.

$$I\_hi\_lim := 3 \cdot \frac{Vref}{Rhys} \cdot \frac{Rcloh}{Rcs}$$

$$I\_hi\_lim = 23\ A$$

$$I\_low\_lim := 2 \cdot \frac{Vref}{Rhys} \cdot \frac{Rcloh}{Rcs}$$

$$I\_low\_lim = 15.333\ A$$

On average, the output-short current is

$$Iout\_short\_circuit := \frac{1}{2} \cdot (I\_hi\_lim + I\_low\_lim)$$

$$Iout\_short\_circuit = 19.167\ A$$

MOSFETs selection and Gate Drive Design

The duty cycle (d) of the converter is a function of the input voltage. In most applications, where the converter runs directly from the battery, AC adapter, or even a regulated +5V source, d is always going to be much less than 50%. The low-side (or synchronous) FET, therefore, is conducting most of the time; further, because the diode clamps the voltage across the low-side FET, it switches with virtually zero voltage across it. The high-side (or control) FET(s) conduct for a relatively small amount of time, but have to switch the entire voltage. Therefore, the control FETs can have a relatively high $R_{DS(ON)}$, but need low capacitive losses, and the synchronous FET needs to have a low $R_{DS(ON)}$, and can have higher capacitance. To accomplish this, one can use a single FET type, with two or more in parallel, or one can use FET sets with individually optimized devices.

The current in the control FET is approximately:

$$I_{QRMS} := I_{CC\_MAX} \cdot \sqrt{d_{MAX}}$$

$$d_{MAX} := \frac{V_{CC\_NOM}}{V_{IN\_MIN}}$$

$$I_{QRMS} := 11.5A$$

Use this current also to size input capacitors, since generally voltage ripple on the battery is not a major concern. Size the synchronous FET(s) for the full output current. Since the drive is derived from 5V, use $R_{DS(ON)}$ and current rating for Vgs=4.5V to select FETs.

Gate resistors are required for the control FET and can be used for multiple synchronous FETs (one resistor per gate). The value is dependent on FET selection and layout. Generally, start with 2.2Ω to 4.7Ω to evaluate the circuit for EMI performance and Miller (gate to drain) capacitance effects. Increasing the high-side FET gate resistor value will lessen both problems, but at the expense of higher switching losses. Synchronous FETs usually work best with zero gate resistance.
Miller capacitance in the low-side FET can cause it to turn ON as the high-side FET turns on. It acts as a charge-pump capacitor to couple the current from the fast dV/dt on the drain into the gate.

If the voltage is sufficient to conduct significant current, then efficiency is poor, and in extreme cases, the devices can be damaged. For a given FET, Cgs is fixed, so one possible solution is to slow down dV/dt; another is to reduce Zdrive. Reducing Zdrive is primarily a function of layout and FET selection, since the internal

reduce the peak gate voltage. However, the best practice is to locate the SC1477 as near as possible to the low-side FET and run wide traces to the gate. Rg of the FET can be on the order of 10Ω. The built-in SC1477 driver is typically 1Ω; so, given the short (10-20ns) dt, Zdrive can be dominated by trace inductance. For long gate drive traces, this inductance can resonate with the gate capacitance; in this case, a few ohms of gate resistance can damp the circuit and actually Other potential solutions are to choose FETs with a low Cds/Cgs ratio, low Rg, or add a capacitor from the low-side gate drive to ground to externally lower the Cds/Cgs ratio.

Phase Node Design

The phase node is one of the most critical nodes in the converter design, and must be treated with care. When low-side FETs are off, the inductor current flows through the Schottky diode. Select the Schottky diode with a forward voltage at the peak inductor current less than the forward voltage of the parasitic diode of the FET, to keep it from conducting, and improving efficiency. The phase node, since it switches at very high rates of speed, is generally the largest source of common-mode noise in the converter circuit. For this reason, it should be kept to a minimum size consistent with its connectivity and current carrying requirements. Occasionally, a snubber network (R/C) is required to dampen parasitic ringing on the phase node caused by parasitic inductance and capacitance excited by the switching. One approach to snubber design is to record the frequency and amplitude of ringing before the snubber, then add pure capacitance until the frequency is reduced to half of the initial value then adding resistance until the required damping is achieved.

Powering the SC1477

There are two 5V supplies to SC1477. V_{CCA} is the 5V supply for the analog circuits within the chip and V5 is the 5V supply for driver circuit within the chip. The advantage of separating the supplies is so that the noise from the switchers would not interferer with the analog circuit behavior. Filter V_{CCA} with an RC network; R should be 10Ω, C, 0.1µF or greater.

Soft-Start Design

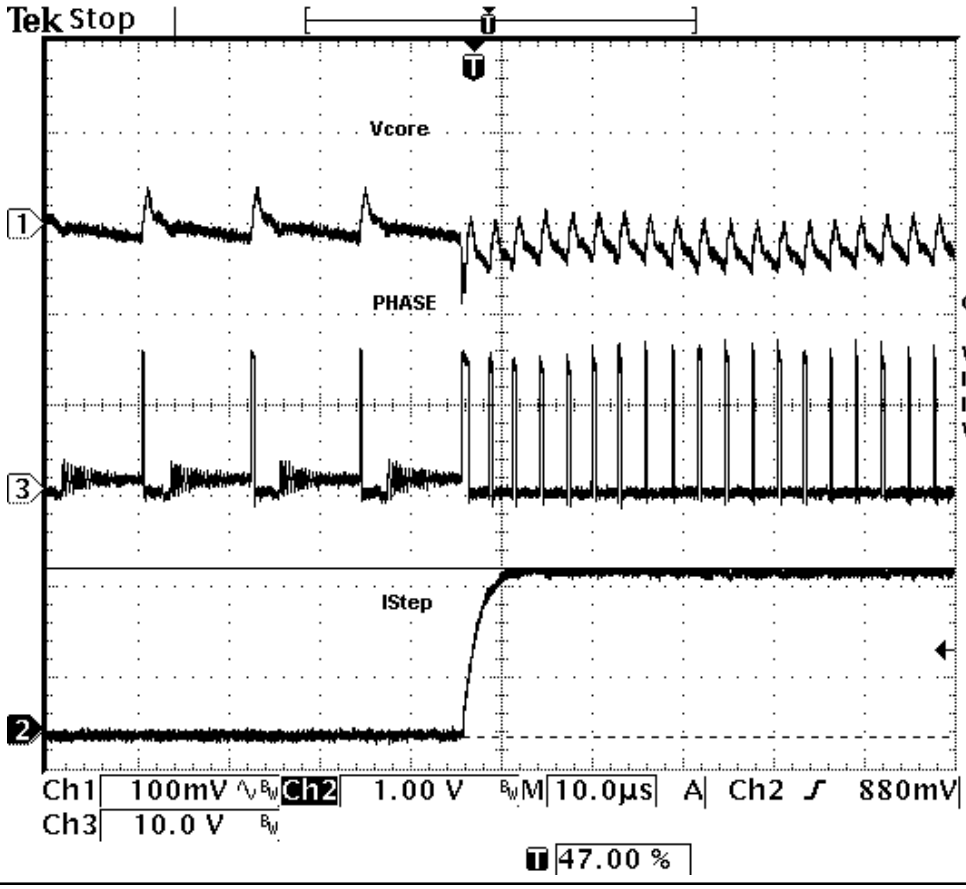
The V_{CE} output has user programmable soft-start. The soft-start timing is controlled with a capacitor charged by a nominal 5µA current source. The soft-start period is the time to charge the capacitor to V_{SS_TERM} (though the voltage eventually terminates near V_{CC}). The soft-start capacitor value is calculated for a 3ms nominal time by:

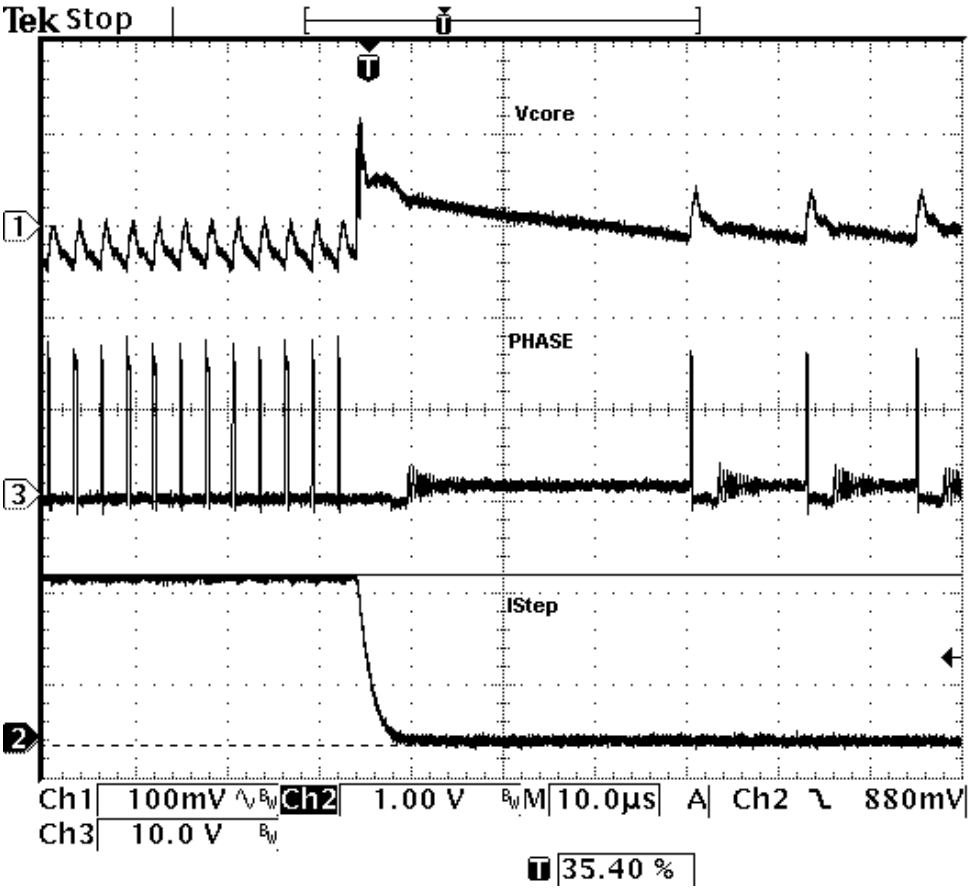
$$Css := \frac{Icss \cdot tss}{Vss\_term}$$

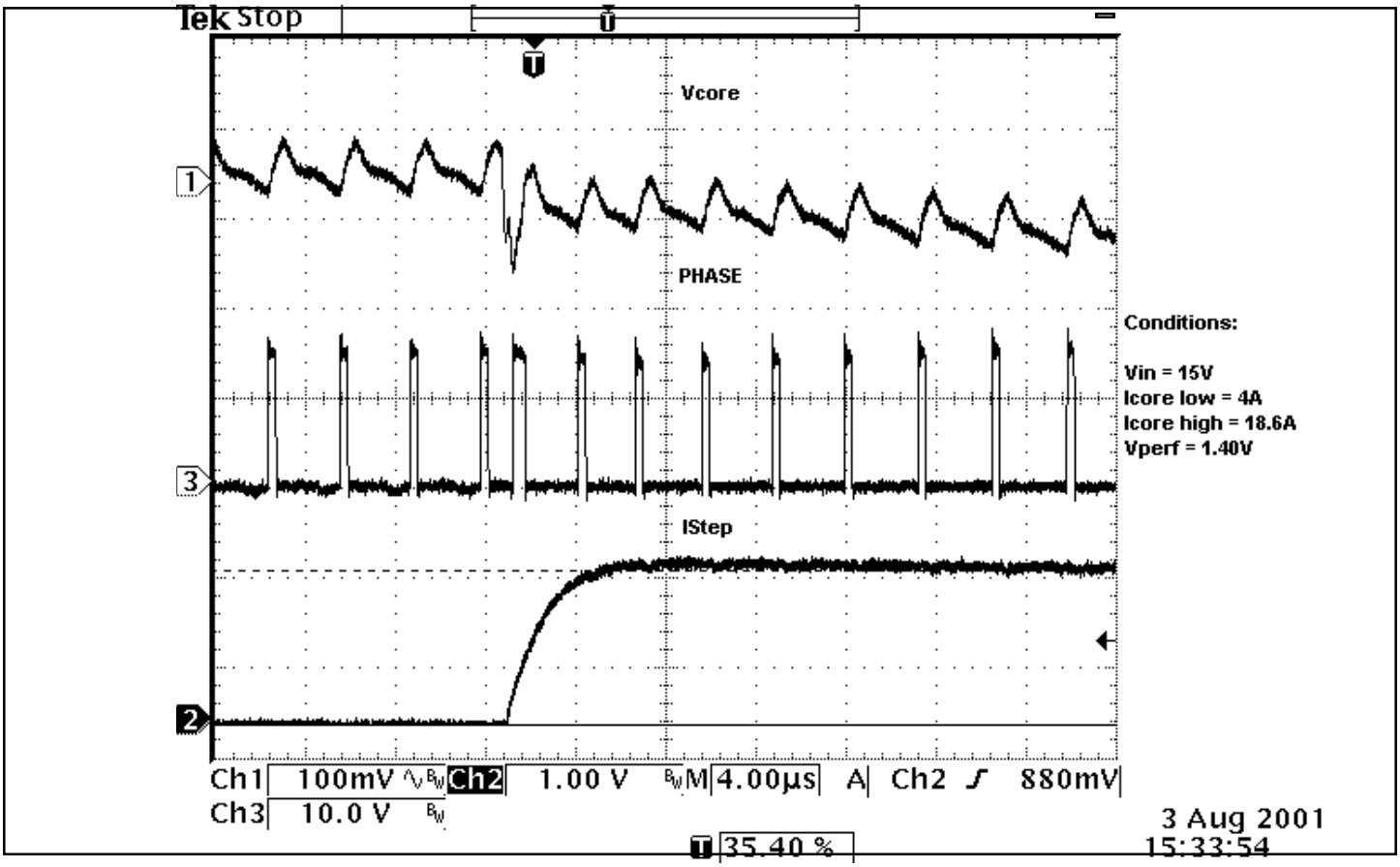
$$Css := 8.2nF$$

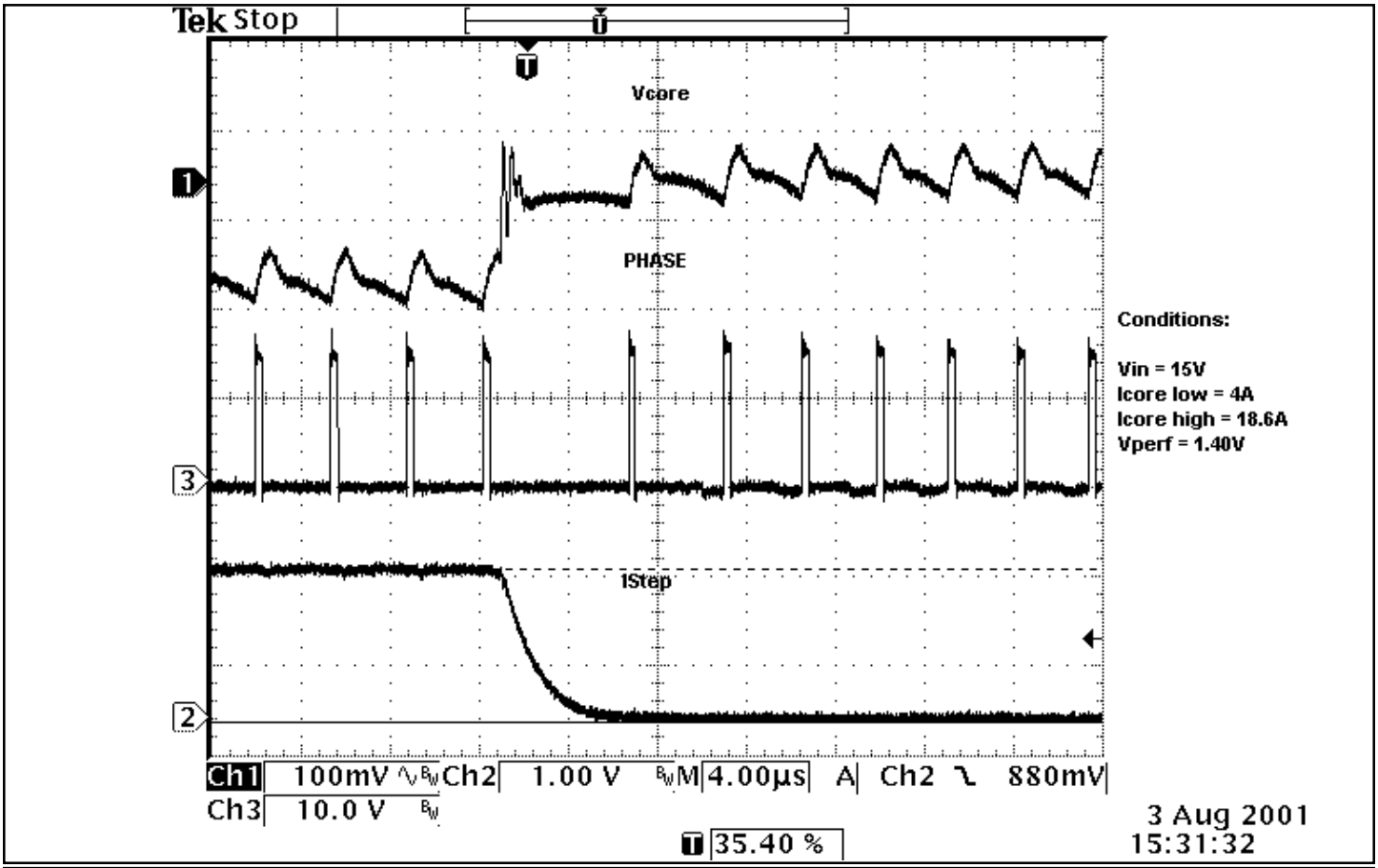
Table I. VID vs VDAC voltage

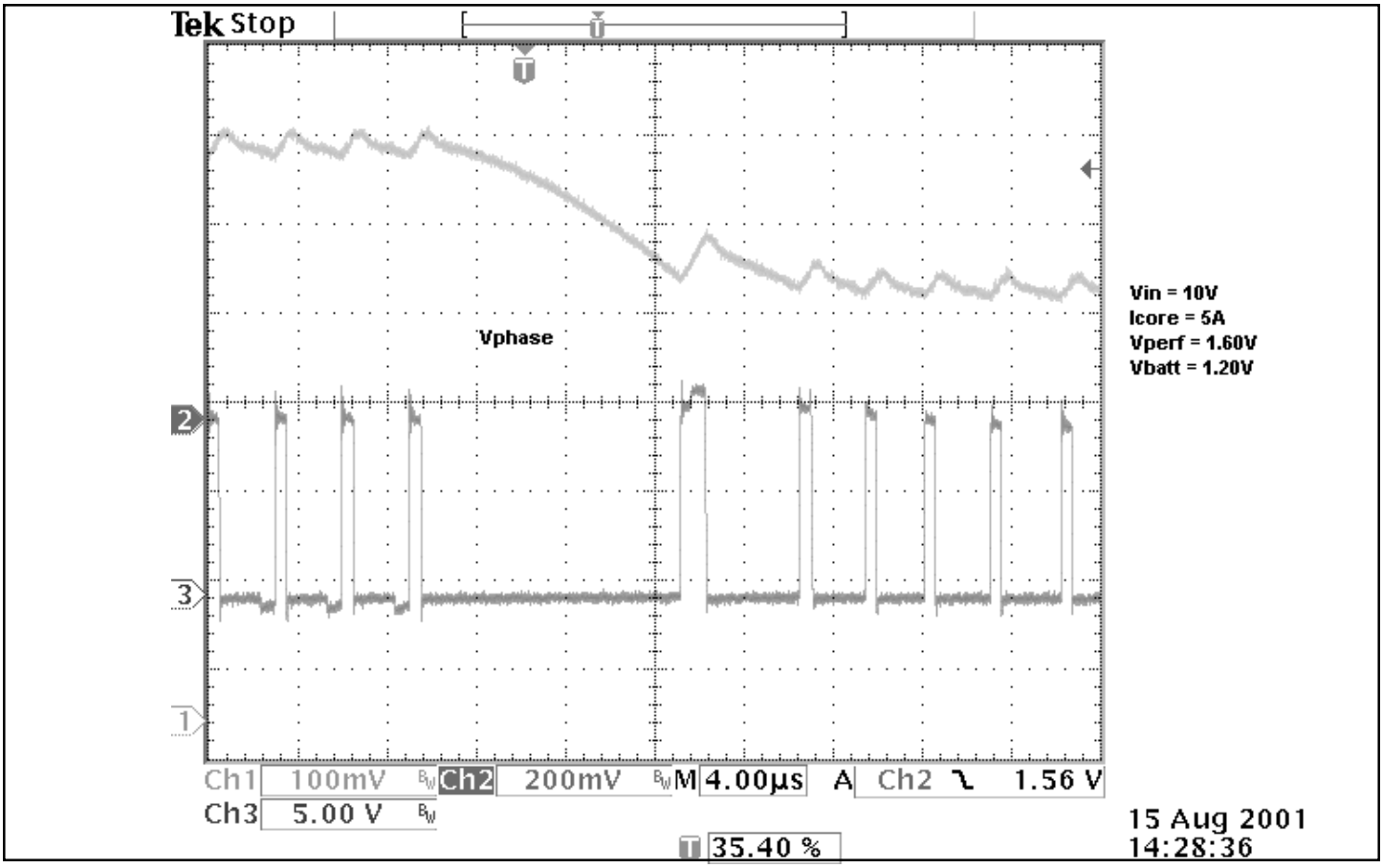
VID4	VID3	VID2	VID1	VID0	V_{DAC} (volts)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	SHUTDOWN
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	SHUTDOWN

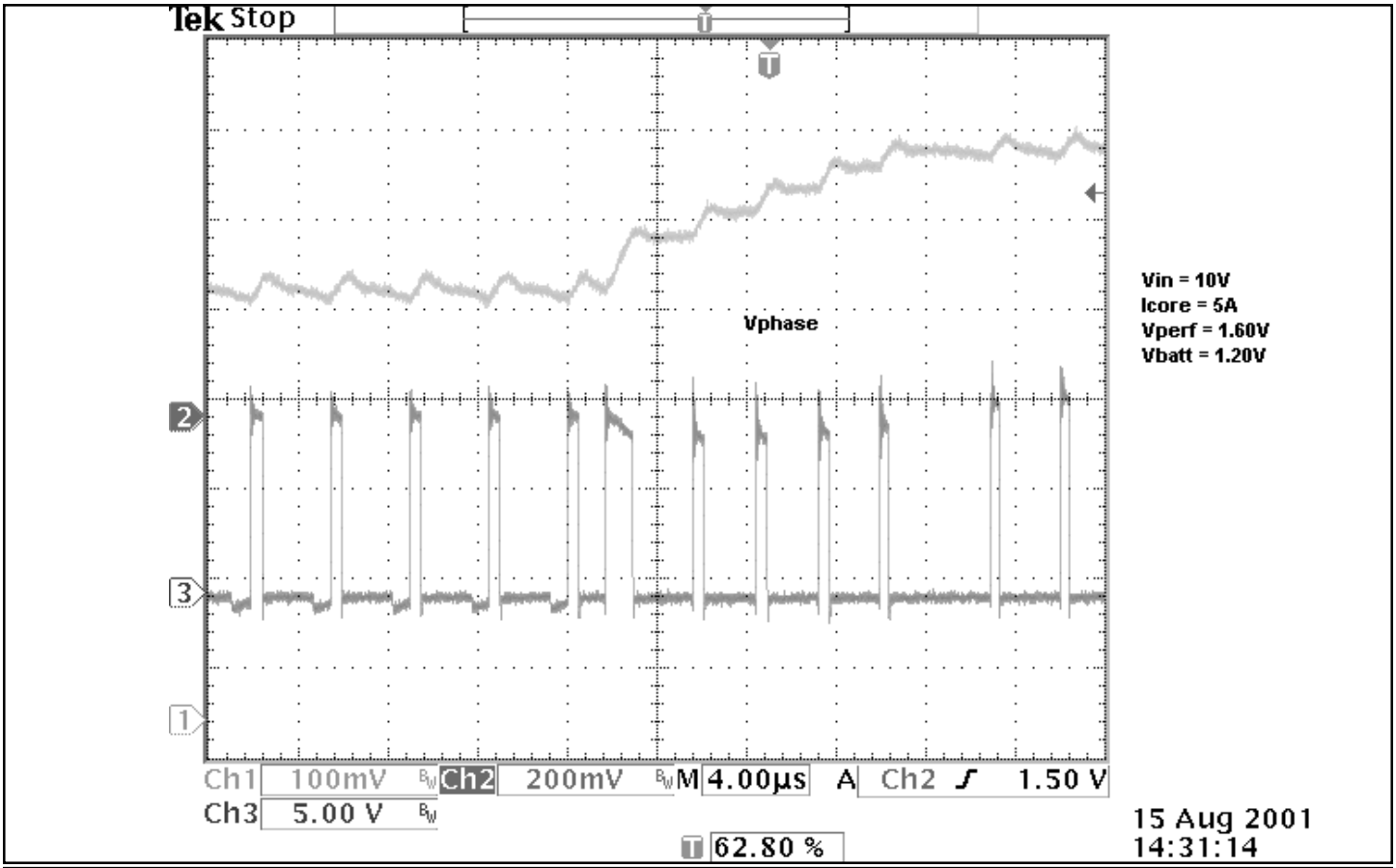

Tek Stop
Vcore
PHASE
IStep
Conditions:
Vin = 15V
Icore low = 1A
Icore high = 18.6A
Vperf = 1.40V
Ch1 100mV Ch2 1.00 V M 10.0µs A Ch2 880mV
Ch3 10.0 V
47.00 %
3 Aug 2001
15:25:36

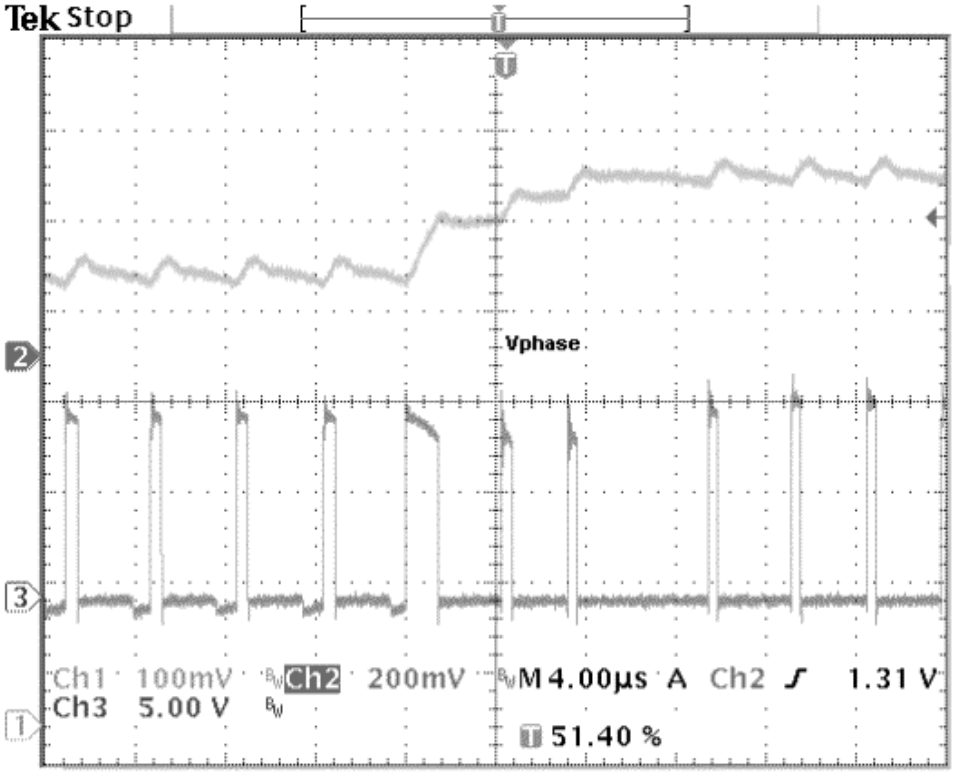

Tek Stop
Vcore
PHASE
IStep
Conditions:
Vin = 15V
Icore low = 1A
Icore high = 18.6A
Vperf = 1.40 V
Ch1 100mV Ch2 1.00 V M 10.0µs A Ch2 880mV
Ch3 10.0 V
35.40 %
3 Aug 2001
15:28:54

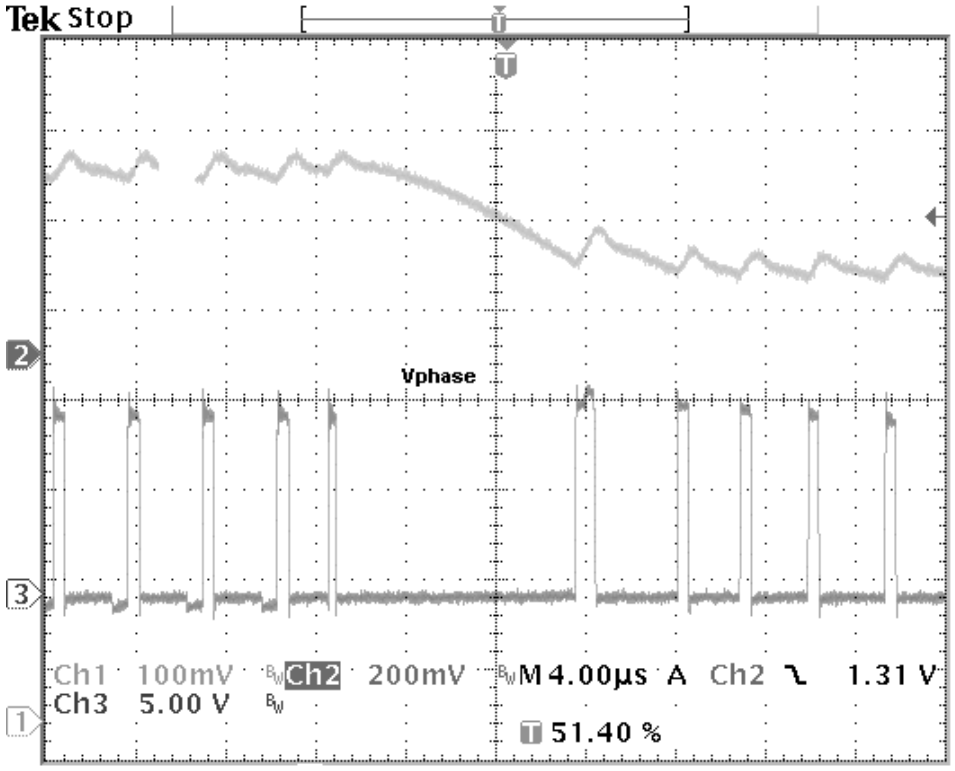

Tek Stop
Vcore
PHASE
IStep
Conditions:
Vin = 15V
Icore low = 4A
Icore high = 18.6A
Vperf = 1.40V
Ch1 100mV Ch2 1.00 V M 4.00µs A Ch2 880mV
Ch3 10.0 V
35.40 %
3 Aug 2001
15:33:54

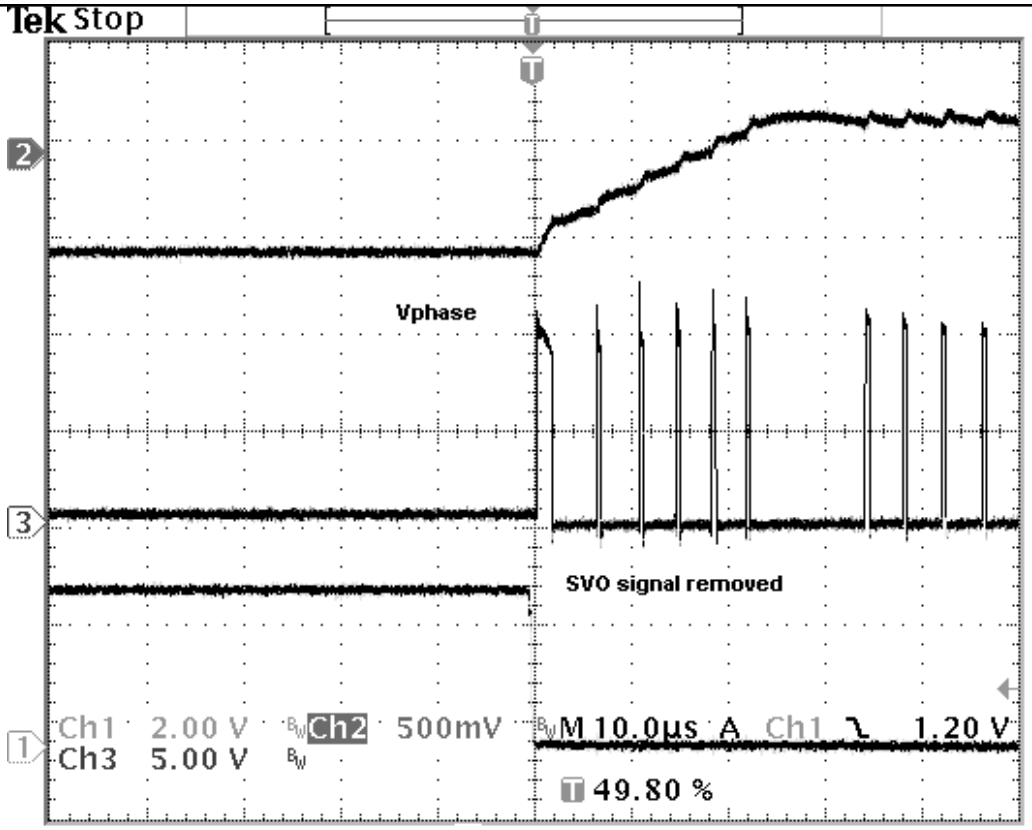

Tek Stop
Vcore
PHASE
IStep
Conditions:
Vin = 15V
Icore low = 4A
Icore high = 18.6A
Vperf = 1.40V
Ch1 100mV Ch2 1.00 V M 4.00µs A Ch2 880mV
Ch3 10.0 V
35.40 %
3 Aug 2001
15:31:32

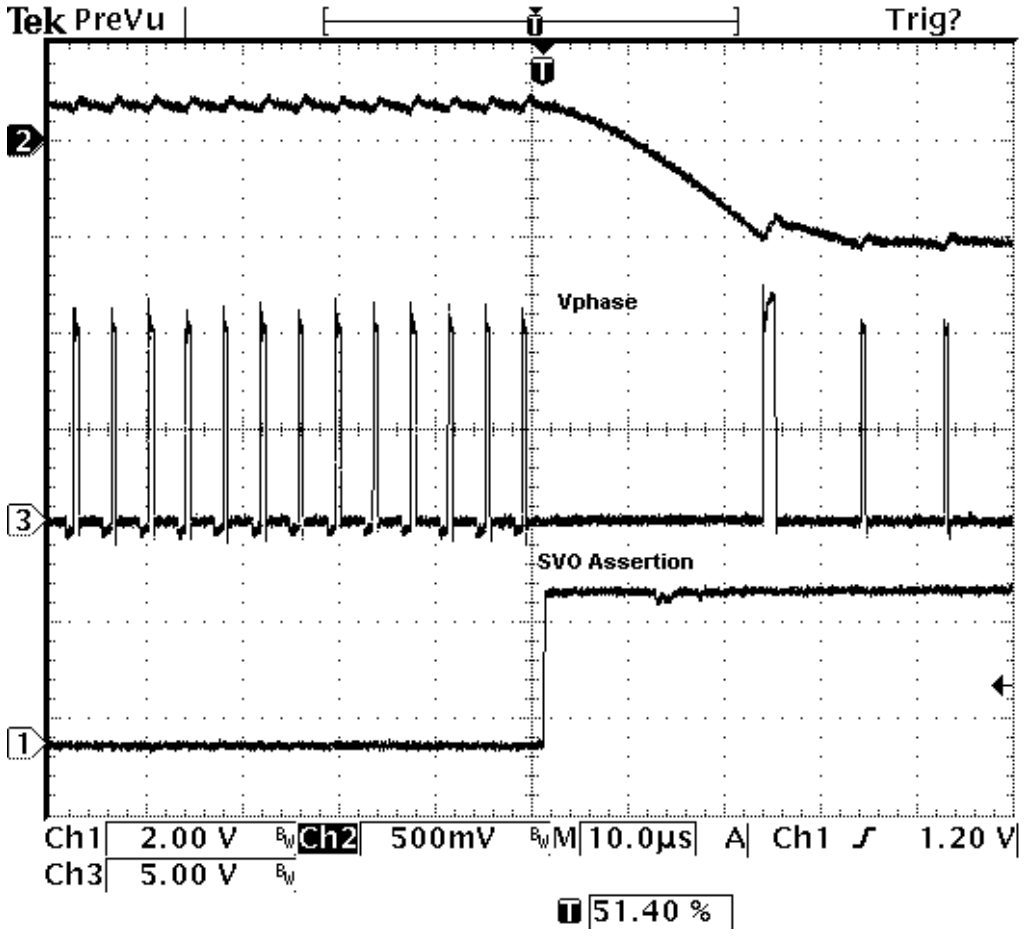

Tek Stop
Vphase
Vin = 10V
Icore = 5A
Vperf = 1.60V
Vbatt = 1.20V
Ch1 100mV Ch2 200mV M 4.00µs A Ch2 1.56 V
Ch3 5.00 V
T 35.40 %
15 Aug 2001
14:28:36


Tek Stop
Vphase
Vin = 10V
Icore = 5A
Vperf = 1.60V
Vbatt = 1.20V
Ch1 100mV Ch2 200mV M 4.00µs A Ch2 1.50 V
Ch3 5.00 V
T 62.80 %
15 Aug 2001
14:31:14


Tek Stop
Vphase
Vin = 10V
Icore = 5A
Vperf = 1.40V
Vbatt = 1.15V
Ch1 100mV Ch2 200mV M4.00µs A Ch2 1.31 V
Ch3 5.00 V
51.40 %

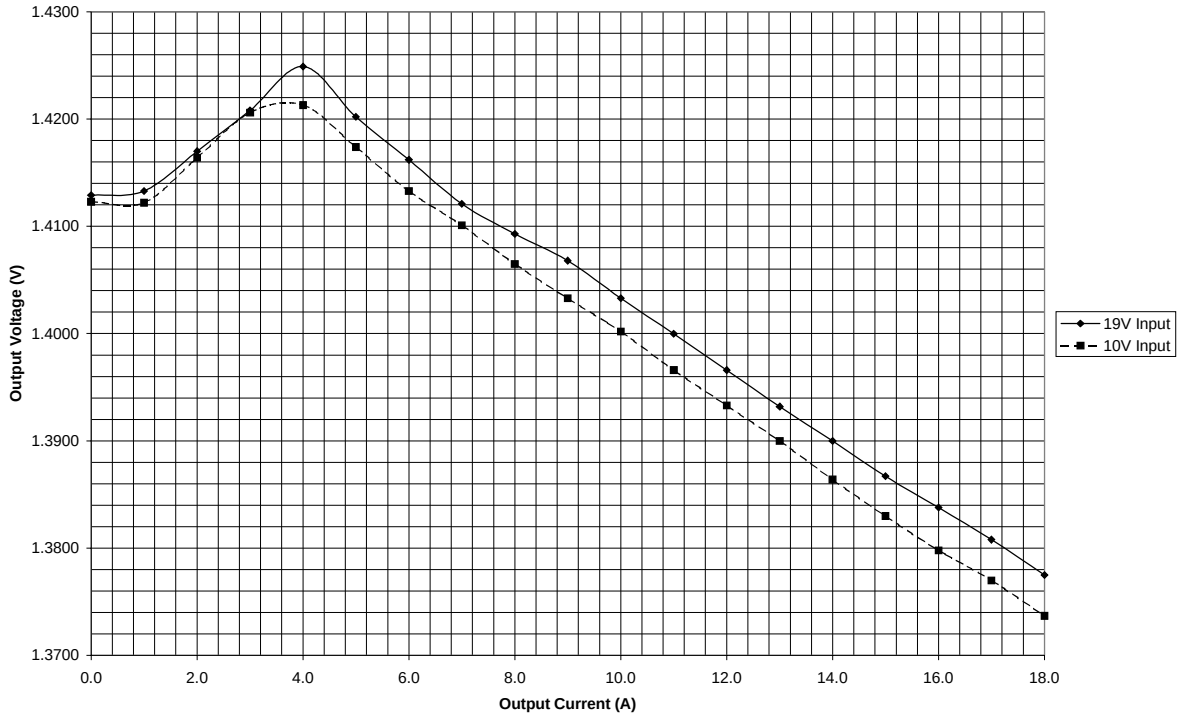

Tek Stop
Vphase
Vin = 10V
Icore = 5A
Vperf = 1.40V
Vbatt = 1.15V
Ch1 100mV Ch2 200mV M4.00µs A Ch2 1.31 V
Ch3 5.00 V
51.40 %


Tek Stop
Vphase
SVO signal removed
Vin = 10V
Vcore = 1.15V
Vsvo = 0.45V
Ch1 2.00 V Ch2 500mV M 10.0µs A Ch1 1.20 V
Ch3 5.00 V
49.80 %

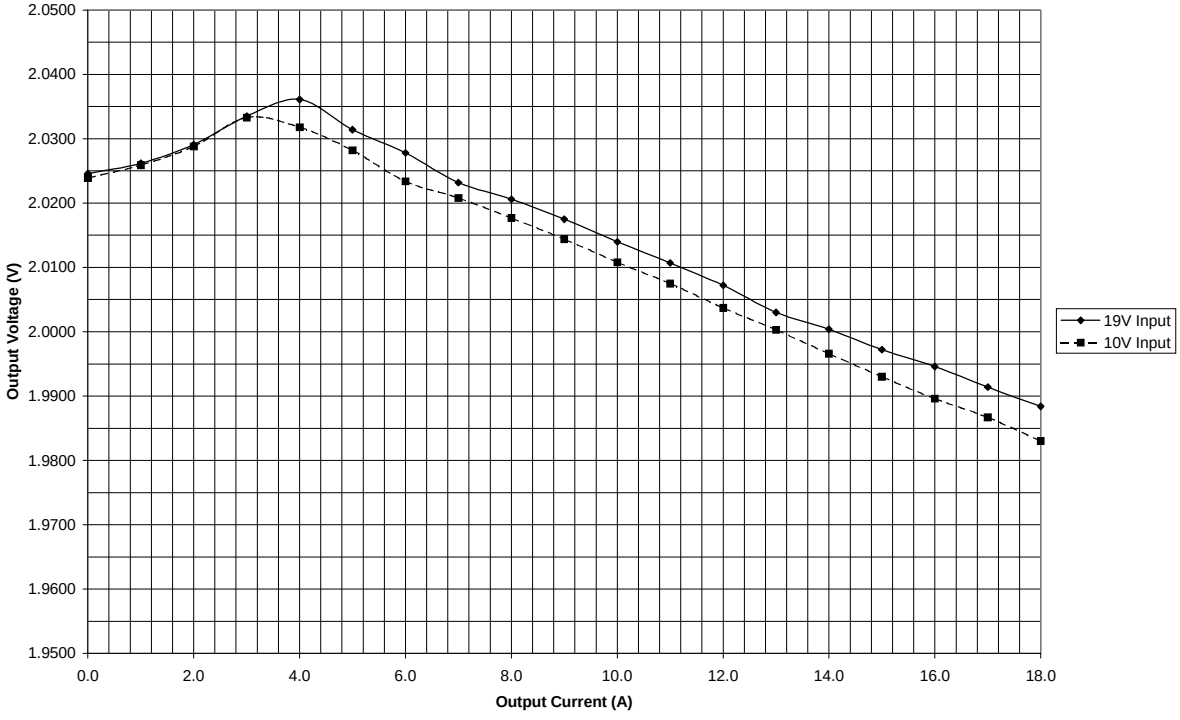

Tek PreVu
Trig?
Vphase
SVO Assertion
Vin = 10V
Vcore = 1.15V
Vsvo = 0.45V
Ch1 2.00 V Ch2 500mV M 10.0µs A Ch1 1.20 V
Ch3 5.00 V
51.40 %
15 Aug 2001
14:47:29

Typical Characteristics

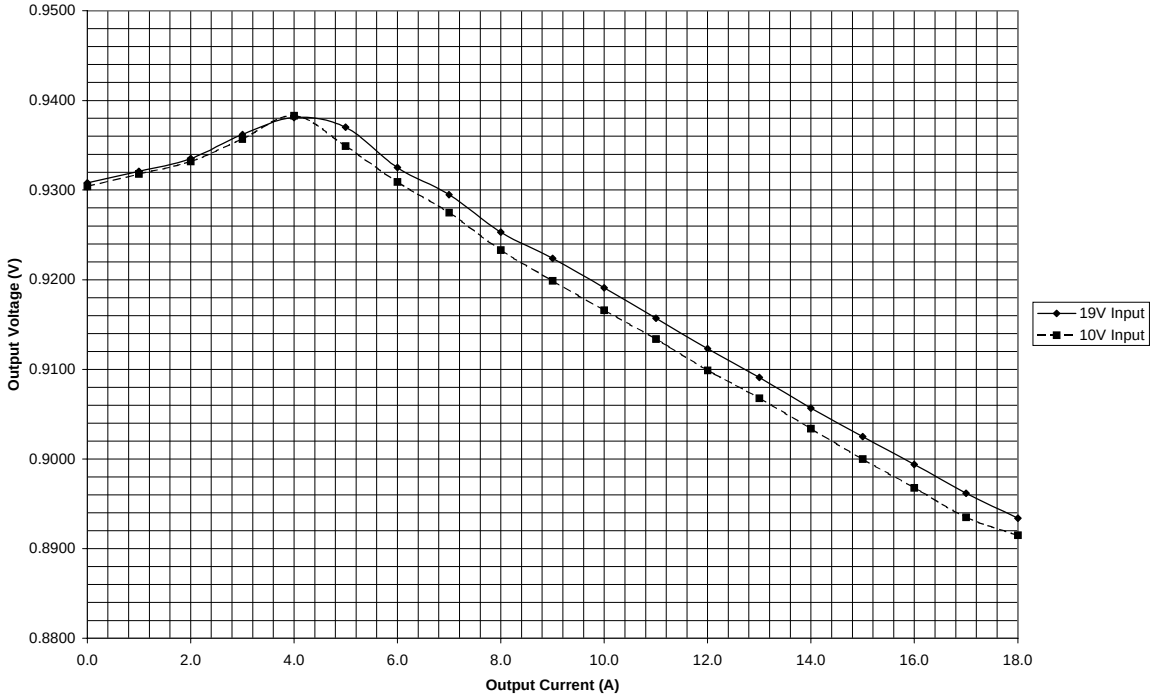
Line and Load Regulation
Vout = 1.4V



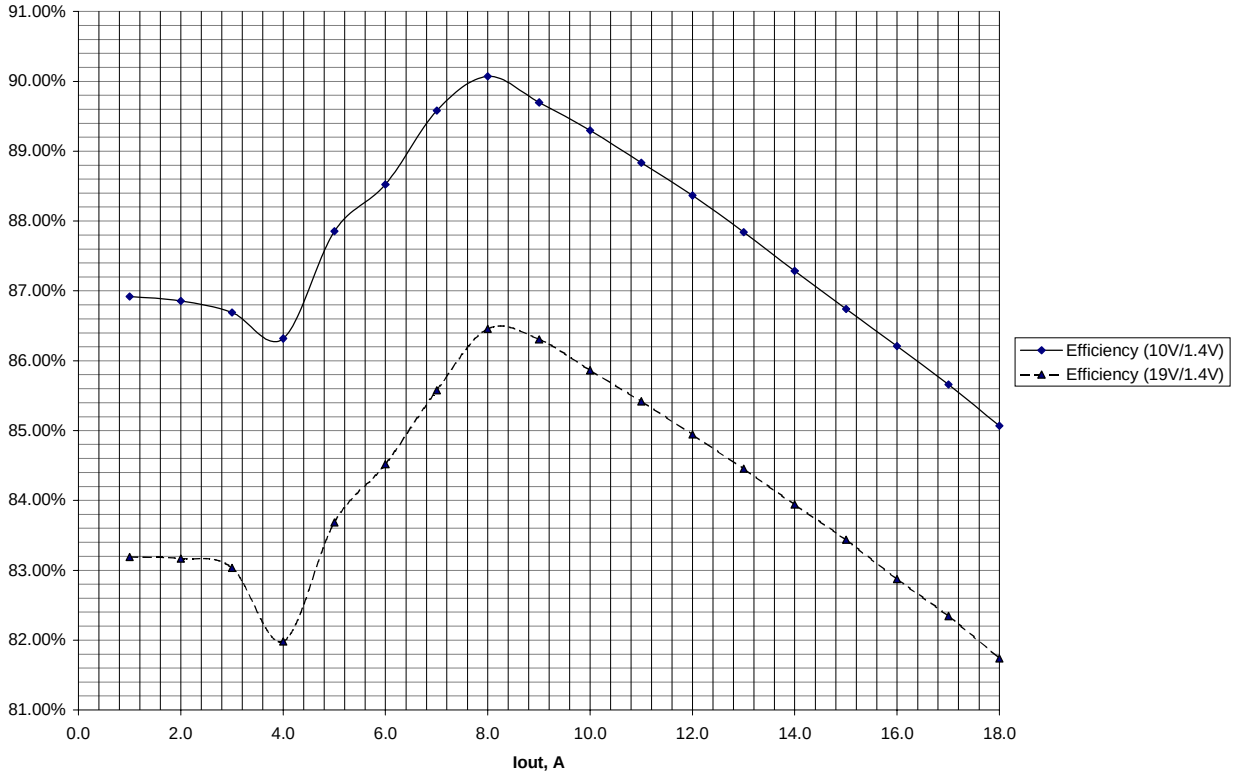
Line and Load Regulation
Vout = 2.0V



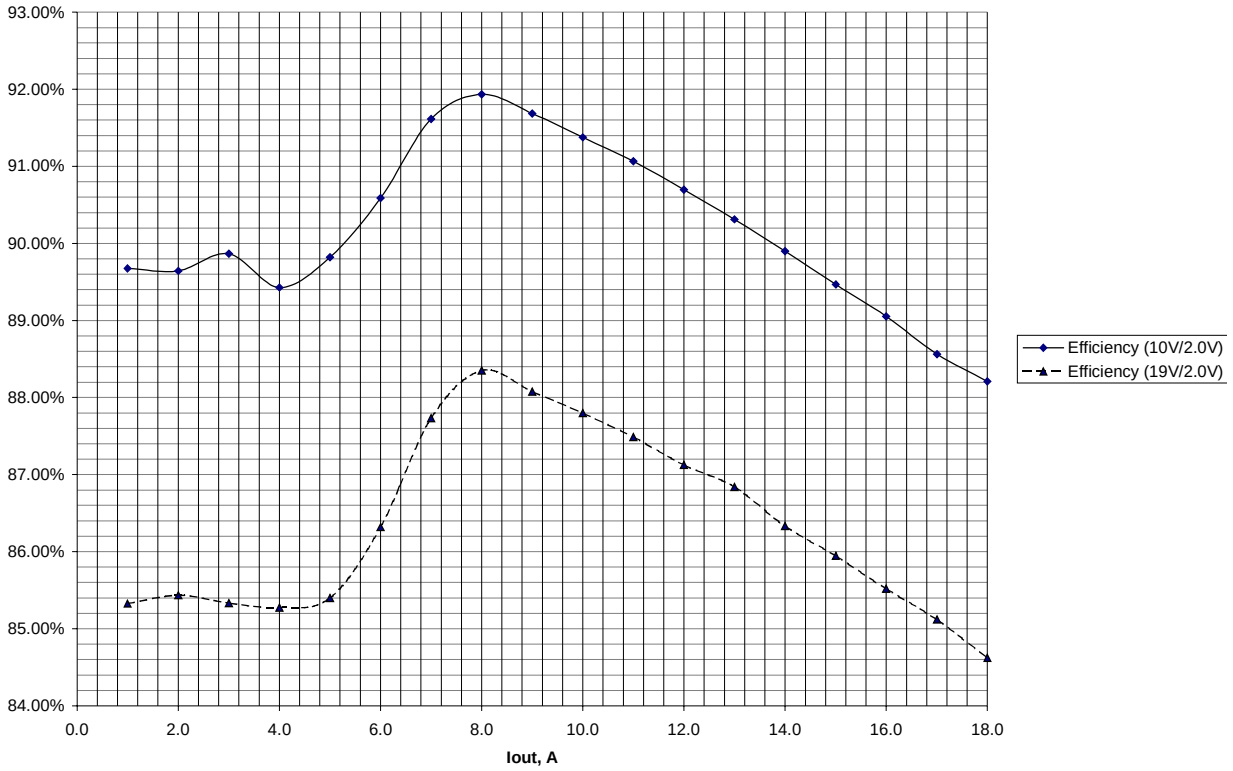
Line and Load Regulation
Vout = 0.925V



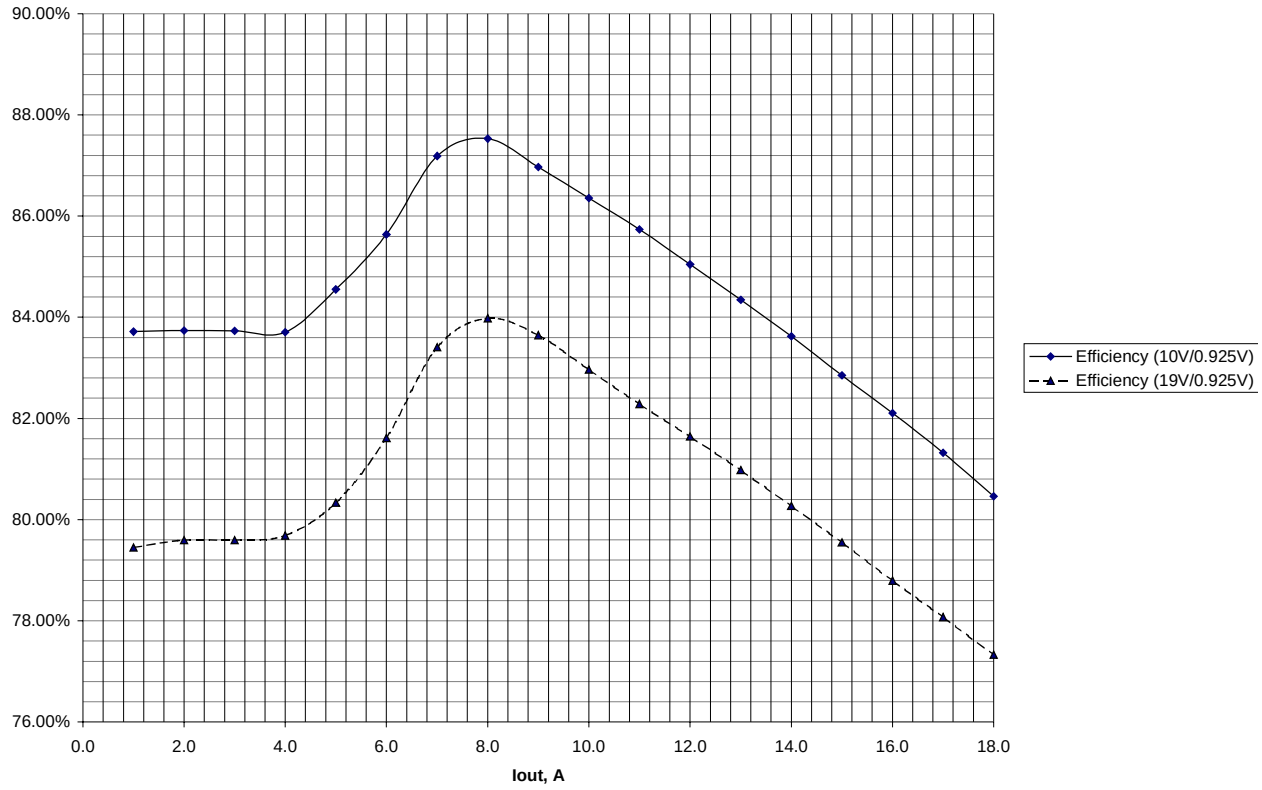
1.4V Output Power Efficiency (Vin = 10V and 19V)
2xFDS6694 + 3xFDS6674A



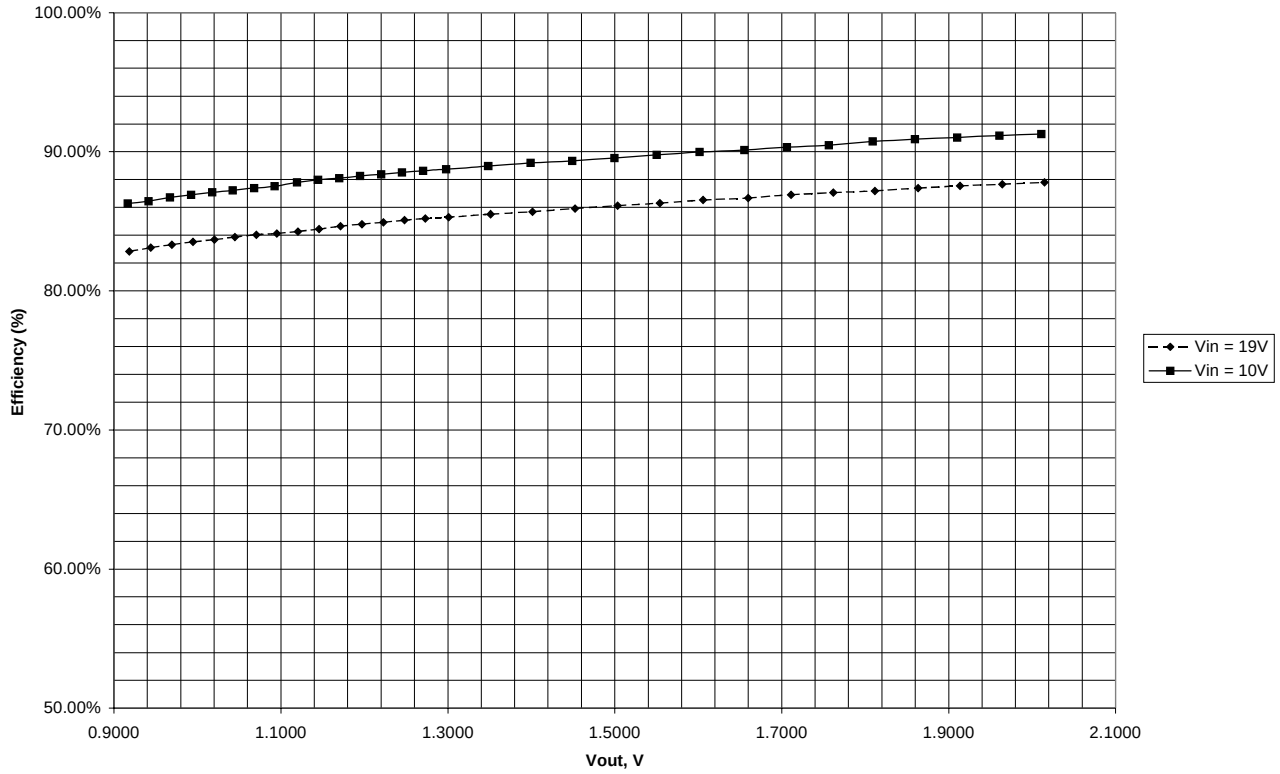
2.0V Output Power Efficiency (Vin = 10V and 19V)
2xFDS6694 + 3xFDS6674A



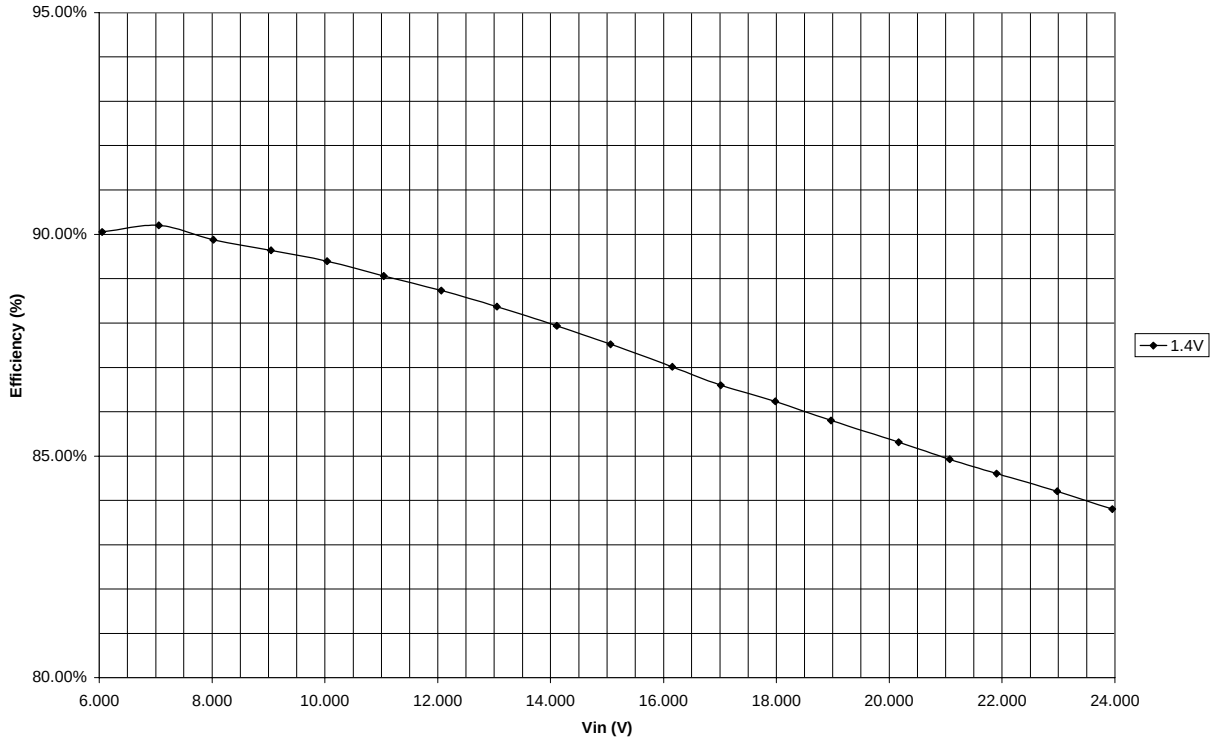
0.925V Output Power Efficiency (Vin = 10V and 19V)
2xFDS6694 + 3xFDS6674A



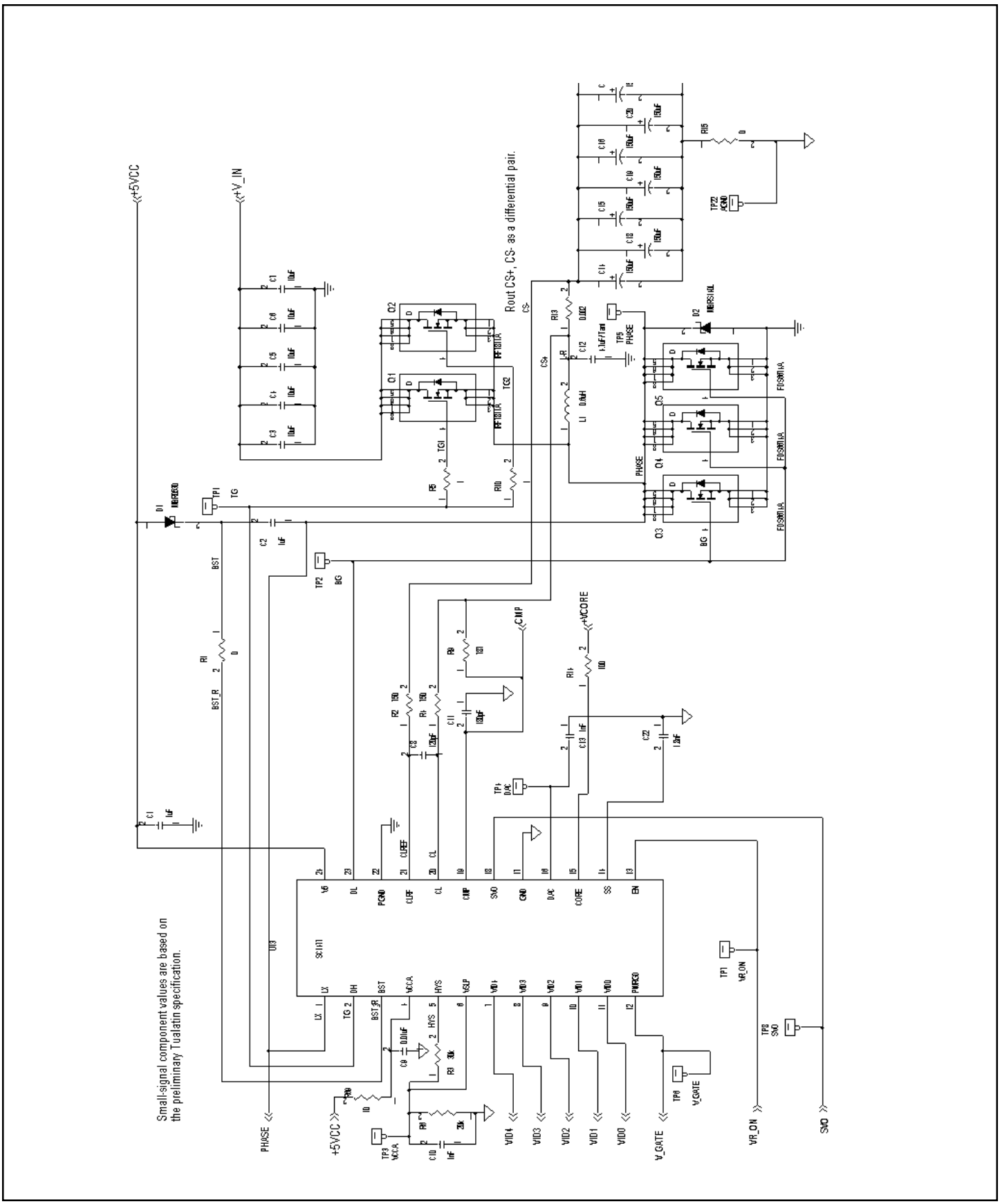
Efficiency vs. Output Voltage
Iout = 10A



Efficiency vs. Input Voltage
Iout = 10A

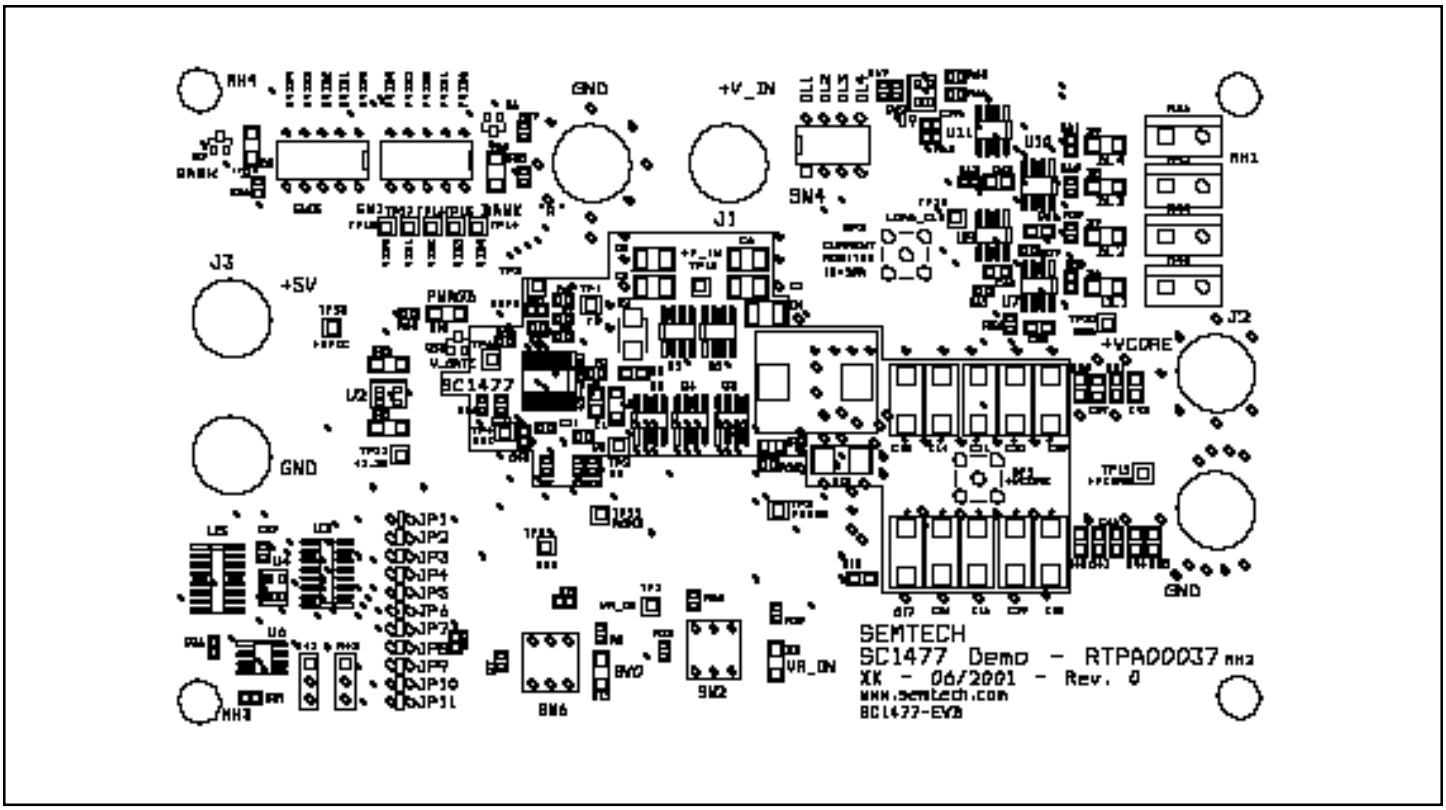


Evaluation Board Schematic

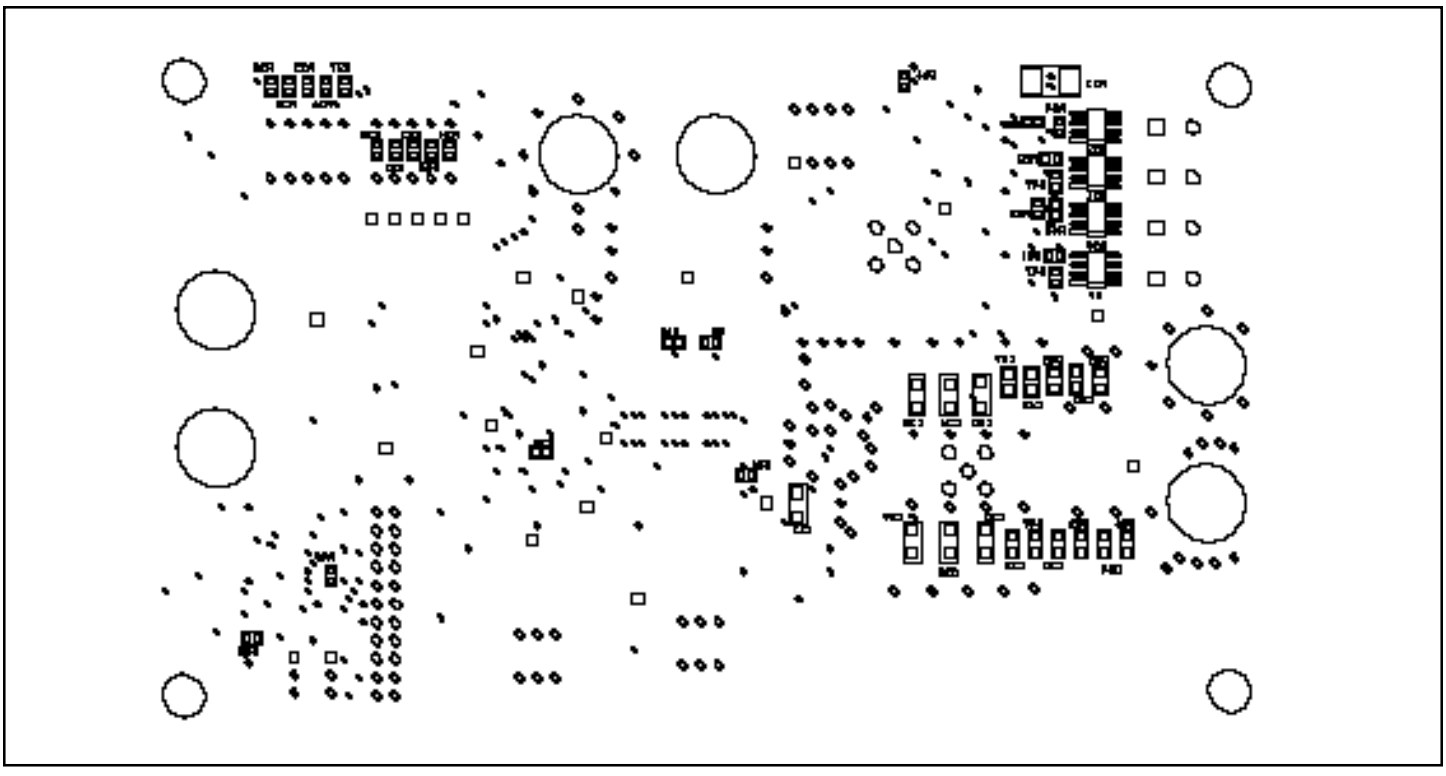


Evaluation Board Gerber Plots

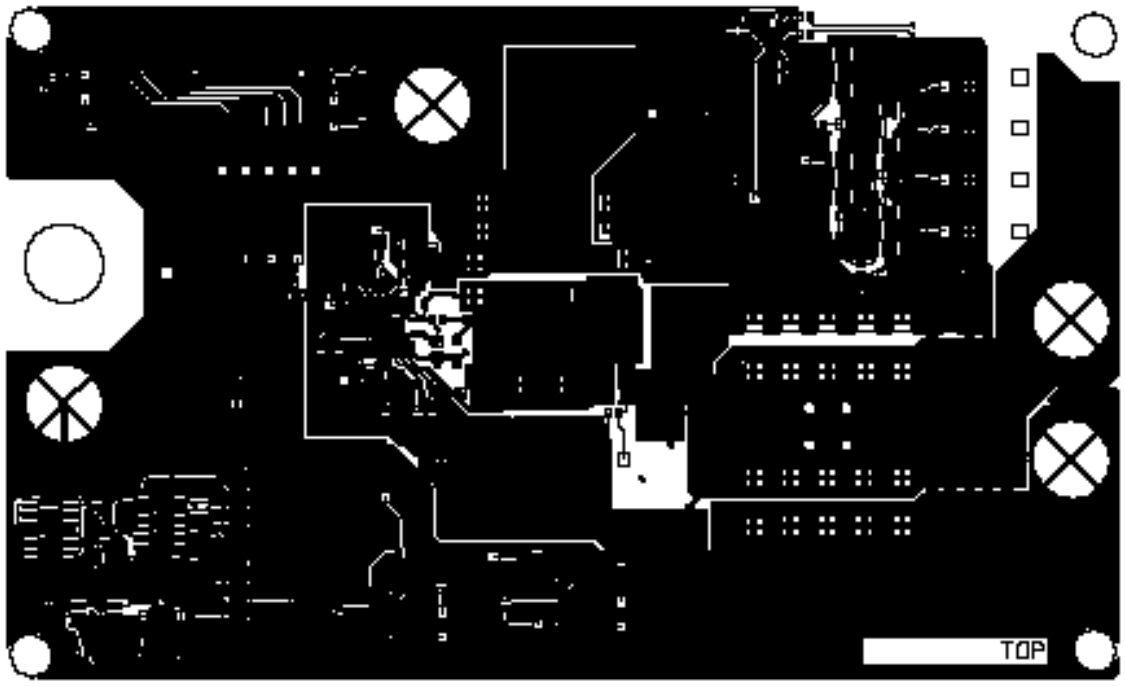
TOP ASSEMBLY



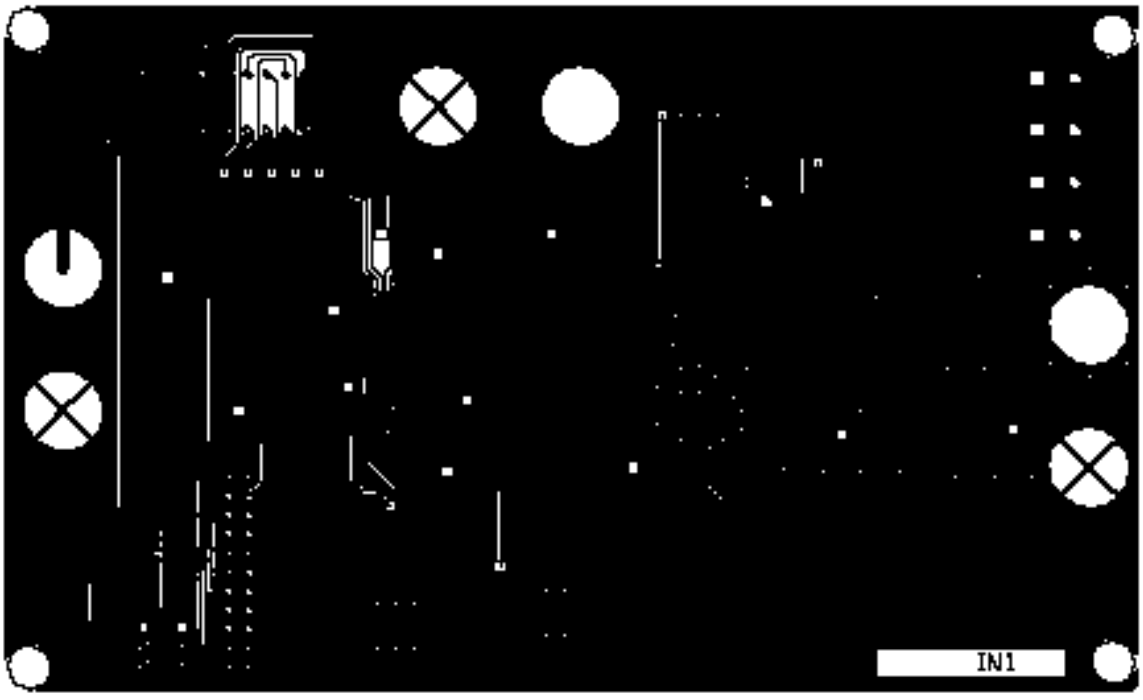
BOTTOM ASSEMBLY



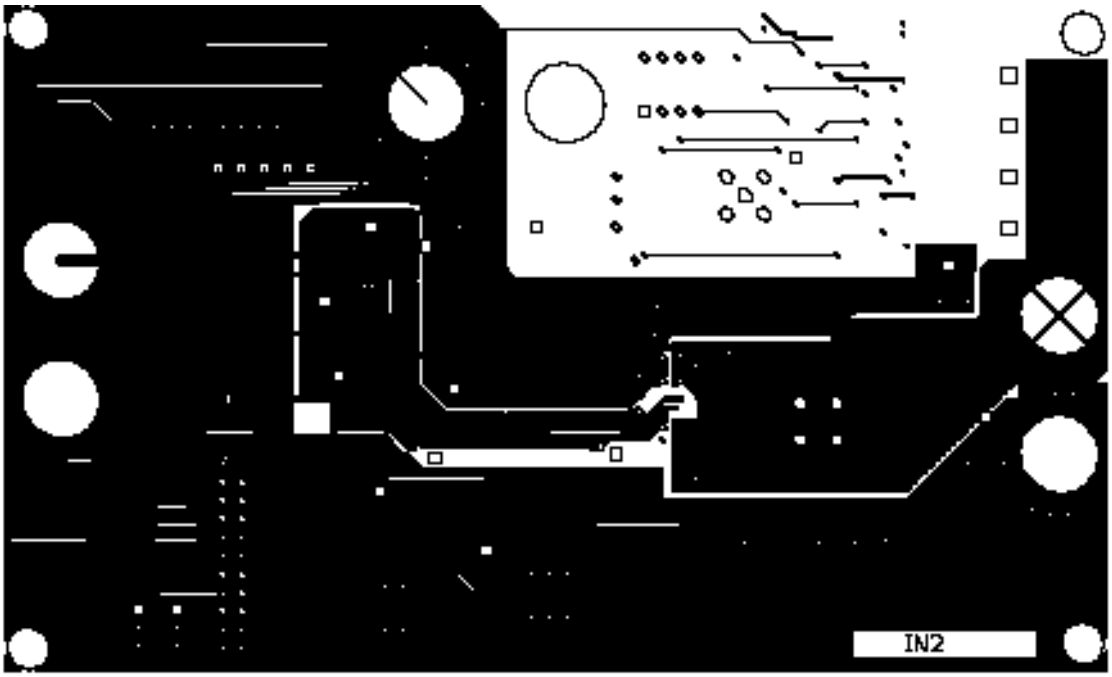
TOP



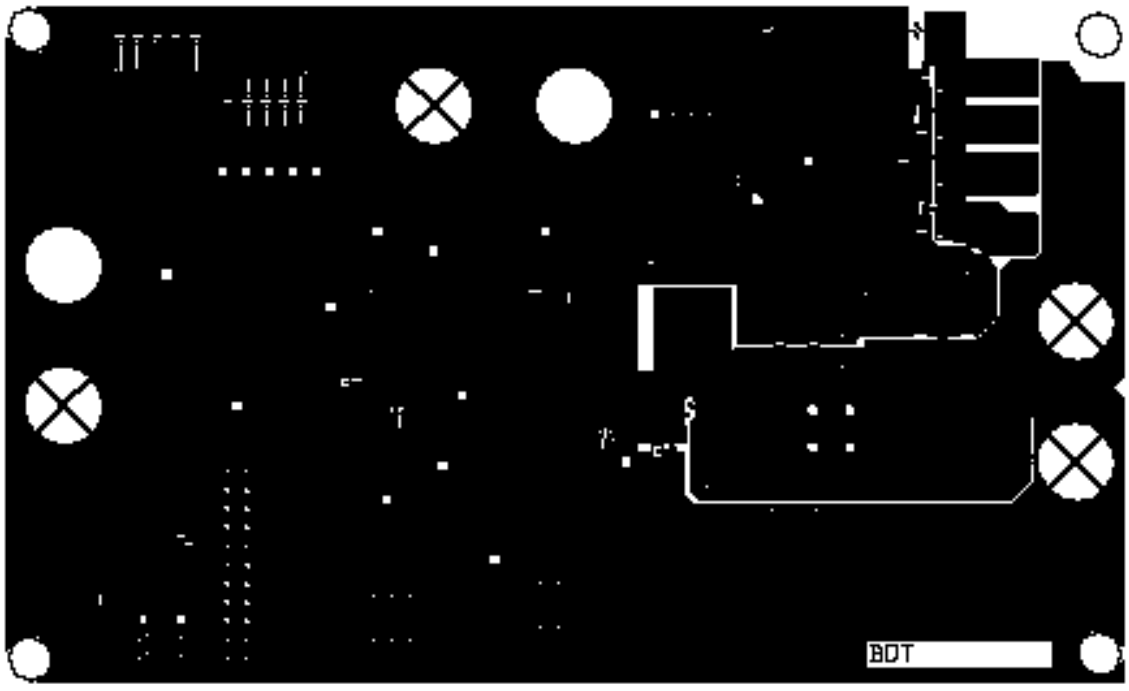
INNER1



INNER2



BOTTOM



LAYOUT GUIDELINE:

As with any high-speed switching converters, the area of high current loops needs to be minimized. The two major loops are:

1. From the input capacitors, through high-side FETS, inductor and output capacitors, returning through PGND.
2. From the low-side FETs through the inductor and output capacitors, returning through PGND.

In addition,

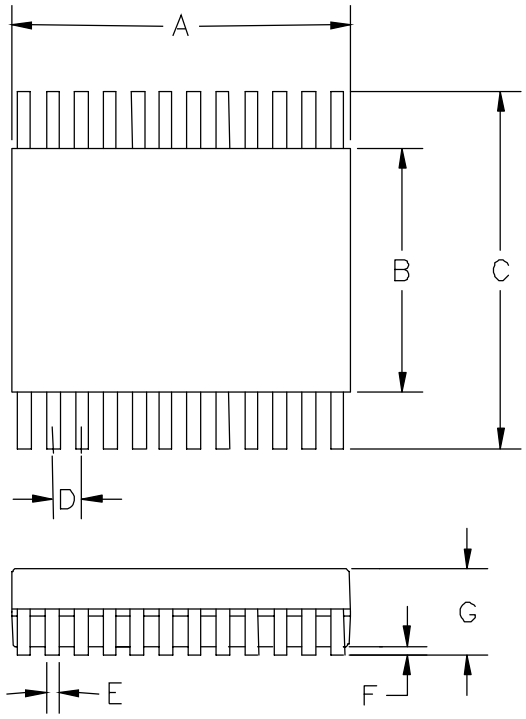
1. Separate the noisy and quiet areas of the circuit.
2. Place the SC1477 so as to reduce the trace length to the synchronous rectifiers.
3. Place the current-sense resistor as close as possible to the output capacitors; inductance from the voltage sense point to ground results in extra output ripple.
4. Connections and routing of the differential pairs are critical. The first three items are essential; the others are suggested for additional guidance.
   a. Run the traces as close together as possible.
   b. Use minimum width traces to reduce capaci tive coupling.
   c. Run a single pair as far as possible; split them at the resistors as close as possible to the SC1477; put the filter capacitors as close as possible to the device.
   d. In noisy environments, use a guard ring (ground trace around the differential pair). Tie the ring to ground every 2-4 cm.
   e. Run the traces in a quiet layer; use the minimum number of vias.
5. Minimize the area of the switching node and any other high-speed nodes.
6. Layout the protection circuitry (OVP) keeping noise in mind:
   a. Minimize the length and area of traces to the pins.
   b. Put the noise filter capacitor next to the pin.

The VRM is designed to be laid out on a 4 or more layer board with copper fill on all high current nodes.

RECOMMENDED COMPONENTS LIST:

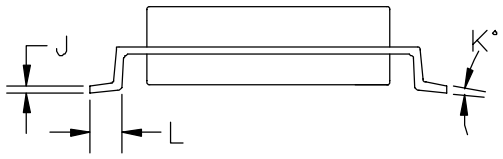
Component	Designa-tion	Part Number	Vender Name
High-Side MOSFET	Q1, Q2	IRF7811A/ FDS6694	International Rectifier/ Fairchild Semicondutor
Low-Side MOSFET	Q3, Q4, Q5	IRF7809AV/ FDS6688	International Rectifier/ Fairchild Semicondutor
Output Inductor	L1	0.6uH ETQP6F0R-6BA	Panasonic
Input Capacitor	C1--C5	10uF, 50V, 1210	Murata
Output Capacitor	C11,C1-4, C15, C16	220uF, 2.5V SP CAP	Panasonic

Outline Drawing



DIMENSIONS (1)					
DIM N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3031	.3110	7.70	7.90	(2)
B	.169	.177	4.30	4.50	(2)
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0015	.0080	.05	.15	—
G		.078		1.20	—
J	.0040	.0100	.09	.20	—
K	0°	8°	0°	8°	—
L	.022	.037	.45	.75	—

JEDEC MO-153AD



(2) DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

(1) CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern

Contact Information

Semtech Corporation
Power Management Products Division
652 Mitchell Rd., Newbury Park, CA 91320
Phone: (805)498-2111 FAX (805)498-3804