Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- Dual coaxial cable driving outputs with selectable slew rate
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Seamless interface to other HD-LINX® III family products
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C

Applications

- SMPTE 424M, SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces.

Description

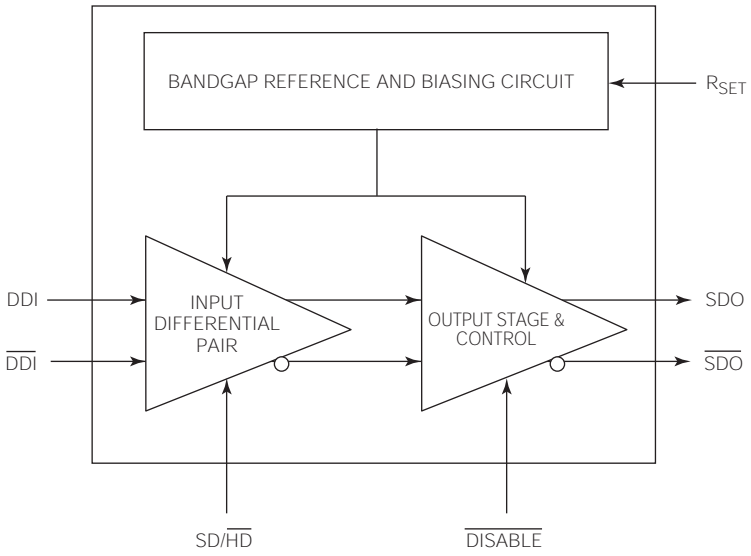
The GS2978 is a high-speed BiCMOS integrated circuit designed to drive one or two 75Ω co-axial cables.

The GS2978 may drive data rates up to 2.97Gb/s and provides two selectable slew rates in order to achieve compliance to SMPTE 424M, SMPTE 259M, SMPTE 344M and SMPTE 292M.

The GS2978 accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 168mW using a 3.3V power supply. The GS2978 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment

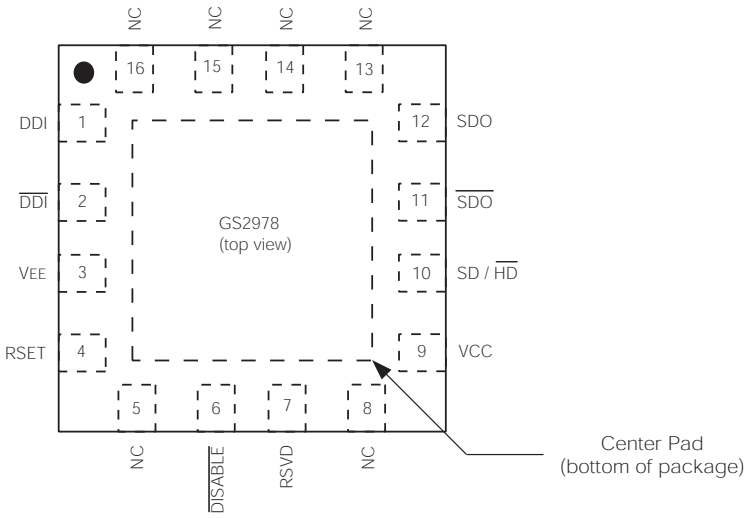


Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	DDI, $\overline{DDI}$	Analog	Input	Serial digital differential input.
3	V_{EE}	–	Power	Most negative power supply connection. Connect to GND.
4	R_{SET}	Analog	Input	External output amplitude control resistor.
5,8,13,14, 15,16	NC	–	–	No Connect. Not bonded internally.
7	RSVD	–	Reserved	Do not connect.
6	$\overline{DISABLE}$	Non Synchronous	Input	Serial output disable. When asserted LOW, the SDO/$\overline{SDO}$ output driver is powered off. SDO/$\overline{SDO}$ will float to V_{CC} through the pull-up resistor.
9	V_{CC}	–	Power	Most positive power supply connection. Connect to +3.3V.
10	SD/$\overline{HD}$	Non Synchronous	Input	Output slew rate control. When set HIGH, the output will meet SMPTE 259M rise/fall time specifications. When set LOW, the serial outputs will meet SMPTE424M and SMPTE 292M rise/fall time specifications.
11,12	$\overline{SDO}$, SDO	Analog	Output	Serial digital differential output.
–	Center Pad	–	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 12.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C
NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.	

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Power Consumption	P_D	T_A = 25°C, SDO/$\overline{\text{SDO}}$ enabled	–	168	–	mW
		T_A = 25°C, SDO/$\overline{\text{SDO}}$ disabled	–	96	–	mW
Supply Current	I_s	T_A = 25°C, SDO/$\overline{\text{SDO}}$ enabled	–	51	–	mA
		T_A = 25°C, SDO/$\overline{\text{SDO}}$ disabled	–	29	–	mA
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V
Input Voltage	V_{CMIN}	Common mode	1.4 + ΔV_{DDI}/2	–	V_{CC} - ΔV_{DDI}/2	V
SD/$\overline{\text{HD}}$, $\overline{\text{DISABLE}}$ Input	V_{IH}	I_{IH} <= 10 uA	2.0	–	–	V
	V_{IL}	I_{IL} <= 10 uA	–	–	0.8	V

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	–	–	2.97	Gb/s	1
Additive jitter	–	2.97Gb/s	–	22	–	ps_{p-p}	–
	–	1.485Gb/s	–	20	–	ps_{p-p}	–
	–	270Mb/s	–	16	–	ps_{p-p}	–
Rise/Fall time	t_r, t_f	SD/$\overline{HD}$=0	–	–	135	ps	2
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	2
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	–	–	–	35	ps	–
Duty cycle distortion	–	SD/$\overline{HD}$=0, 2.97 Gb/s	–	–	27	ps	3
	–	SD/$\overline{HD}$=0, 1.485 Gb/s	–	–	30	ps	3
	–	SD/$\overline{HD}$=1	–	–	100	ps	3
Overshoot	–	SD/$\overline{HD}$=0,	–	–	10	%	3
	–	SD/$\overline{HD}$=1	–	–	8	%	3
Output Return Loss	ORL	5 MHz – 1.485 GHz	15	20	–	dB	4
		1.485 GHz – 2.97 GHz	10	12	–	dB	4
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	3
Input Voltage Swing	$\triangle V_{DDI}$	Differential	100	–	2200	mV_{p-p}	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.
3. Single Ended into 75Ω external load.
4. ORL depends on board design. The GS2978 achieves this specification on Gennum's evaluation boards.

2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-1.The recommended standard Pb reflow profile is shown in Figure 2-2.

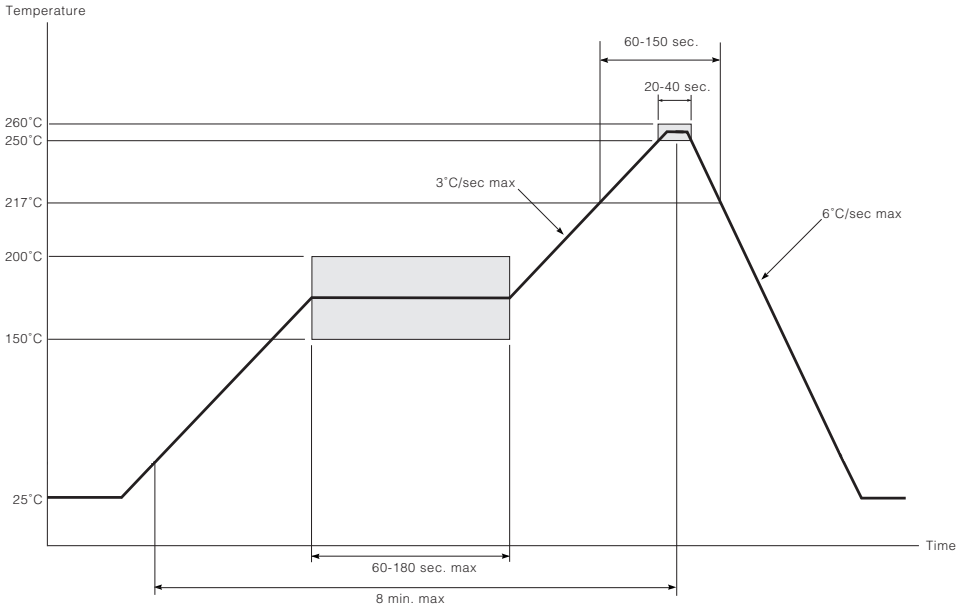


Figure 2-1: Maximum Pb-free Solder Reflow Profile (Preferred)

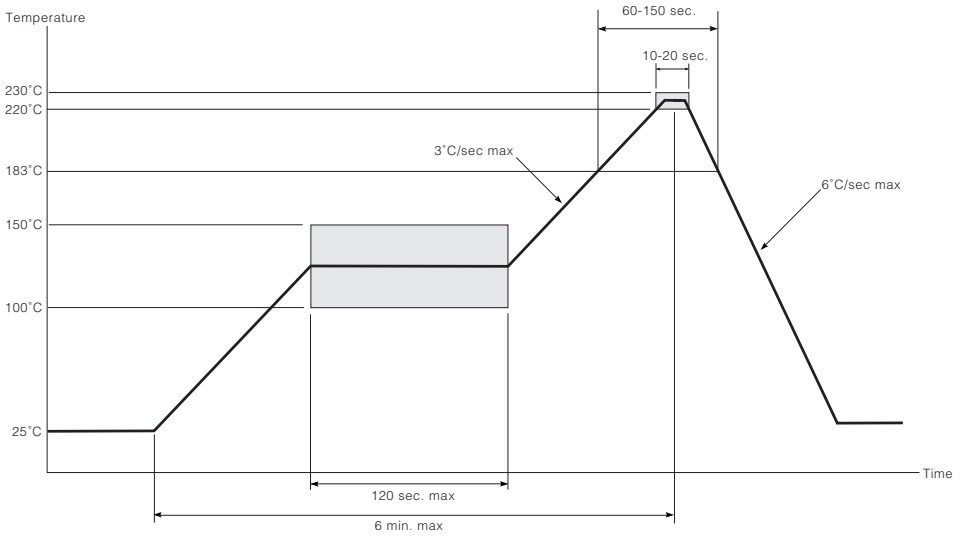


Figure 2-2: Standard Pb Reflow Profile

3. Input / Output Circuits

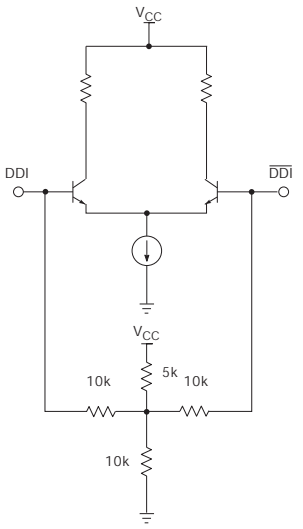


Figure 3-1: Differential Input Stage (DDI/$\overline{\text{DDI}}$)

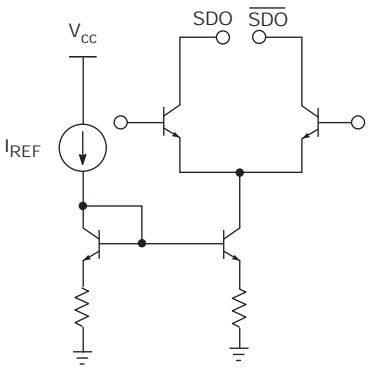


Figure 3-2: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

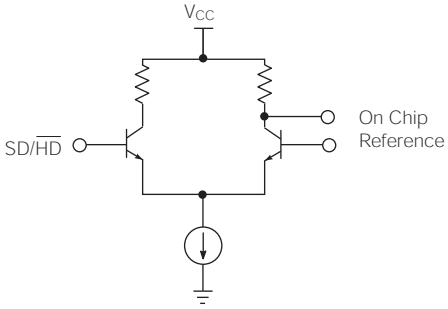


Figure 3-3: Slew Rate Select Input Stage

4. Detailed Description

4.1 Input Interfacing

DDI/$\overline{\text{DDI}}$ are high impedance differential inputs. The equivalent input circuit is shown in Figure 3-1.

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 100 and 2200mVpp.
- The common mode voltage range must be as specified in the DC Electrical Characteristics on page 4.
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS2978 inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

SD/$\overline{\text{HD}}$ Input Pin

The GS2978 SDO rise and fall times can be set to comply with both SMPTE 259M/344M and SMPTE 424M / SMPTE 292M. For all SMPTE 259M standards, or any data rate that requires longer rise and fall time characteristics, the SD/$\overline{\text{HD}}$ pin must be set HIGH by the application layer. For SMPTE 424M and SMPTE 292M standards and signals which require faster rise and fall times, this pin should be set LOW.

4.2 Output Interfacing

The GS2978 outputs are current mode, and will drive typically 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal ESD protection diodes.

In order for a DDI output circuit using the GS2978 to meet this specification, the output application circuit shown in Typical Application Circuit on page 10 is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7µF capacitor is used for AC coupling the output of the device. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring. Please see Application Information on page 10 for more details.

4.2.1 Output Amplitude (RSET)

The output amplitude of the GS2978 can be adjusted by changing the value of the R_{SET} resistor as shown in Table 4-1. For an 800mV_{p-p} output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS2978. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

Table 4-1: R_{SET} vs V_{OD}

R_{SET} R (Ω)	Output Swing (mVp-p)
995	608
824	734
750	800
680	884
573	1040

NOTE: For reliable operation of the GS2978 over the full temperature range, do not use an R_{SET} value below 573Ω.

4.2.2 Output Disable

The serial output disable ($\overline{\text{DISABLE}}$), disables power to the current mode serial digital output driver. When asserted LOW, the SDO/SDO output driver is powered off. SDO/$\overline{\text{SDO}}$ will float to V_{CC} through the pull-up resistor.

4.3 Output Return Loss Measurement

To perform a practical return loss measurement, it is necessary to force the GS2978 output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the device swing between V_{CC}-0.4V and V_{CC}-1.2V.

5. Application Information

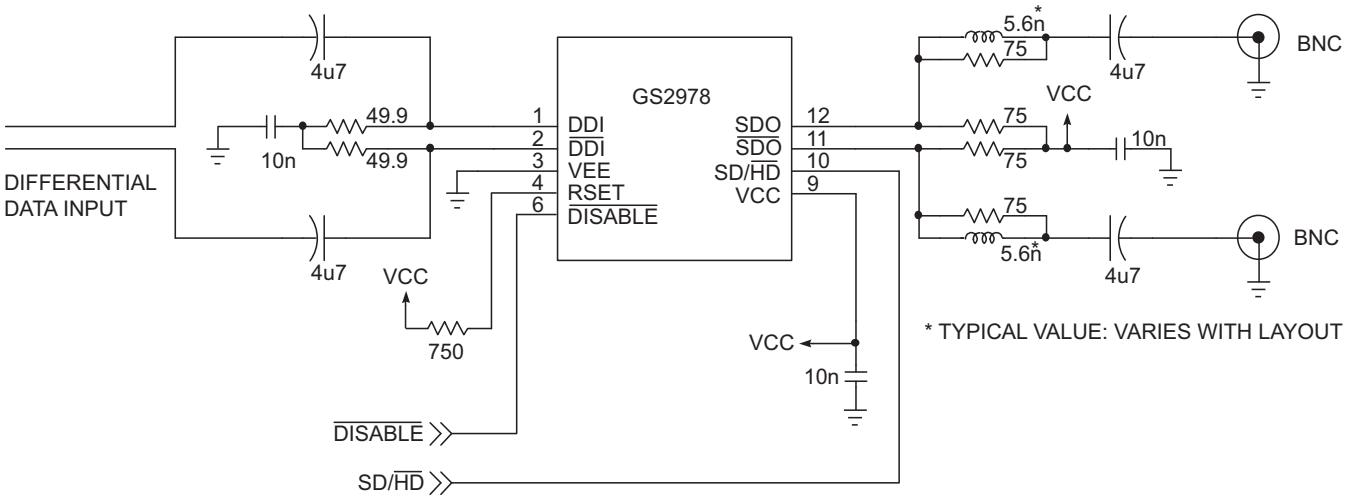
5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance.
- The PCB ground plane is removed under the GS2978 output components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS2978 R_{SET} pin and resistor to minimize parasitic capacitance.
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high speed traces which are curved to minimize impedance variations due to change of PCB trace width.

5.2 Typical Application Circuit

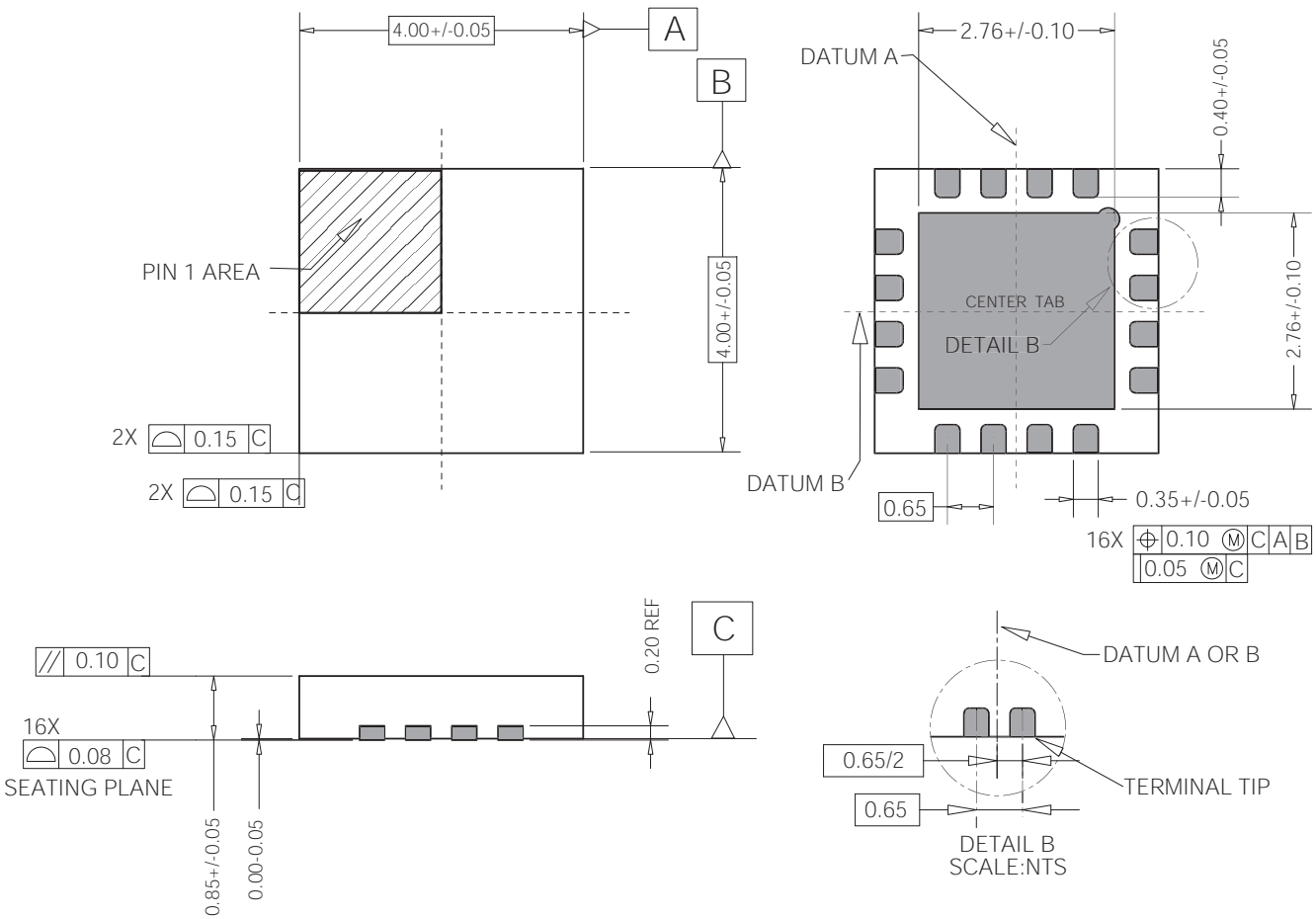


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

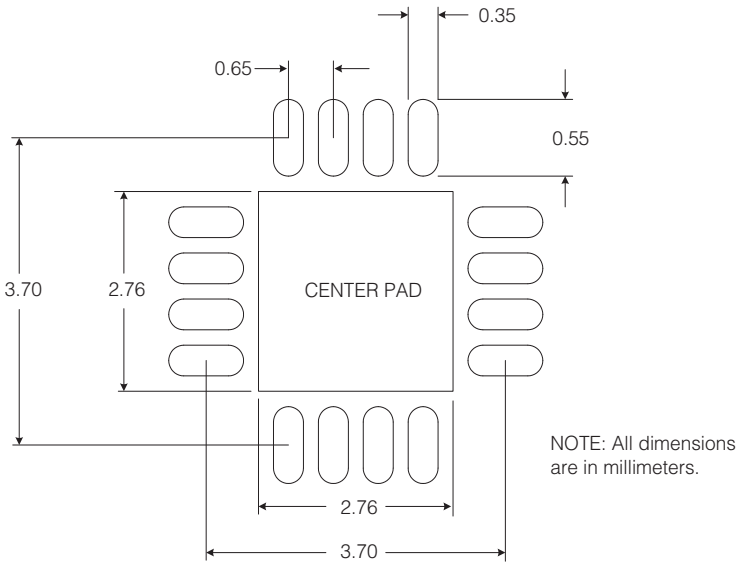
Figure 5-1: Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

6.4 Marking Diagram

6.5 Ordering Information

	Part Number	Package	Temperature Range
GS2978	GS2978-CNE3	16-pin QFN	0°C to 70°C

7. Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
A	138454	–	February 2006	New document.
B	139766	–	March 2006	Corrected pad standoff height and tolerances for pad width & package dimension. Corrected pad shape.
0	140608	–	May 2006	Changed to Preliminary Data Sheet. Removed references to trial publication for SMPTE 424M. Modified I_{IH}/I_{IL} conditions to 10 uA in DC Electrical Characteristics and additive jitter in AC Electrical Characteristics. Added section 4.3 Output Return Loss Measurement.
1	142318	–	November 2006	Converting to Data Sheet. Added section 6.4 Marking Diagram. Added typical ORL values in AC Electrical Characteristics.
2	144827	41693	April 2007	Added Table 4-1: RSET vs VOD.
3	146309	–	July 2007	Corrected part number typo in Ordering Information on page 13.
4	147552	–	September 2007	Changed Input Voltage Swing in Table 2-2: AC Electrical Characteristics.
5	147849	–	October 2007	Changed minimum value of differential input signal amplitude in Section 4.1.

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