ATS682LSH

Miniature, Two-Wire, True Zero Speed Differential Peak-Detecting Sensor IC

Features and Benefits

- True zero-speed operation
- Automatic Gain Control (AGC) for air gap independent switchpoints
- Automatic Offset Adjustment (AOA) for signal processing optimization
- Running-mode calibration for continuous optimization
- Precise duty cycle over operating temperature range
- Internal current regulator for two-wire operation
- Undervoltage lockout
- On-chip voltage regulator with wide operating voltage range and stability in the presence of a variety of complex load impedances
- Single chip IC for high reliability

Package: 4-pin SIP (suffix SH)

Not to scale

Description

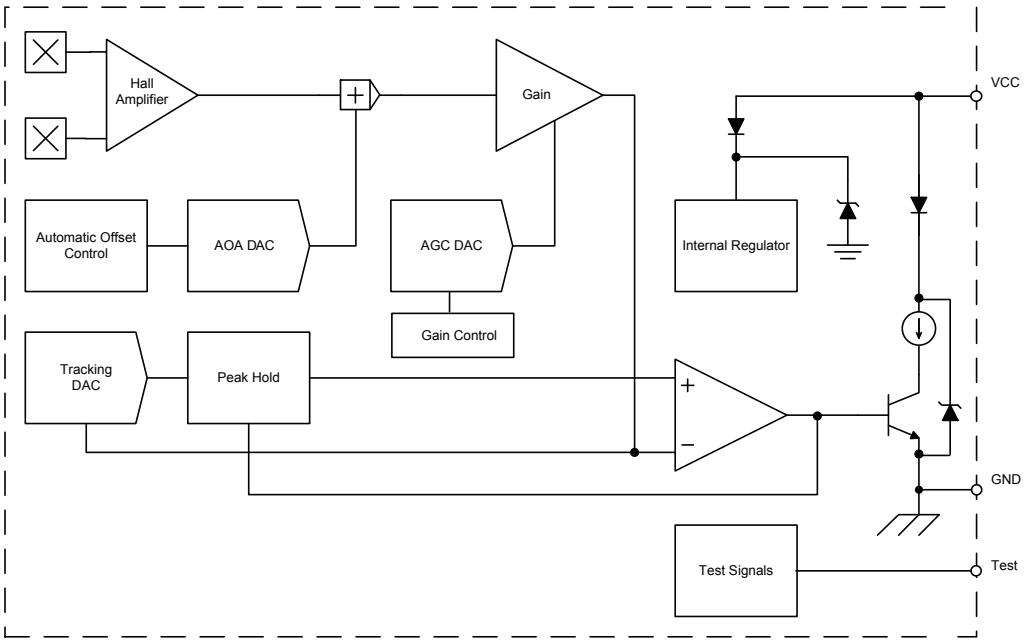
The ATS682LSH is a Hall-effect integrated circuit and rare earth pellet combination that provides a user-friendly solution for true zero-speed digital gear-tooth sensing in two-wire applications. This small package, with an optimized two-wire leadframe, can be easily assembled and used in conjunction with a wide variety of gear shapes and sizes.

The integrated circuit incorporates a dual-element Hall-effect circuit and signal processing that switches in response to differential magnetic signals created by ferrous gear teeth. The circuitry contains a sophisticated digital circuit that reduces magnet and system offsets, calibrates the gain for air gap independent switchpoints and provides true zero-speed operation.

Signal optimization occurs at power-up through the adjustment of offset and gain and is and is maintained throughout operation with the use of a running-mode calibration scheme. Running-mode calibration provides immunity from environmental effects such as micro-oscillations of the sensed target or sudden air gap changes.

The regulated current output is configured for two-wire interface circuitry and is ideally suited for obtaining speed information in wheel speed applications. The Hall element spacing is optimized for high resolution, small diameter targets. The package is lead (Pb) free, with 100% matte tin lead frame plating.

Functional Block Diagram



Selection Guide

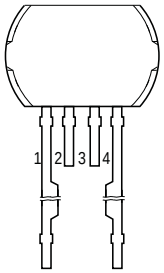
Part Number	Packing*
ATS682LSHTN-T	800 pieces per 13-in. reel

*Contact Allegro® for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to Power Derating curve	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagram



Terminal List

Number	Name	Function
1	VCC	Connects power supply to chip
2	NC	No connection
3	TEST	Test (float or tie to ground)
4	GND	Ground terminal

OPERATING CHARACTERISTICS Valid at V_{CC} and T_A within specification; unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Electrical Characteristics						
Supply Voltage[3]	V_{CC}	Operating, $T_J < T_J$(max)	4.0	–	24	V
Undervoltage Lockout	V_{CCUV}	V_{CC} = 0 → 5 V or 5 → 0 V	–	–	3.95	V
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC}$(max) + 3 mA, T_A = 25°C	28	–	–	V
Supply Zener Current	I_Z	T_A = 25°C, V_S = 28 V	–	–	19.8	mA
Supply Current	$I_{CC(LOW)}$		5.0	7	8.4	mA
	$I_{CC(HIGH)}$		11.8	14	16.8	mA
Supply Current Ratio	$I_{CC(HIGH)}/I_{CC(LOW)}$	Measured as ratio of high current to low current	1.9	–	–	–
Reverse Battery Current[4]	I_{RCC}	V_{RCC} = –18 V	–	–	–5	mA
Power-On State Characteristics						
Power-On Time[5]	t_{PO}	$V_{CC} > V_{CC}$(min), f_{OP} < 100 Hz	–	1	2	ms
Power-On State[6]	POS	$t > t_{PO}$	–	$I_{CC(HIGH)}$	–	–
Output Stage						
Output Slew Rate[7,8]	dI/dt	R_{SENSE} = 100 Ω, C_{LOAD} = 10 pF, no C_{BYP} (see figure 7)	–	14	–	mA/µs
Performance Characteristics						
Operating Frequency[9]	f_{OP}		0	–	8000	Hz
Analog Signal Bandwidth	BW		20	40	–	kHz
Operate Point	B_{OP}	Magnitude (see figure 6)	–	120	–	mV
Release Point	B_{RP}	Magnitude (see figure 6)	–	120	–	mV
Calibration						
Initial Calibration	CAL_I	Quantity of rising output (current) edges required for accurate edge detection; edge accuracy not guaranteed during initial calibration.	–	–	3	edge

Continued on the next page…

OPERATING CHARACTERISTICS (continued) Valid at V_{CC} and T_A within specification; unless otherwise noted

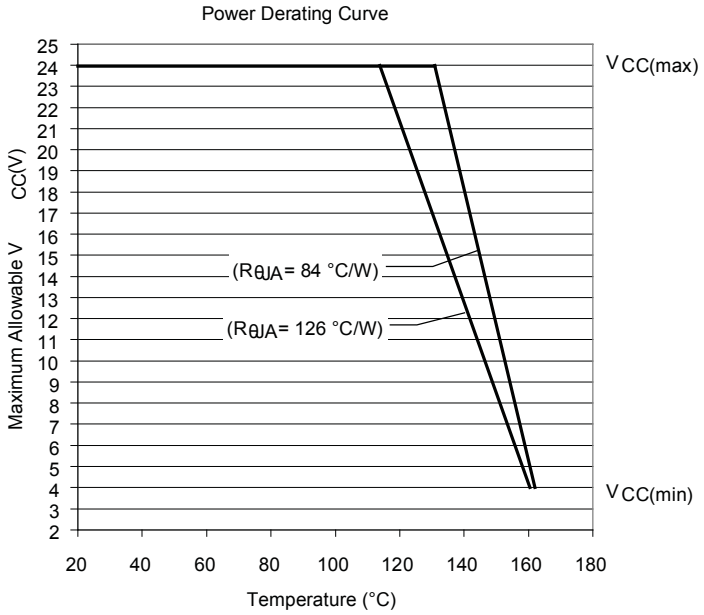
Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit[2]
Digital-to-Analog Converter (DAC) Characteristics						
Allowable User-Induced Differential Offset	$\Delta B_{DIFFEXT}$	Operation within specification	–	± 60	–	G
Functional Characteristics						
Operating Signal Range[10]	B_{DIFF}	Differential signal, measured peak-to-peak; operation within specification	30	–	1000	G
Minimum Operating Signal	$B_{DIFFOP(MIN)}$	Output switching (no missed edges); duty cycle not guaranteed	20	–	–	G
Allowable Signal Amplitude Variation	B_{SOA}	See Functional Description section	–	–	–	–
Operational Air Gap Range	AG	Using Reference Target 60-0, duty cycle within specification	0.5	–	2.75	mm
Maximum Operational Air Gap Range	$AG_{OP(MAX)}$	Using Reference Target 60-0, output switching (no missed edges); duty cycle not guaranteed	–	–	3.00	mm
Duty Cycle[11]	D	AG within specification	41	–	61	%
Consecutive Duty Cycle Variation[12]	err_D	AG = 1.5 mm	–	±1.5	–	%

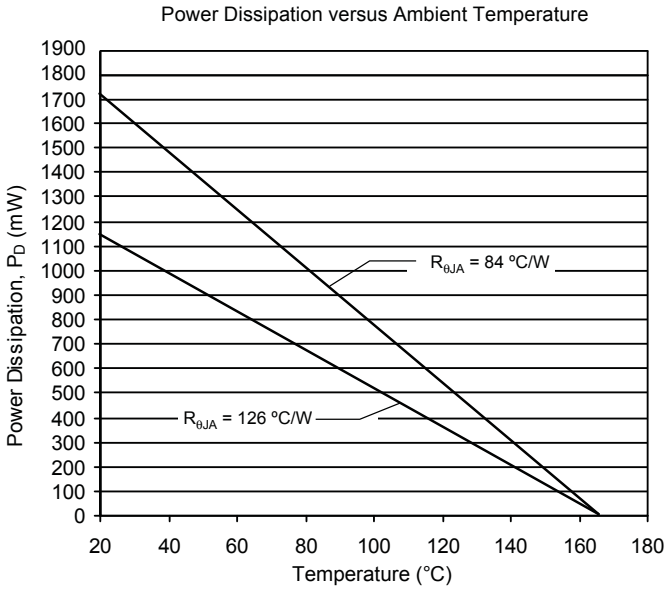
[1]Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]1 G (gauss) = 0.1 mT (millitesla).
[3]Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.
[4]Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[5]Power-On Time includes the time required to complete the internal automatic offset adjust after which the DAC is ready for peak acquisition.
[6]See Device Operation section.
[7]dI is the difference between 10% of $I_{CC(LOW)}$ and 90% of $I_{CC(HIGH)}$, and dt is the time period between those two points.
[8]C_{LOAD} is the probe capacitance of the oscilloscope used to make the measurement.
[9]Refer to Functional Description section for performance over input magnetic frequency.
[10]AG is dependent on the available magnetic field. The available field is dependent on target geometry and material, and should be independently characterized. The field available from the Reference Target is given in the Reference Target parameter section of the datasheet.
[11]Target rotation from pin 4 to pin 1.
[12]Consecutive Duty Cycle Variation represents the difference between consecutive duty cycles, D(n) – D(n–1); mean ± 3 sigma.

Thermal Characteristics may require derating at maximum conditions, see Power Derating section

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	126	°C/W
		Single layer PCB, with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) copper area each side	84	°C/W

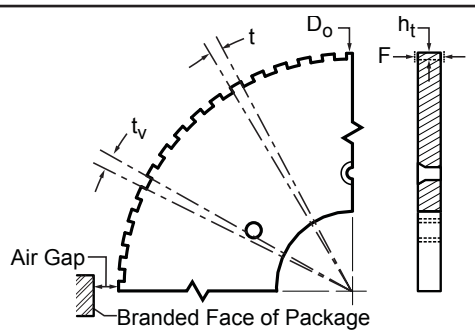
*Additional thermal information available on the Allegro website

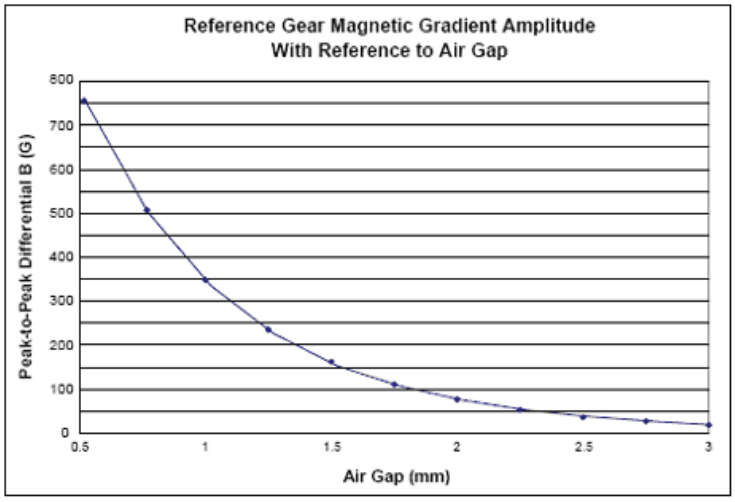


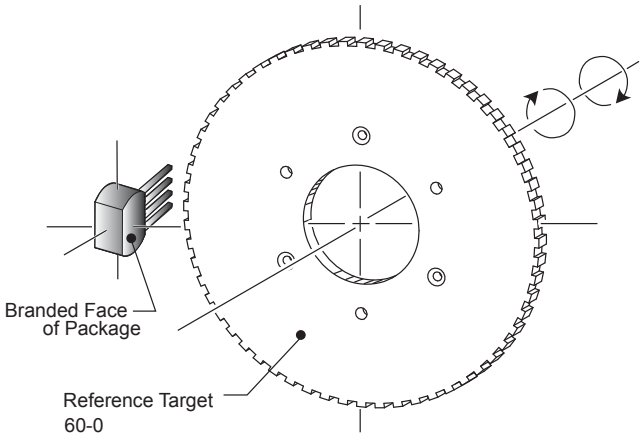


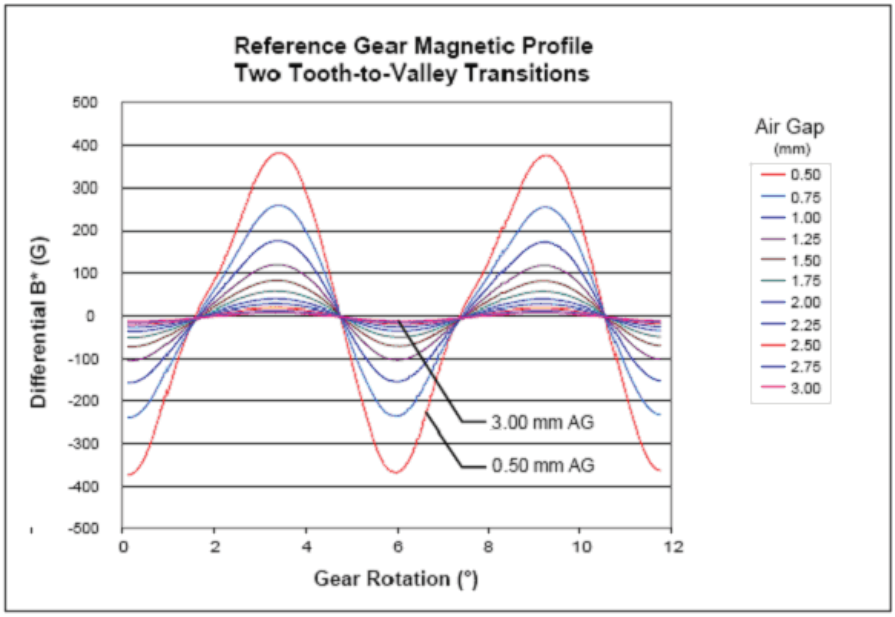
Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Angular Tooth Thickness	t	Length of tooth, with respect to branded face	3	deg.	
Angular Valley Thickness	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	



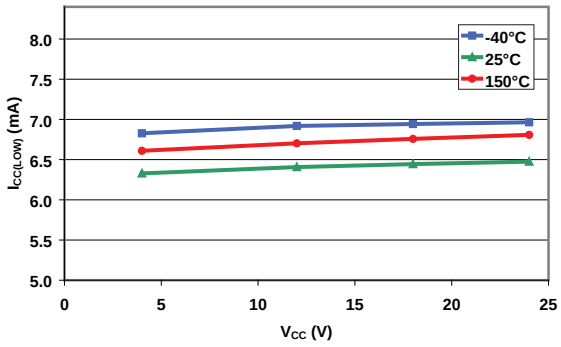




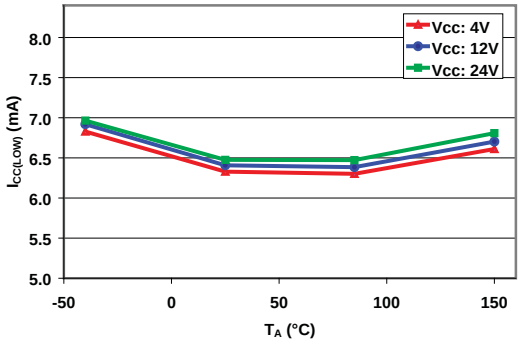


Characteristic Performance

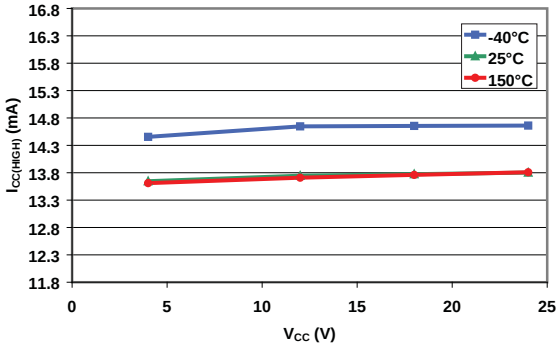
Supply Current (Low) versus Supply Voltage



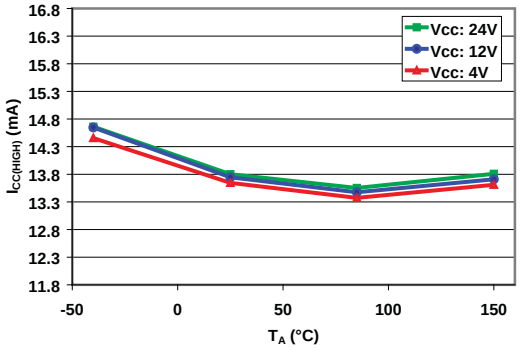
Supply Current (Low) versus Ambient Temperature



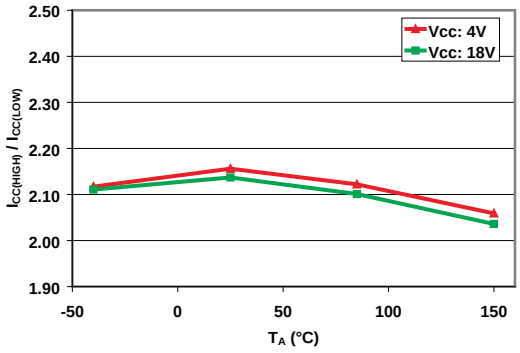
Suppply Current (High) versus Supply Voltage

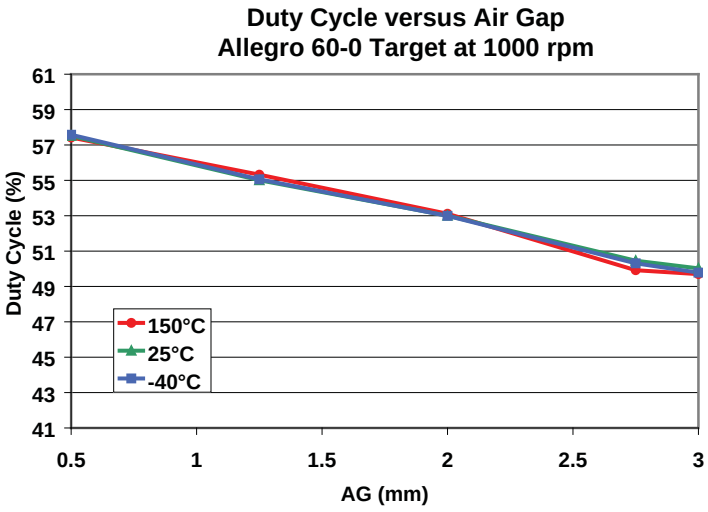


Supply Current (High) versus Ambient Temperature

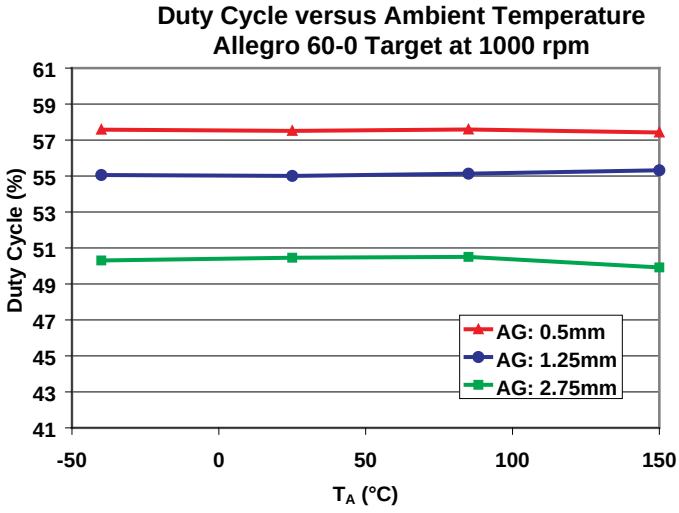


Supply Current Ratio versus Ambient Temperature





The trend of duty cycle versus air gap is driven by the actual magnetic profile of the target (see Reference Target figures)



Functional Description

Hall Technology

This single-chip differential Hall-effect sensor IC possesses two Hall elements spaced at a fixed distance (1.5 mm), which simultaneously are affected by the magnetic profile of the target, and generate a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset compensation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling

An operating device is capable of providing digital information that is representative of the magnetic features on a rotating target. The waveform diagram shown in figure 3 represents the automatic translation of the magnetic profile to the digital output signal of the IC.

Output Polarity

Figure 3 shows the output polarity for the orientation of the target and package shown in figure 2. The target direction of rotation shown is perpendicular to the leads, across the face of the device, from pin 1 to pin 4. This results in the IC output switching from high, $I_{CC(HIGH)}$, to low $I_{CC(LOW)}$, as the leading edge of a tooth (a rising mechanical edge, as detected by the IC) passes the branded face. In this configuration, the device output current switches to its low polarity when a tooth is the target feature nearest to the branded face. If the direction of rotation is reversed, then the output polarity inverts.

Note: the translated output voltage polarity is dependent on the position of a sense resistor, R_{SENSE} (see figure 4).

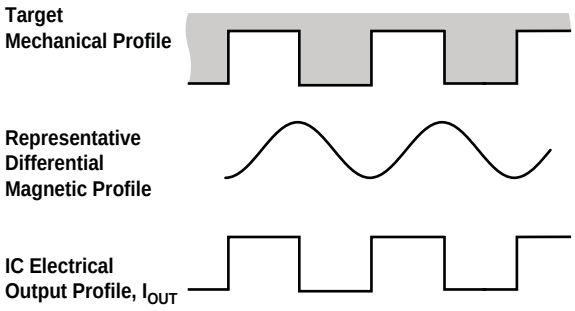


Figure 3. Output Profile of a gear target for the polarity indicated in figure 2.

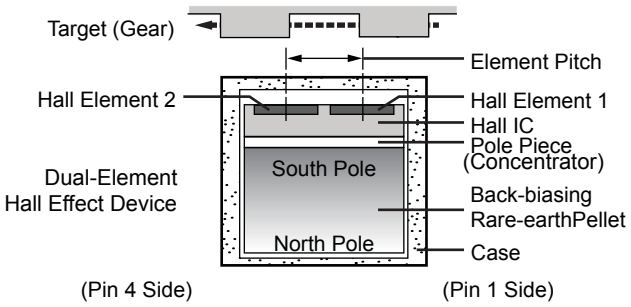


Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

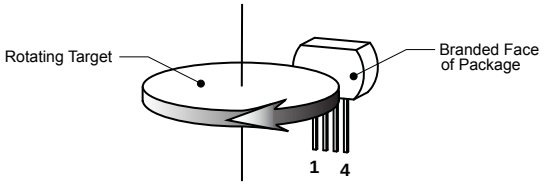


Figure 2. This left-to-right (pin 1 to pin 4) direction of target rotation results in a low output signal when a tooth of the target gear is nearest the face of the package (see Figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

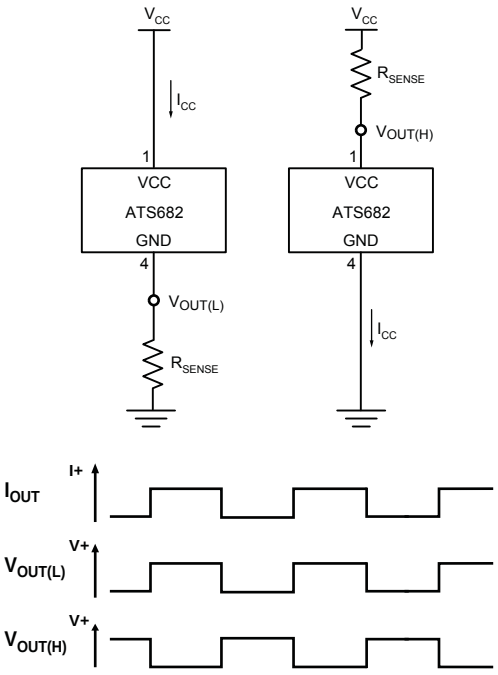


Figure 4. Voltage profiles for high-side and low-side two-wire sensing.

Automatic Gain Control (AGC)

AGC allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the operating signal range specification). During calibration, the device determines the peak-to-peak amplitude of the signal generated by the target and automatically adjusts the signal gain. Figure 5 illustrates the effect of this feature.

Automatic Offset Adjust (AOA)

AOA circuitry automatically compensates for the effects of chip, magnet, and installation offsets. (For capability, see Allowable User-Induced Differential Offset, in the Operating Characteristics table.) This circuitry is continuously active in both calibration mode and running mode. Continuous operation of AOA allows the IC to compensate for offset drift and for offsets induced by temperature variations over time.

Digital Peak Detection

A digital-to-analog converter (DAC) tracks the internal analog voltage signal V_{PROC}, and is used for holding the peak value of the internal analog signal. In the example shown in figure 6, the DAC would first track up with the signal and hold the upper peak value. When V_{PROC} drops below this peak value by B_{OP}, the device hysteresis, the output switches, and the DAC begin tracking the signal downward toward the negative V_{PROC} peak. After the DAC acquires the negative peak, the output again switches states when V_{PROC} is greater than the peak by the value B_{RP}. At this point, the DAC tracks up again and the cycle repeats. The digital tracking of the differential analog signal allows the IC to achieve true zero-speed operation.

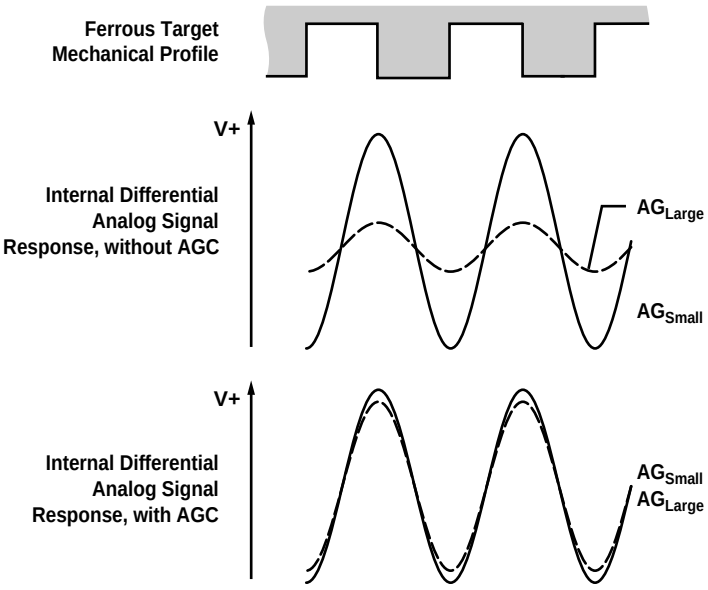


Figure 5: Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap affect the magnetic gradient, but AGC prevents that from affecting device performance, as shown in the lowest panel.

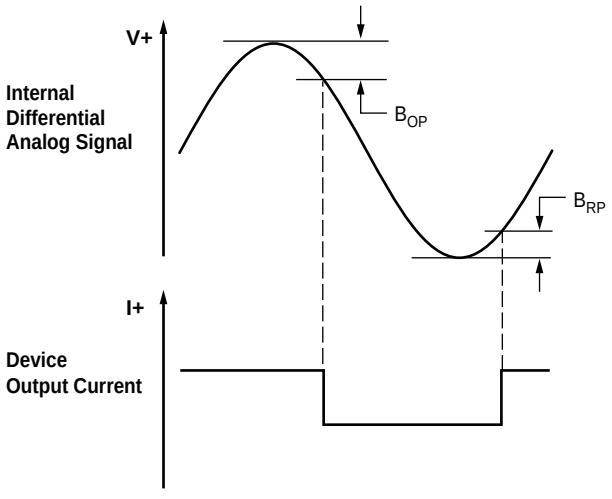


Figure 6. Peak detection switchpoint detail

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 7 for an example of a basic application circuit.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout threshold, $V_{CC(UV)}$, the device enters Reset mode, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. I_{CC} levels may not meet datasheet limits when $V_{CC} < V_{CC}(min)$.

Assembly Description

This device is molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction. Refer to the Allegro website, www.allegromicro.com, for more specific applications notes on finished package processing.

Diagnostics

The regulated current output is configured for two-wire applications, requiring one less wire for operation than do switches with the traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges, shown in figure 8 as $I_{CC(HIGH)}$ and $I_{CC(LOW)}$. Any current level not within these ranges indicates a fault condition. If $I_{CC} > I_{CC(HIGH)}(max)$, then a short condition exists, and if $I_{CC} < I_{CC(LOW)}(min)$, then an open condition exists. Any value of I_{CC} between the allowed ranges for $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ indicates a general fault condition.

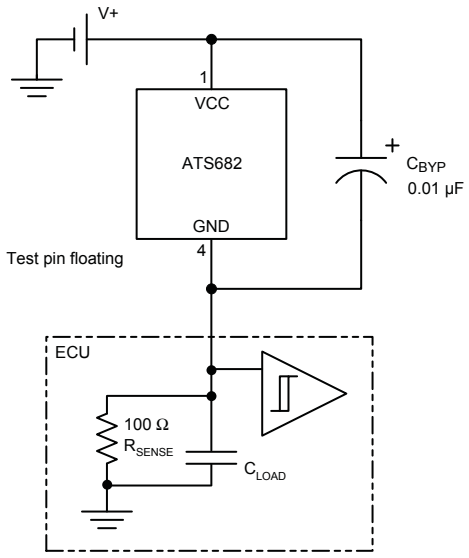


Figure 7. Typical application circuit

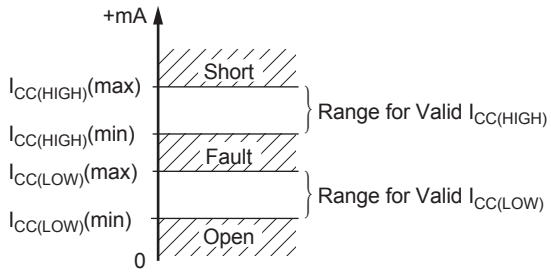


Figure 8. Diagnostic characteristics of supply current values

Device Operation

Power-On When power ($V_{CC} > V_{CC}(min)$) is applied to the device, a short period of time is required to activate the various portions of the IC. During this period, the ATS682 powers-on in the high current state, $I_{CC(HIGH)}$. After power-on, there are conditions that could induce a change in the output state. Such an event could be caused by thermal transients, but it would also require a static applied magnetic field, proper signal polarity, and particular direction and magnitude of internal signal drift.

Initial Offset Adjust The IC initially compensates for differential offset, ΔB_{APP}, that results from chip, magnet, and installation alignment. Once the effective differential magnetic offset has been cancelled, the digital tracking DAC is ready to track the signal and provide output switching.

The period of time required for both power-on and initial offset adjust is defined as the Power-On Time specification.

Calibration Mode The calibration mode allows the IC to automatically select the proper signal gain and continue to adjust for DC differential magnetic offset. The AGC is active, and selects the optimal signal gain based on the amplitude of the V_{PROC} signal. Following each adjustment to the AGC DAC, the Offset DAC is also adjusted to ensure the internal analog signal is properly centered. During this mode, the tracking DAC is active and output switching occurs, but the duty cycle is not guaranteed to be within specification.

Running Mode After the initial calibration process (CAL_I edges) establishes a signal gain, the device moves to Running mode. During Running mode, the IC tracks the input signal and continues to give an output edge for every peak of the signal. AOA remains active to compensate for any offset drift over time.

The ATS682 also incorporates an algorithm for adjusting the signal gain during Running mode. This algorithm is designed to optimize the V_{PROC} signal amplitude in instances where the magnetic signal during the calibration period is not representative of the amplitude of the magnetic signal for the installed application air gap (see figure 9).

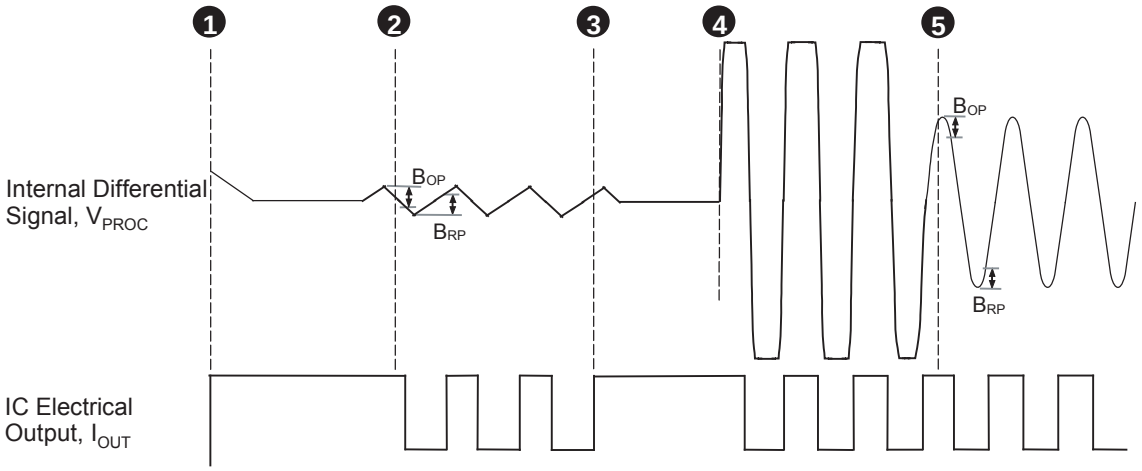


Figure 9: Operation of Running Mode Gain Adjust.
Position 1. The device is initially powered-on. Self-calibration occurs.
Position 2. Small amplitude oscillation of the target sends an erroneously small differential signal to the device. The amplitude of V_{PROC} is greater than the switching hysteresis (B_{OP} and B_{RP}), and the device output switches.
Position 3. The calibration period completes on the third rising output edge, and the device enters Running mode.
Position 4. True target rotation occurs and the correct magnetic signal is generated for the installation air gap. The established signal gain is too large for the rotational magnetic signal of the target, at the given air gap.
Position 5. Running mode calibration corrects the signal gain to an optimal level for the installation air gap.

Characteristic Allowable Signal Amplitude Variation

The colored area in figure 10 shows B_{SOA}, the safe operating area of allowable magnetic signal amplitude within which the IC will continue output switching. The output duty cycle is wholly dependent on the magnetic signature of the target across the air gap range of movement, and may not always be within specification throughout the entire operating region (to $B_{DIFF}(max)$). Signal amplitude changes may be due to deflection (relative air gap change between Hall element and target), target eccentricity, magnet temperature coefficient or a combination thereof.

The axis parameters for the chart in figure 10 are defined in figure 11. As an example, assume the case where the signal changes from the nominal at the installed air gap (B_{CAL}) within the range defined by an increase factor of $B_{DIFF}(max) / B_{CAL} = 3.0$, and a decrease of $B_{DIFF(lim)} / B_{CAL} = 0.75$. This case is plotted with an "x" in figure 10.

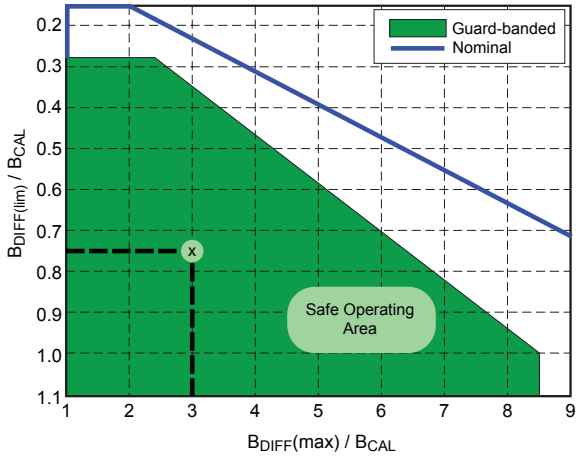


Figure 10. Allowable Signal Amplitude Change chart

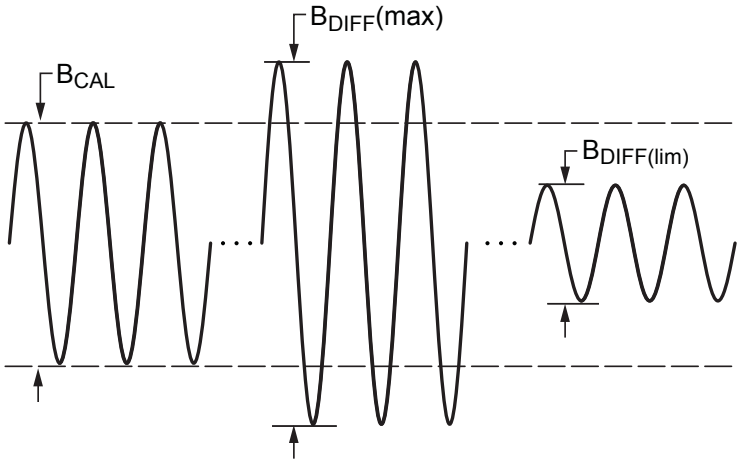


Figure 11. Illustration of B_{CAL}, $B_{DIFF}(max)$ and $B_{DIFF(lim)}$ for amplitude variation discussion. B_{CAL} is the magnetic amplitude at the IC during its calibration cycle $B_{DIFF}(max)$ and $B_{DIFF(lim)}$ are the maximum and minimum magnetic amplitudes during IC operation.

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 7 mA, and $R_{\theta JA}$ = 126 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7\ mA = 84\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 84\ mW \times 126\ °C/W = 10.6°C$$

$$T_J = T_A + \Delta T = 25°C + 10.6°C = 35.6°C$$

A worst-case estimate, P_D(max), represents the maximum allowable power level (V_{CC}(max), I_{CC}(max)), without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=126°C/W, T_J(max)=165°C, V_{CC}(max)=24 V, and I_{CC} = 16.8 mA.

Calculate the maximum allowable power level, P_D(max). First, invert equation 3:

$$\Delta T(max) = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T(max) \div R_{\theta JA} = 15°C \div 126\ °C/W = 119\,mW$$

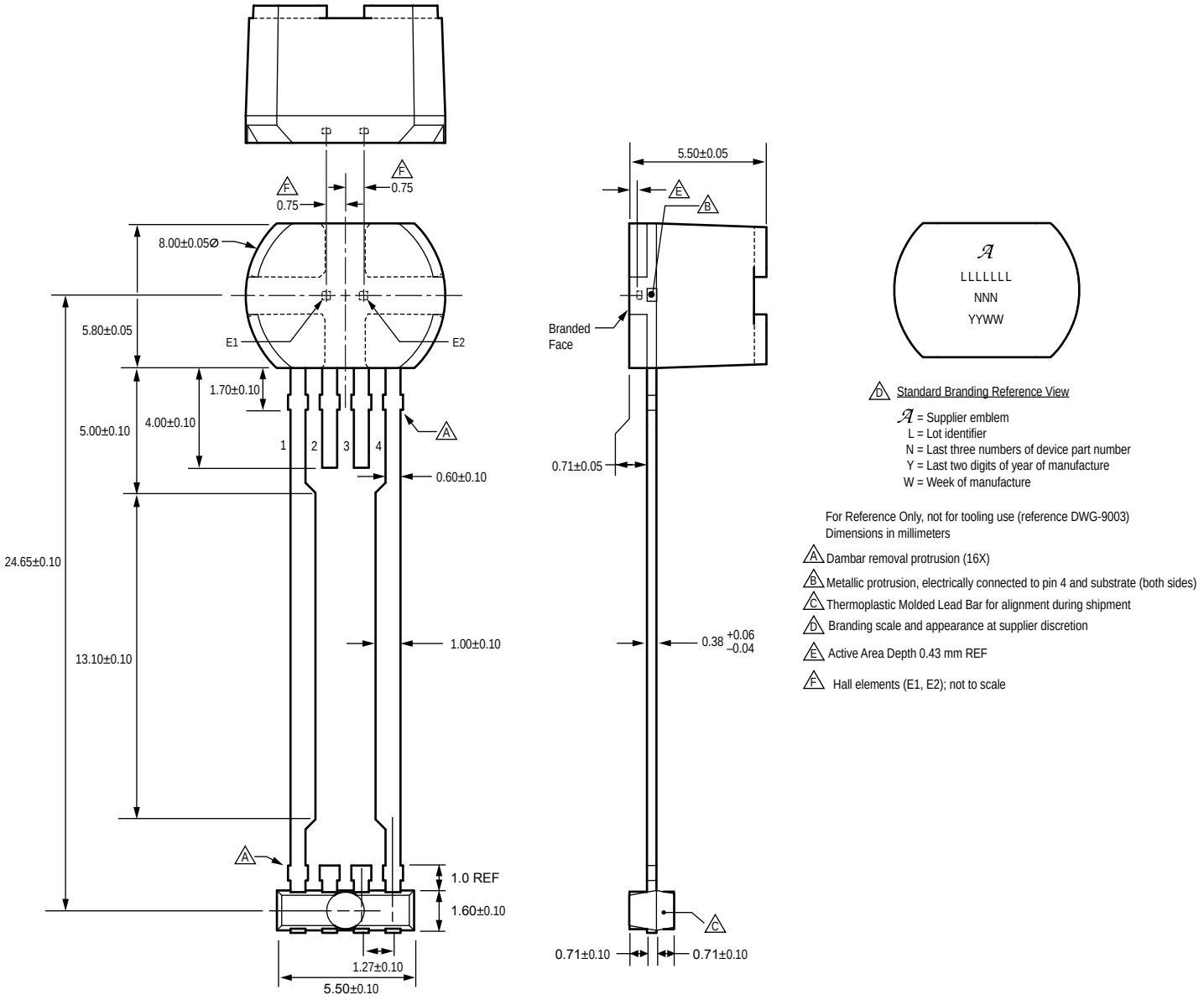
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC} = 119\,mW \div 16.8\,mA = 7.1V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to V_{CC}(max). If $V_{CC(est)} \leq V_{CC}$(max), then reliable operation between $V_{CC(est)}$ and V_{CC}(max) requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and V_{CC}(max) is reliable under these conditions.

Package SH 4-Pin SIP



D Standard Branding Reference View

A = Supplier emblem
L = Lot identifier
N = Last three numbers of device part number
Y = Last two digits of year of manufacture
W = Week of manufacture

For Reference Only, not for tooling use (reference DWG-9003)
Dimensions in millimeters

A Dambar removal protrusion (16X)

B Metallic protrusion, electrically connected to pin 4 and substrate (both sides)

C Thermoplastic Molded Lead Bar for alignment during shipment

D Branding scale and appearance at supplier discretion

E Active Area Depth 0.43 mm REF

F Hall elements (E1, E2); not to scale

The products described herein are manufactured under one or more of the following U.S. patents: 5,264,783; 5,389,889; 5,442,283; 5,517,112; 5,581,179; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; 6,091,239; 6,100,680; 6,232,768; 6,242,908; 6,265,865; 6,297,627; 6,525,531; 6,690,155; 6,693,419; 6,919,720; 7,046,000; 7,053,674; 7,138,793; 7,199,579; 7,253,614; 7,365,530; 7,368,904; 7,518,414; 7,548,056; and other patents pending.

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