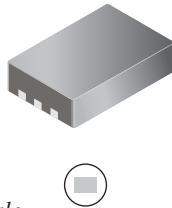


Micro Power 3 V Linear Hall Effect Sensor ICs with Tri-State Output and User-Selectable Sleep Mode

Features and Benefits

- High-impedance output during sleep mode
- Compatible with 2.5 to 3.5 V power supplies
- 10 mW power consumption in the active mode
- Miniature MLP/DFN package
- Ratiometric output scales with the ratiometric supply reference voltage (VREF pin)
- Temperature-stable quiescent output voltage and sensitivity
- Wide ambient temperature range: -20°C to 85°C
- ESD protection greater than 3 kV
- Solid-state reliability
- Preset sensitivity and offset at final test

Package: 6 pin MLP/DFN (suffix EH)



Approximate scale

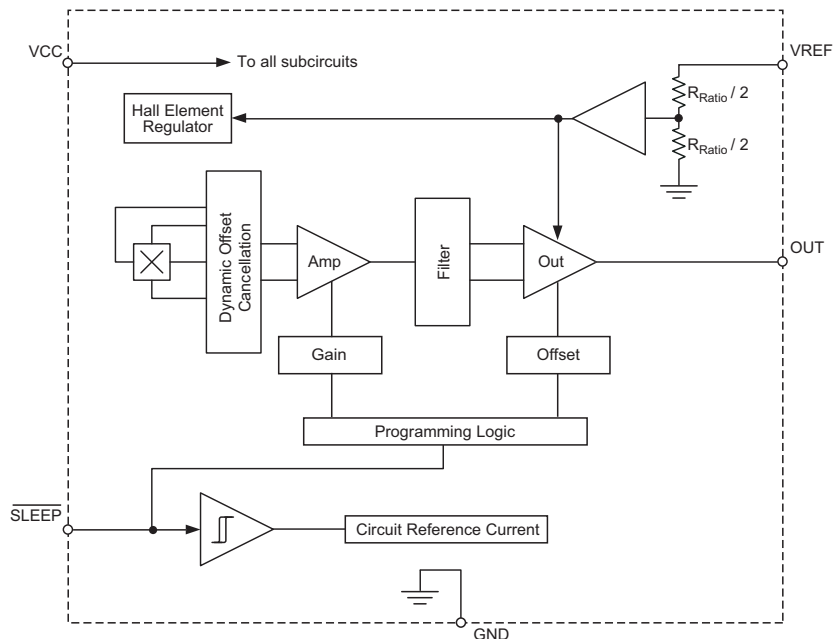
Description

The A139x family of linear Hall effect sensor integrated circuits (ICs) provide a voltage output that is directly proportional to an applied magnetic field. Before amplification, the sensitivity of typical Hall effect ICs (measured in mV/G) is directly proportional to the current flowing through the Hall effect transducer element inside the ICs. In many applications, it is difficult to achieve sufficient sensitivity levels with a Hall effect sensor IC without consuming more than 3 mA of current. The A139x minimize current consumption to less than 25 μA through the addition of a user-selectable sleep mode. This makes these devices perfect for battery-operated applications such as: cellular phones, digital cameras, and portable tools. End users can control the current consumption of the A139x by applying a logic level signal to the SLEEP pin. The outputs of the devices are not valid (high-impedance mode) during sleep mode. The high-impedance output feature allows the connection of multiple A139x Hall effect devices to a single A-to-D converter input.

The quiescent output voltage of these devices is 50% nominal of the ratiometric supply reference voltage applied to the VREF pin of the device. The output voltage of the device is not ratiometric with respect to the SUPPLY pin.

Continued on the next page...

Functional Block Diagram



Description (continued)

Despite the low power consumption of the circuitry in the A139x, the features required to produce a highly-accurate linear Hall effect IC have not been compromised. Each BiCMOS monolithic circuit integrates a Hall element, improved temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, and proprietary dynamic

offset cancellation circuits. End of line, post-packaging, factory programming allows precise control of device sensitivity and offset.

These devices are available in a small 2.0 × 3.0 mm, 0.75 mm nominal height microleaded package (MLP/DFN). It is Pb (lead) free, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Sensitivity (mV/G, Typ.)	Packing
A1391SEHLT-T	1.25	7-in. reel, 3000 pieces/reel
A1392SEHLT-T	2.50	7-in. reel, 3000 pieces/reel
A1393SEHLT-T	5	7-in. reel, 3000 pieces/reel
A1395SEHLT-T	10	7-in. reel, 3000 pieces/reel

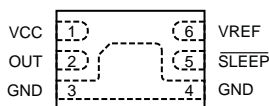


Absolute Maximum Ratings*

Supply Voltage	V_{CC}		8	V
Reverse-Supply Voltage	V_{RCC}		-0.1	V
Ratiometric Supply Reference Voltage	V_{REF}		7	V
Reverse-Ratiometric Supply Reference Voltage	V_{RREF}		-0.1	V
Logic Supply Voltage	V_{SLEEP}	($V_{CC} > 2.5 V$)	32	V
Reverse-Logic Supply Voltage	V_{RSLEEP}		-0.1	V
Output Voltage	V_{OUT}		$V_{CC} + 0.1$	V
Reverse-Output Voltage	V_{ROUT}		-0.1	V
Operating Ambient Temperature	T_A	Range S	-20 to 85	°C
Junction Temperature	$T_J(MAX)$		165	°C
Storage Temperature	T_{stg}		-65 to 170	°C

*All ratings with reference to ground

Pin-out Diagram



Terminal List Table

Pin	Name	Function
1	VCC	Supply
2	OUT	Output
3	GND	Ground
4	GND	Ground
5	\overline{SLEEP}	Toggle sleep mode
6	VREF	Supply for ratiometric reference

Device Characteristics Tables

ELECTRICAL CHARACTERISTICS valid through full operating ambient temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ. ¹	Max.	Units
Supply Voltage	V_{CC}		2.5	–	3.5	V
Nominal Supply Voltage	V_{CCN}		–	3.0	–	V
Supply Zener Clamp Voltage	V_{CCZ}	$I_{CC} = 7 \text{ mA}, T_A = 25^\circ\text{C}$	6	8.3	–	V
Ratiometric Reference Voltage ²	V_{REF}		2.5	–	V_{CC}	V
Ratiometric Reference Zener Clamp Voltage	V_{REFZ}	$I_{VREF} = 3 \text{ mA}, T_A = 25^\circ\text{C}$	6	8.3	–	V
$\overline{\text{SLEEP}}$ Input Voltage			–0.1	–	$V_{CC} + 0.5$	V
$\overline{\text{SLEEP}}$ Input Threshold	V_{INH}	For active mode	–	$0.45 \times V_{CC}$	–	V
	V_{INL}	For sleep mode	–	$0.20 \times V_{CC}$	–	V
Ratiometric Reference Input Resistance	R_{REF}	$V_{\overline{\text{SLEEP}}} > V_{INH}, V_{CC} = V_{CCN}, T_A = 25^\circ\text{C}$	250	–	–	k Ω
		$V_{\overline{\text{SLEEP}}} < V_{INL}, V_{CC} = V_{CCN}, T_A = 25^\circ\text{C}$	–	5	–	M Ω
Chopper Stabilization Chopping Frequency	f_C	$V_{CC} = V_{CCN}, T_A = 25^\circ\text{C}$	–	200	–	kHz
$\overline{\text{SLEEP}}$ Input Current	$I_{\overline{\text{SLEEP}}}$	$V_{\overline{\text{SLEEP}}} = 3 \text{ V}, V_{CC} = V_{CCN}$	–	1	–	μA
Supply Current ³	I_{CC}	$V_{\overline{\text{SLEEP}}} < V_{INL}, V_{CC} = V_{CCN}, T_A = 25^\circ\text{C}$	–	0.025	–	mA
		$V_{\overline{\text{SLEEP}}} > V_{INH}, V_{CC} = V_{CCN}, T_A = 25^\circ\text{C}$	–	3.2	–	mA
Quiescent Output Power Supply Rejection ⁴	PSR_{VOQ}	$f_{AC} < 1 \text{ kHz}$	–	–60	–	dB

¹Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as $T_A = 25^\circ\text{C}$. Performance may vary for individual units, within the specified maximum and minimum limits.

² Voltage applied to the VREF pin. Note that the V_{REF} voltage must be less than or equal to V_{CC} . Degradation in device accuracy will occur with applied voltages of less than 2.5 V.

³ If the VREF pin is tied to the VCC pin, the supply current would be $I_{CC} + V_{REF} / R_{REF}$

⁴ f_{AC} is any AC component frequency that exists on the supply line.

OUTPUT CHARACTERISTICS valid through full operating ambient temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ. ¹	Max.	Units	
Linear Output Voltage Range	V_{OUTH}	$V_{CC} = V_{CCN}, V_{REF} \leq V_{CC}$	–	$V_{REF} - 0.1$	–	V	
	V_{OUTL}	$V_{CC} = V_{CCN}, V_{REF} \leq V_{CC}$	–	0.1	–	V	
Maximum Voltage Applied to Output	V_{OUTMAX}	$V_{SLEEP} < V_{INL}$	–	–	$V_{CC} + 0.1$	V	
Sensitivity ²	Sens	A1391 $T_A = 25^\circ\text{C}, V_{CC} = V_{REF} = V_{CCN}$	–	1.25	–	mV/G	
		A1392 $T_A = 25^\circ\text{C}, V_{CC} = V_{REF} = V_{CCN}$	–	2.50	–	mV/G	
		A1393 $T_A = 25^\circ\text{C}, V_{CC} = V_{REF} = V_{CCN}$	–	5	–	mV/G	
		A1395 $T_A = 25^\circ\text{C}, V_{CC} = V_{REF} = V_{CCN}$	–	10	–	mV/G	
Quiescent Output	V_{OUTQ}	$T_A = 25^\circ\text{C}, B = 0\text{ G}$	–	$0.500 \times V_{REF}$	–	V	
Output Resistance ³	R_{OUT}	$f_{out} = 1\text{ kHz}, V_{SLEEP} > V_{INH}$, active mode	–	20	–	Ω	
		$f_{out} = 1\text{ kHz}, V_{SLEEP} < V_{INL}$, sleep mode	–	4M	–	Ω	
Output Load Resistance	R_L	Output to ground	15	–	–	k Ω	
Output Load Capacitance	C_L	Output to ground	–	–	10	nF	
Output Bandwidth	BW	–3 dB point, $V_{OUT} = 1\text{ V}_{pp}$ sinusoidal, $V_{CC} = V_{CCN}$	–	10	–	kHz	
Noise ^{4,5}	V_n	1391	$C_{bypass} = 0.1\ \mu\text{F}, BW_{externalLPF} = 2\text{ kHz}$	–	6	12	mV _{pp}
			$C_{bypass} = 0.1\ \mu\text{F}$, no load	–	–	20	mV _{pp}
		1392	$C_{bypass} = 0.1\ \mu\text{F}$, no load	–	–	40	mV _{pp}
			1393	$C_{bypass} = 0.1\ \mu\text{F}, BW_{externalLPF} = 2\text{ kHz}$	–	12	24
		$C_{bypass} = 0.1\ \mu\text{F}$, no load		–	–	40	mV _{pp}
1395	$C_{bypass} = 0.1\ \mu\text{F}$, no load	–	–	80	mV _{pp}		

¹Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as $T_A = 25^\circ\text{C}$. Performance may vary for individual units, within the specified maximum and minimum limits.

²For V_{REF} values other than $V_{REF} = V_{CCN}$, the sensitivity can be derived from the following equation: $K \times V_{REF}$, where $K = 0.416$ for the A1391, $K = 0.823$ for the A1392, $K = 1.664$ for the A1393, and $K = 3.328$ for the A1395.

³ f_{OUT} is the output signal frequency.

⁴Noise specification includes digital and analog noise.

⁵Values for $BW_{externalLPF}$ do not include any noise resulting from noise on the externally-supplied VREF voltage.

OUTPUT TIMING CHARACTERISTICS¹ T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ. ²	Max.	Units
Power-On Time ³	t _{PON}		–	40	60	μs
Power-Off Time ⁴	t _{POFF}		–	1	–	μs

¹See figure 1 for explicit timing delays.

²Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.

³Power-On Time is the elapsed time after the voltage on the SLEEP pin exceeds the active mode threshold voltage, V_{INH}, until the time the device output reaches 90% of its value.

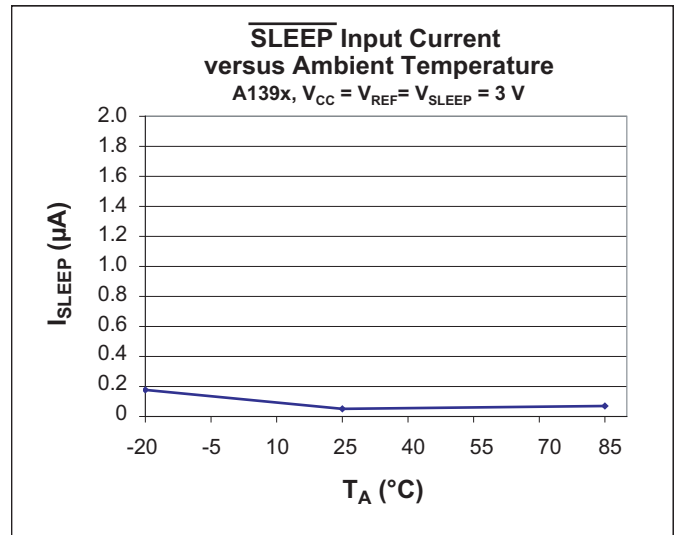
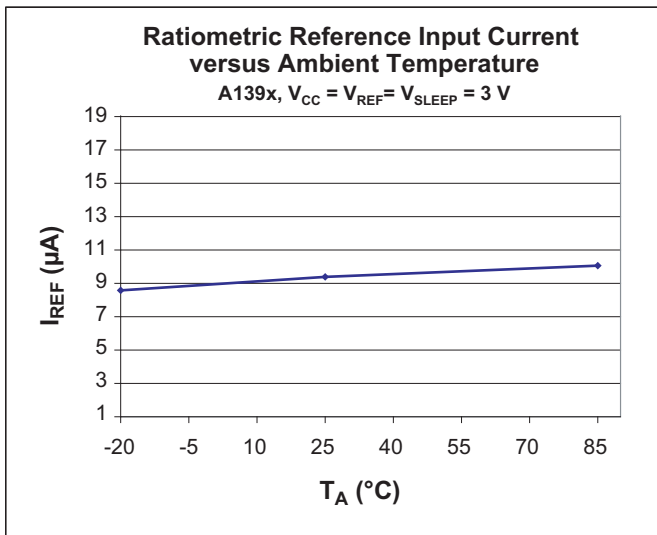
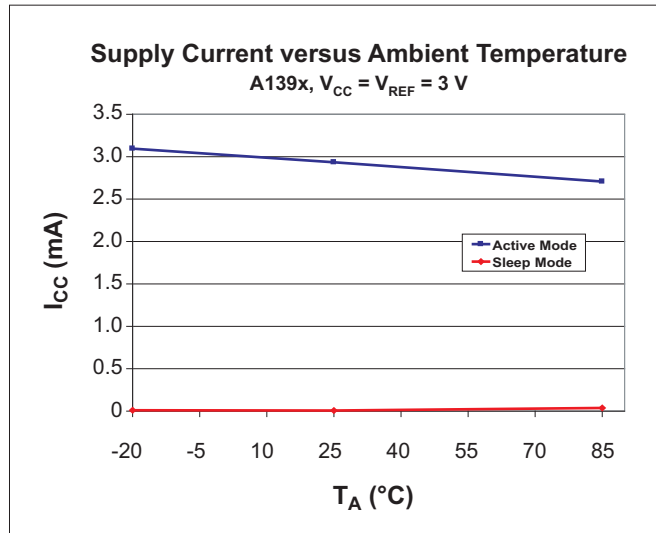
⁴Power-Off Time is the duration of time between when the signal on the $\overline{\text{SLEEP}}$ pin switches from HIGH to LOW and when I_{CC} drops to under 100 μA. During this time period, the output goes into the HIGH impedance state.

MAGNETIC CHARACTERISTICS T_A = 25°C

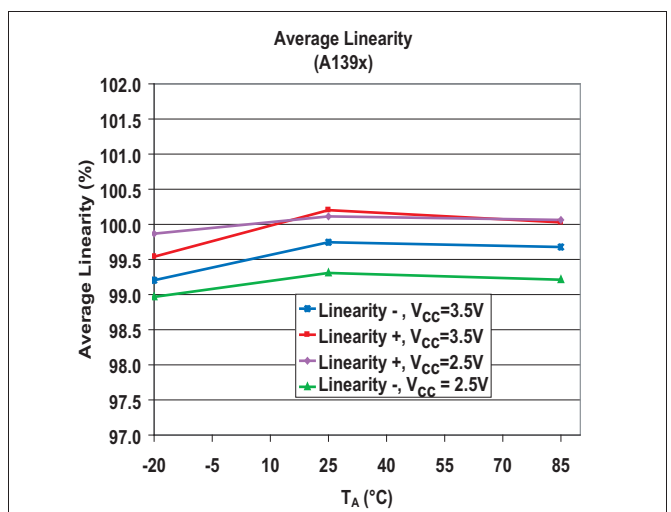
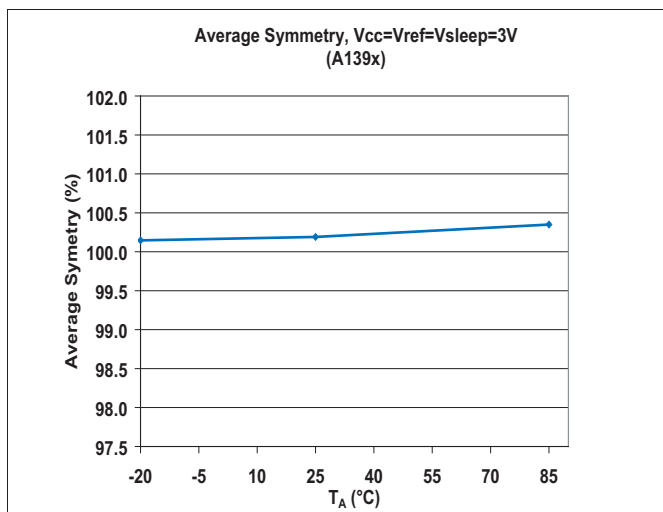
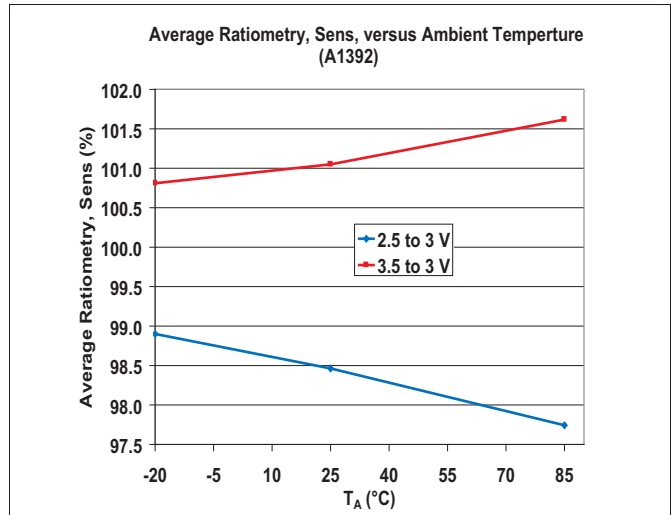
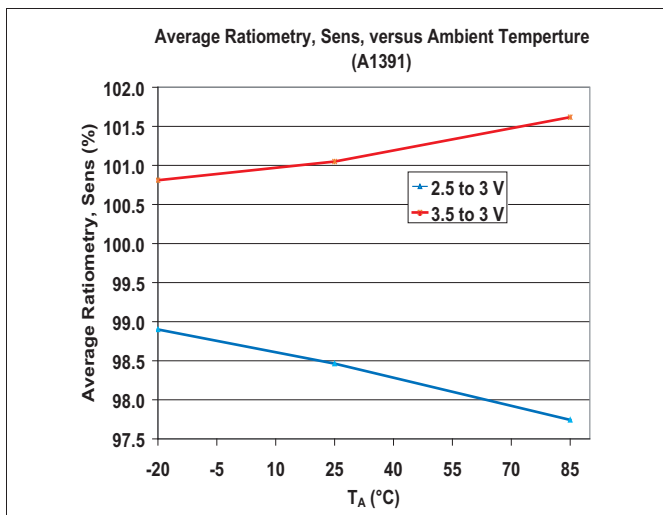
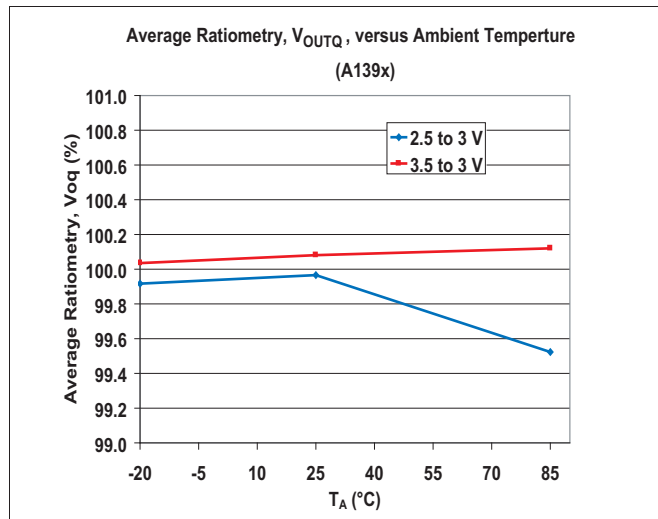
Characteristic	Symbol	Test Conditions	Min.	Typ.*	Max.	Units
Ratiometry	ΔV _{OUTQ(ΔV)}		–	100	–	%
Ratiometry	ΔSens _(ΔV)		–	100	–	%
Positive Linearity	Lin+		–	100	–	%
Negative Linearity	Lin–		–	100	–	%
Symmetry	Sym		–	100	–	%

*Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions, such as T_A = 25°C. Performance may vary for individual units, within the specified maximum and minimum limits.

Electrical Characteristic Data



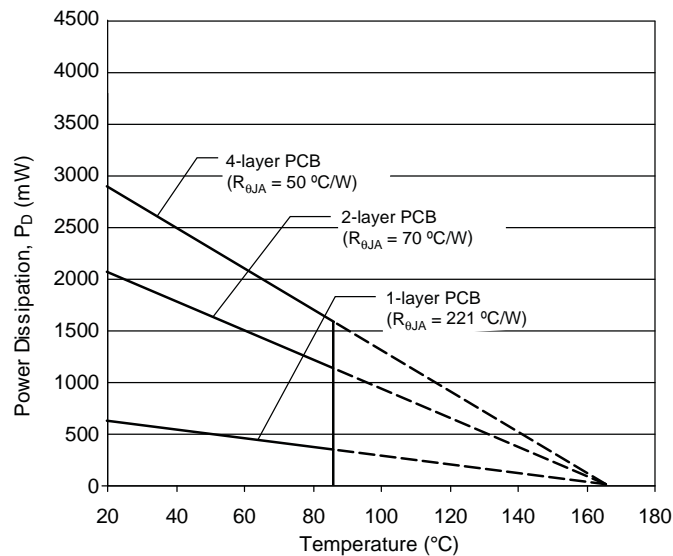
Magnetic Characteristic Data



THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	1-layer PCB with copper limited to solder pads	221	$^{\circ}\text{C}/\text{W}$
		2-layer PCB with 0.6 in. ² of copper area each side, connected by thermal vias	70	$^{\circ}\text{C}/\text{W}$
		4-layer PCB based on JEDEC standard	50	$^{\circ}\text{C}/\text{W}$

Power Dissipation versus Ambient Temperature



Characteristics Definitions

Ratiometric. The A139x devices feature ratiometric output. The quiescent voltage output and sensitivity are proportional to the ratiometric supply reference voltage. The percent ratiometric change in the quiescent voltage output is defined as:

$$\Delta V_{OUTQ(\Delta V)} = \frac{\Delta V_{OUTQ(V_{REF})} \mp \Delta V_{OUTQ(3V)}}{V_{REF} \mp 3V} \times 100\% \quad (1)$$

and the percent ratiometric change in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{\Delta Sens_{(V_{REF})} \mp \Delta Sens_{(3V)}}{V_{REF} \mp 3V} \times 100\% \quad (2)$$

Linearity and Symmetry. The on-chip output stage is designed to provide a linear output with maximum supply voltage of V_{CCN} . Although application of very high magnetic fields will not damage these devices, it will force the output into a non-linear region. Linearity in percent is measured and defined as

$$Lin+ = \frac{V_{OUT(+B)} - V_{OUTQ}}{2(V_{OUT(+B/2)} - V_{OUTQ})} \times 100\% \quad (3)$$

$$Lin- = \frac{V_{OUT(-B)} - V_{OUTQ}}{2(V_{OUT(-B/2)} - V_{OUTQ})} \times 100\% \quad (4)$$

and output symmetry as

$$Sym = \frac{V_{OUT(+B)} - V_{OUTQ}}{V_{OUTQ} - V_{OUT(-B)}} \times 100\% \quad (5)$$

Device Low-Power Functionality

A139x are low-power Hall effect sensor ICs that are perfect for power sensitive customer applications. The current consumption of these devices is typically 3.2 mA, while the device is in the active mode, and less than 25 μ A when the device is in the sleep mode. Toggling the logic level signal connected to the $\overline{\text{SLEEP}}$ pin drives the device into either the active mode or the sleep mode. A logic low sleep signal drives the device into the sleep mode, while a logic high sleep signal drives the device into the active mode.

In the case in which the VREF pin is powered before the VCC pin, the device will not operate within the specified limits until the supply voltage is equal to the reference voltage. When the device is switched from the sleep mode to the active mode, a time defined by t_{PON} must elapse before the output of the device is

valid. The device output transitions into the high impedance state approximately t_{POFF} seconds after a logic low signal is applied to the $\overline{\text{SLEEP}}$ pin (see figure 1).

If possible, it is recommended to power-up the device in the sleep mode. However, if the application requires that the device be powered on in the active mode, then a 10 k Ω resistor in series with the $\overline{\text{SLEEP}}$ pin is recommended. This resistor will limit the current that flows into the $\overline{\text{SLEEP}}$ pin if certain semiconductor junctions become forward biased before the ramp up of the voltage on the VCC pin. Note that this current limiting resistor is not required if the user connects the $\overline{\text{SLEEP}}$ pin directly to the VCC pin. The same precautions are advised if the device supply is powered-off while power is still applied to the $\overline{\text{SLEEP}}$ pin.

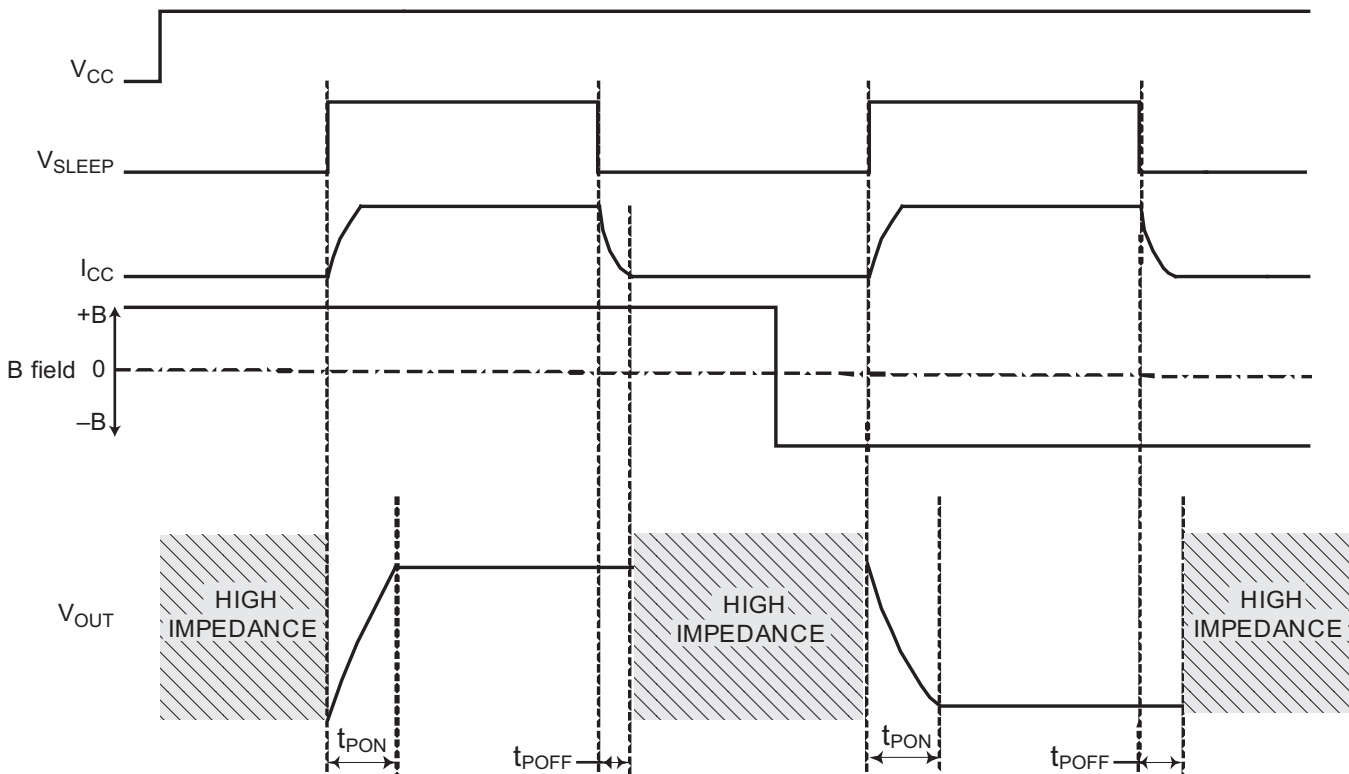


Figure 1. A139x Timing Diagram

Device Supply Ratiometry Application Circuit

Figures 2 and 3 present applications where the VCC pin is connected together with the VREF pin of the A139x. Both of these pins are connected to the battery, Vbat2. In this case, the device output will be ratiometric with respect to the battery voltage.

The only difference between these two applications is that the $\overline{\text{SLEEP}}$ pin in figure 2 is connected to the Vbat2 potential, so the device is always in the active mode. In figure 3, the $\overline{\text{SLEEP}}$ pin is toggled by the microprocessor; therefore, the device is selectively and periodically toggled between active mode and sleep mode.

In both figures, the device output is connected to the input of an A-to-D converter. In this configuration, the converter reference voltage is Vbat1.

It is **strongly recommended** that an external bypass capacitor be connected, in close proximity to the A139x device, between the VCC and GND pins of the device to reduce both external noise and noise generated by the chopper-stabilization circuits inside of the A139x.

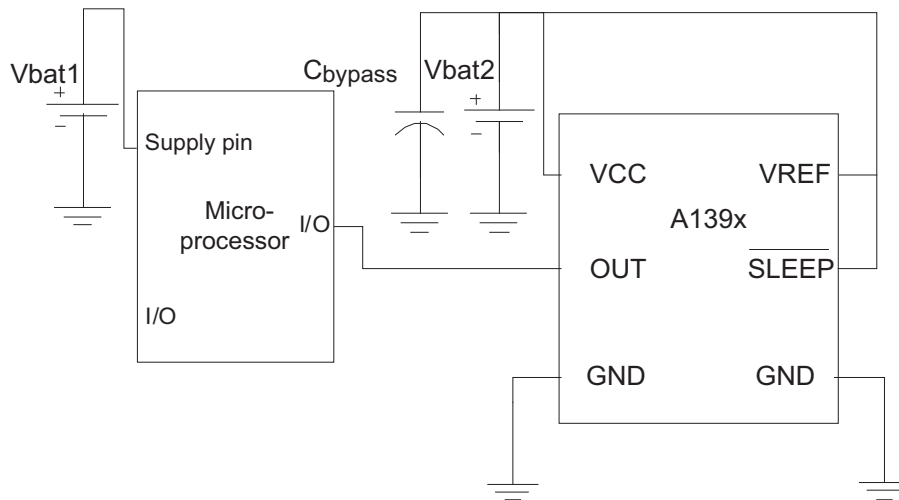


Figure 2. Application circuit showing sleep mode disabled and output ratiometric to the A139x supply.

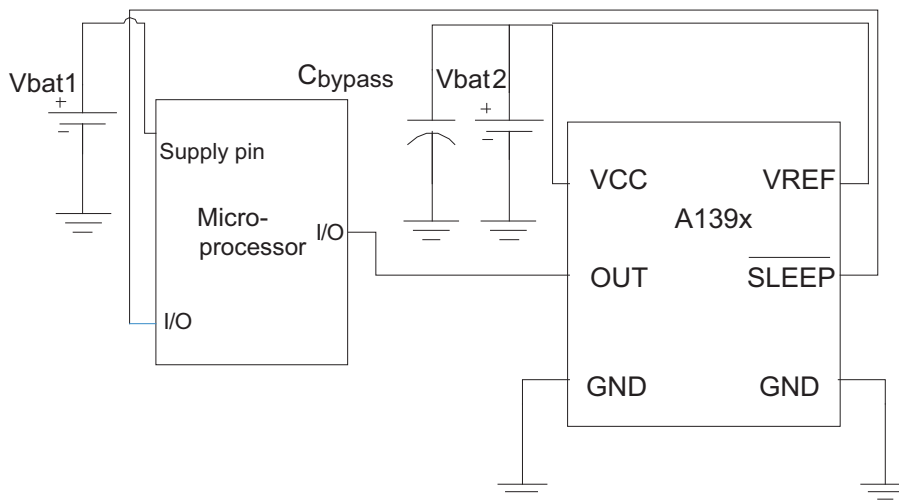


Figure 3. Application circuit showing microprocessor-controlled sleep mode and output ratiometric to the A139x supply.

Application Circuit with User-Configurable Ratiometry

In figures 4 and 5, the microprocessor supply voltage determines the ratiometric performance of the A139x output signal. As in the circuits shown in figures 2 and 3, the device is powered by the Vbat2 supply, but in this case, ratiometry is determined by the microprocessor supply, Vbat1.

The $\overline{\text{SLEEP}}$ pin is triggered by the output logic signal from the microprocessor in figure 5, while in figure 4, the $\overline{\text{SLEEP}}$ pin is connected to the device power supply pin. Therefore, the device as configured in figure 4 is constantly in active mode, while the device as configured in figure 5 can be periodically toggled

between the active and sleep modes.

The capacitor C_{filter} is optional, and can be used to prevent possible noise transients from the microprocessor supply reaching the device reference pin, VREF.

It is **strongly recommended** that an external bypass capacitor be connected, in close proximity to the A139x device, between the VCC and GND pins of the device to reduce both external noise and noise generated by the chopper-stabilization circuits inside of the A139x.

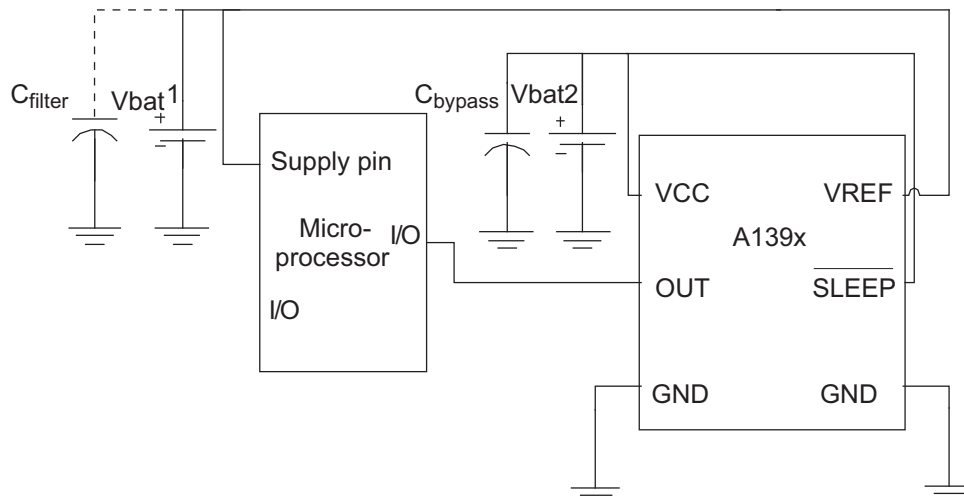


Figure 4. Application circuit showing ratiometry of V_{REF} . Sleep mode is disabled and the VREF pin is tied to the microprocessor supply.

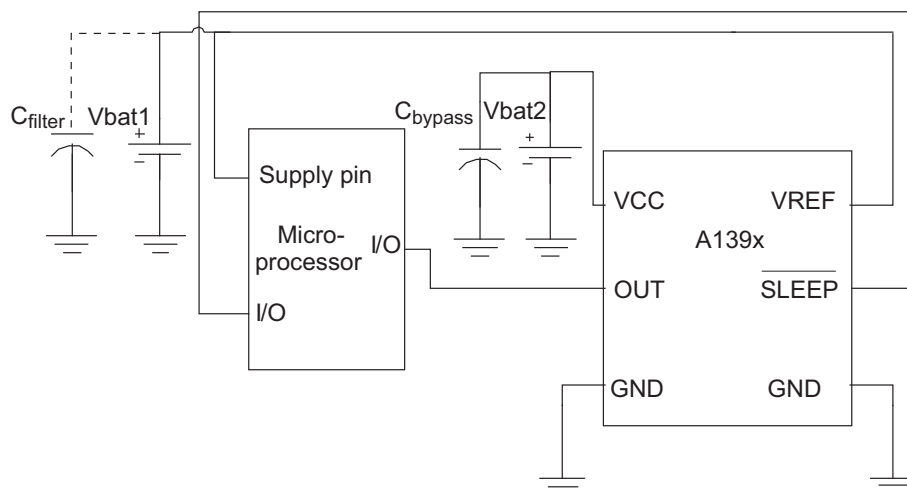


Figure 5. Application circuit showing device reference pin, VREF, tied to microprocessor supply. The device sleep mode also is controlled by the microprocessor.

Summary of Single-Device Application Circuits

Application Circuit	Device Pin Connections		Device Output
	VREF pin (Ratiometric Reference Supply)	$\overline{\text{SLEEP}}$ pin	
	Connected to A139x device supply, VCC	Connected to A139x device supply, VCC	Ratiometric to device supply (VCC), and always valid
	Connected to A139x device supply, VCC	Controlled by microprocessor	Ratiometric to device supply (VCC), and controlled by the microprocessor
	Connected to microprocessor supply	Connected to A139x device supply, VCC	Ratiometric to micro-processor supply, and always valid
	Connected to microprocessor supply	Controlled by microprocessor	Ratiometric to micro-processor supply, and controlled by the microprocessor

Application Circuit with Multiple Hall Devices and a Single A-to-D Converter

Multiple A139x devices can be connected to a single microprocessor or A-to-D converter input. In this case, a single device is periodically triggered and put into active mode by the microprocessor. While one A139x device is in active mode, all of the other A139x devices must remain in sleep mode. While these devices are in sleep mode, their outputs are in a high-impedance state. In this circuit configuration, the microprocessor reads the output of one device at a time,

according to microprocessor input to the $\overline{\text{SLEEP}}$ pins.

When multiple device outputs are connected to the same microprocessor input, pulse timing from the microprocessor (for example, lines A1 through A4 in figure 6) must be configured to prevent more than one device from being in the awake mode at any given time of the application. A device output structure can be damaged when its output voltage is forced above the device supply voltage by more than 0.1 V.

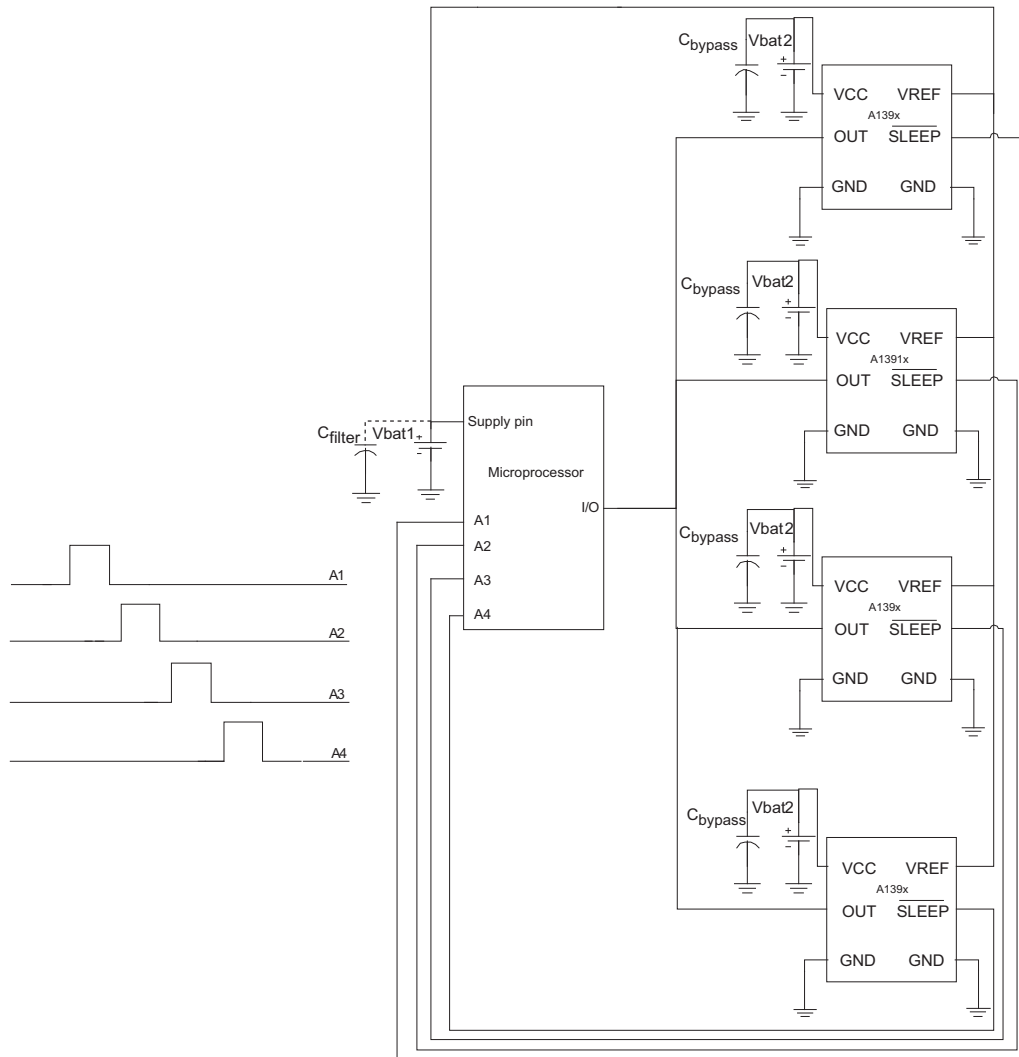
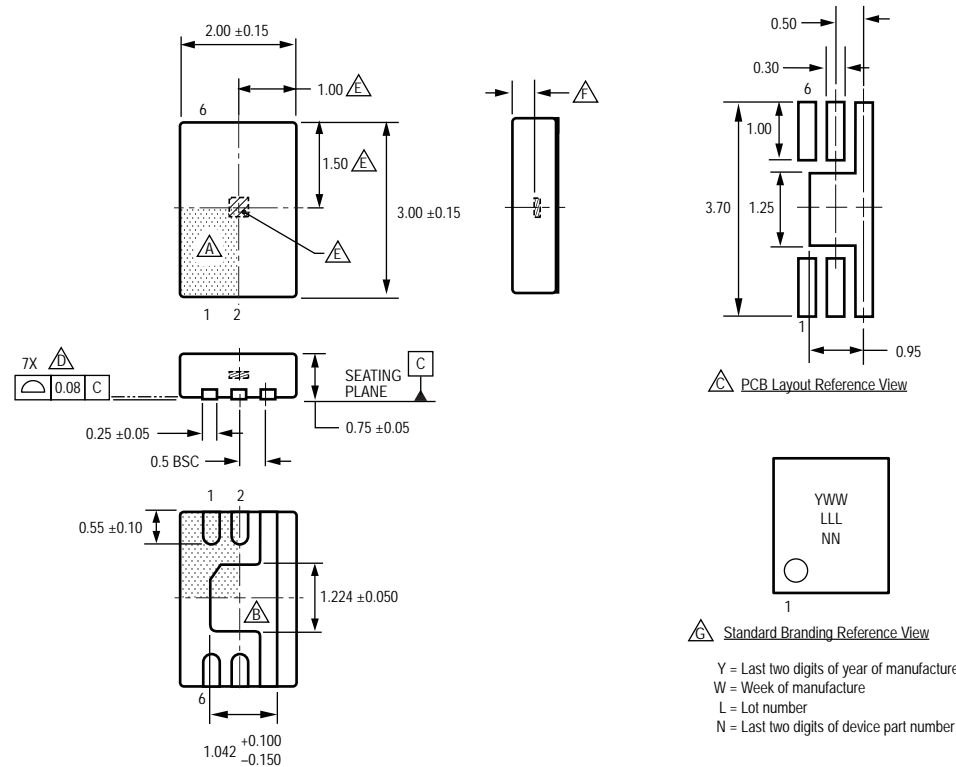


Figure 6. Application circuit showing multiple A139x devices, controlled by a single microprocessor.

Package EH, 6-pin MLP/DFN



For Reference Only, not for tooling use (reference DWG-2861;
reference JEDEC MO-229WCED, Type 1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

- Terminal #1 mark area
- Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- Reference land pattern layout:
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- Coplanarity includes exposed thermal pad and terminals
- Hall Element (not to scale); U.S. customary dimensions controlling
- Active Area Depth, 0.32 mm NOM
- Branding scale and appearance at supplier discretion

Copyright ©2005-2010, Allegro MicroSystems, Inc.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

www.allegromicro.com

