

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND.

V_{DD}, V_S	7 V
P_{GND}	± 0.3 V
Linear Inputs	-0.3 V to $V_{DD} + 0.3$ V
Logic Inputs	-0.3 V to $V_{DD} + 0.3$ V
Peak Output Drive Current	350 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	150°C

Power Dissipation (Package)^a

16-Pin TSSOP (Q Suffix)^{a, b} 925 mW

Thermal Impedance (Θ_{JA})^a

16-Pin TSSOP 135°C/W

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.4 mW/°C above 25°C.

* Exposure to Absolute Maximum rating conditions for extended periods may affect device reliability. Stresses above Absolute Maximum rating may cause permanent damage. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Otherwise Specified ^a $2.7 \text{ V} \leq V_{DD}, V_S \leq 6.0 \text{ V}, \text{GND} = P_{GND}$	Limits B Suffix -25 to 85°C			Unit
			Min ^b	Typ	Max ^b	
Reference						
Output Voltage	V_{REF}	$I_{REF} = -10 \mu\text{A}$ $T_A = 25^\circ\text{C}$	1.455		1.545	V
			1.477	1.50	1.523	
Oscillator						
Maximum Frequency ^c	f_{MAX}	$V_{DD} = 5 \text{ V}, C_{OSC} = 47 \text{ pF}, R_{OSC} = 5.0 \text{ k}\Omega$	2.0			MHz
Oscillator Frequency Accuracy		$V_{DD} = 3.0 \text{ V}, f_{OSC} = 1 \text{ MHz (nominal)}$ $C_{OSC} = 100 \text{ pF}, R_{OSC} = 7.0 \text{ k}\Omega, T_A = 25^\circ\text{C}$	-15		15	%
R_{OSC} Peak Voltage	V_{ROSC}			1.0		V
Voltage Stability ^c	$\Delta f/f$	$4 \text{ V} \leq V_{DD} \leq 6 \text{ V}, \text{Ref to } 5 \text{ V}, T_A = 25^\circ\text{C}$	-8		8	%
Temperature Stability ^c			Referenced to 25°C		± 5	
Error Amplifier ($C_{OSC} = \text{GND}$, OSC DISABLED)						
Input Bias Current	I_B	$V_{NI} = V_{REF}, V_{FB} = 1.0 \text{ V}$	-1.0		1.0	μA
Open Loop Voltage Gain	A_{VOL}		47	55		dB
Offset Voltage	V_{OS}	$V_{NI} = V_{REF}$	-15	0	15	mV
Unity Gain Bandwidth ^c	BW			10		MHz
Output Current	I_{OUT}	Source ($V_{FB} = 1 \text{ V}, NI = V_{REF}$)		-2.0	-1.0	mA
		Sink ($V_{FB} = 2 \text{ V}, NI = V_{REF}$)	0.4	0.8		
Power Supply Rejection ^c	PSRR	$4 \text{ V} < V_{DD} < 6 \text{ V}$		60		dB
UVLO_{SET} Voltage Monitor						
Under Voltage Lockout	V_{UVLOHL}	UVLO _{SET} High to Low	0.85	1.0	1.15	V
	V_{UVLOLH}	UVLO _{SET} Low to High		1.2		
Hysteresis	V_{HYS}	$V_{UVLOLH} - V_{UVLOHL}$		200		mV
UVLO Input Current	$I_{UVLO(SET)}$	$V_{UVLO} = 0 \text{ to } V_{DD}$	-100		100	nA

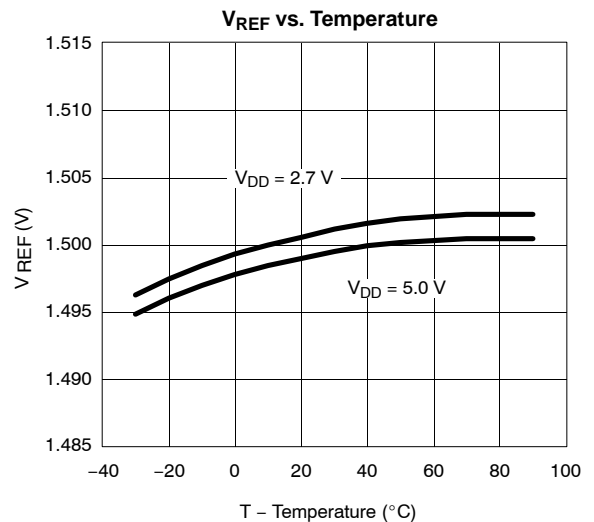
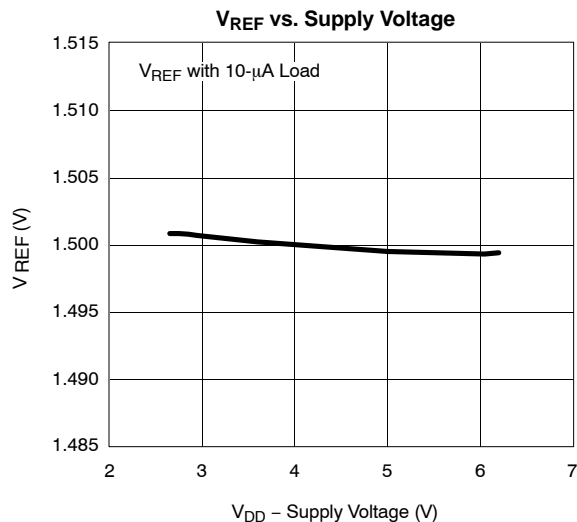


SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified ^a 2.7 V ≤ V _{DD} , V _S ≤ 6.0 V, GND = P _{GND}		Limits B Suffix -25 to 85°C			Unit	
				Min ^b	Typ	Max ^b		
Output Drive (D_R and D_S)								
Output High Voltage	V _{OH}	V _{DD} = 2.7 V V _S = 5.3 V	I _{OUT} = -10 mA	5.15	5.2		V	
Output Low Voltage	V _{OL}		I _{OUT} = 10 mA		0.06	0.15		
Peak Source Output Current	I _{SOURCE}	V _{DD} = 2.7 V, V _S = 5.3 V			-300	-250	mA	
Peak Sink Output Current	I _{SINK}			250	300			
Break-Before-Make	t _{BBM}	V _{DD} = 6.0 V			40		ns	
Logic								
ENABLE Delay to Output	t _{dEN}	ENABLE Rising to OUTPUT, V _{DD} = 6.0 V			1.4		μs	
ENABLE Logic Low	V _{ENL}					0.2 V _{DD}	V	
ENABLE Logic High	V _{ENH}			0.8 V _{DD}				
ENABLE Input Current	I _{EN}	ENABLE = 0 to V _{DD}		-1.0		1.0	μA	
Duty Cycle								
Maximum Duty Cycle	CYCLE _{MAX}	V _{DD} = 6.0 V			80	95	%	
D _{MAX} /SS Input Current	I _{DMAX}	D _{MAX} = 0 to V _{DD}		-100		100	nA	
Supply								
Supply Current—Normal Mode	I _{DD}	f _{OSC} = 1 MHz R _{OSC} = 7.0 kΩ		V _{DD} = 2.7 V		1.1	1.5	mA
				V _{DD} = 4.5 V		1.6	2.3	
Supply Current—Standby Mode		ENABLE = Low				250	330	μA

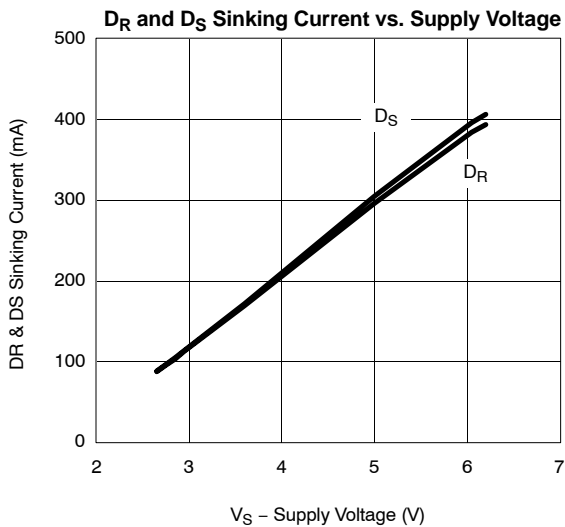
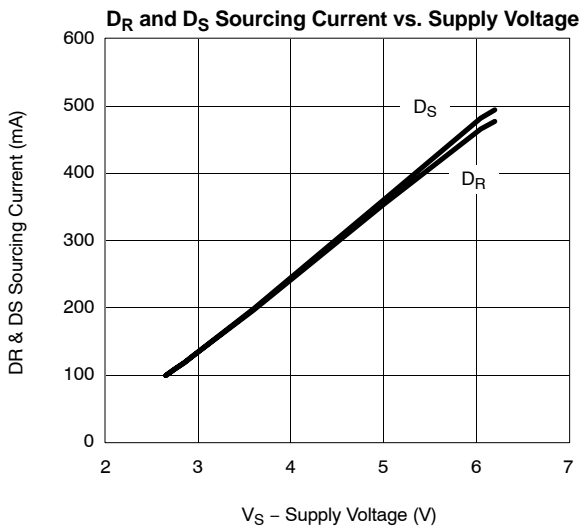
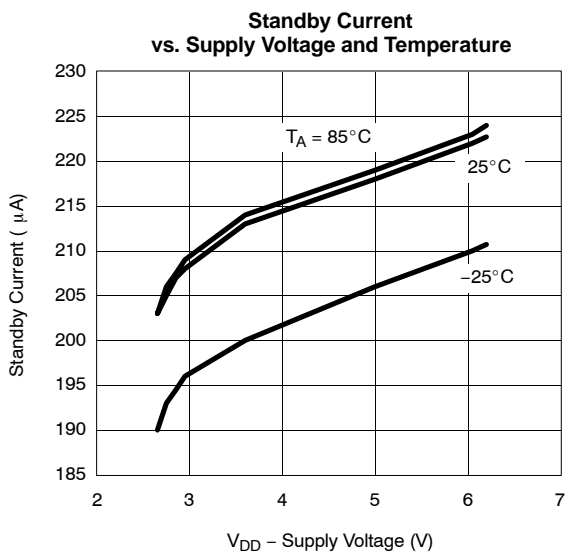
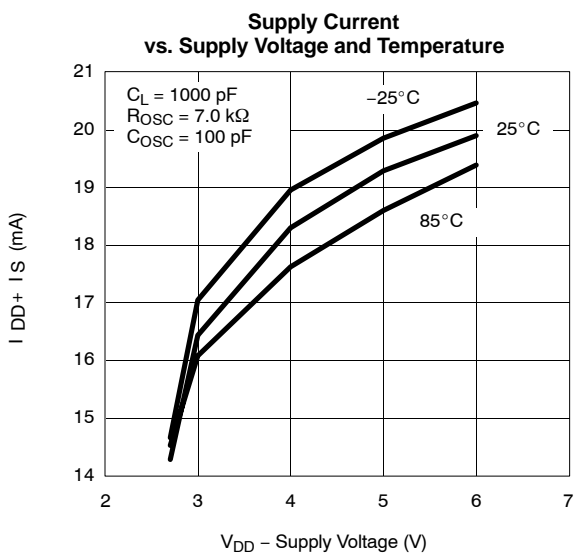
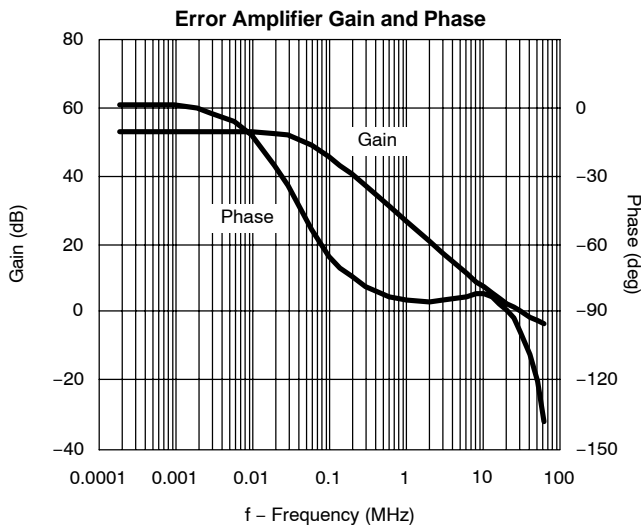
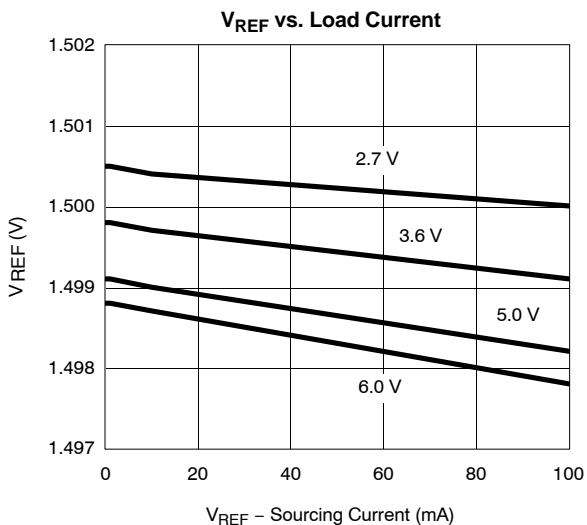
Notes

- a. C_{STRAY} < 5 pF on C_{OSC}. After Start-Up, V_{DD} of ≥ 3 V.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production testing.

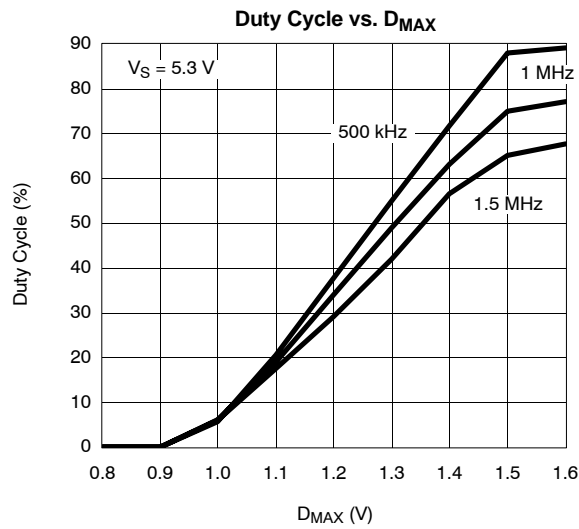
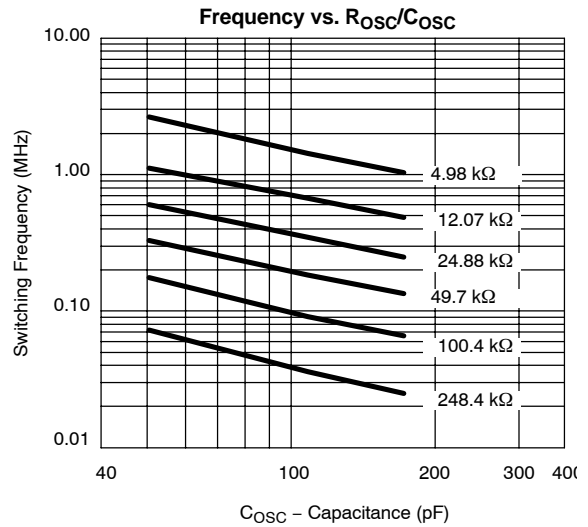
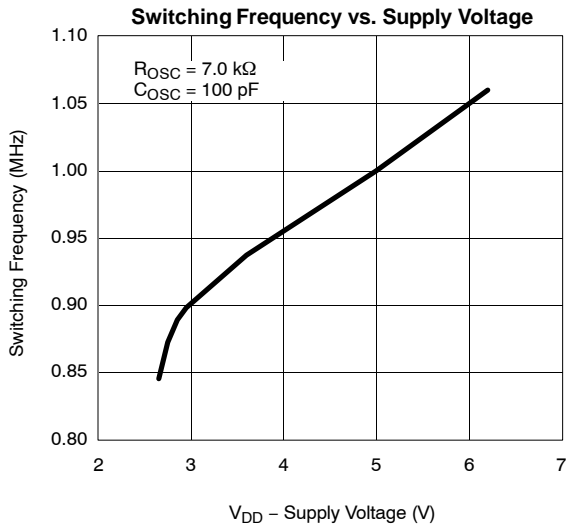
TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)

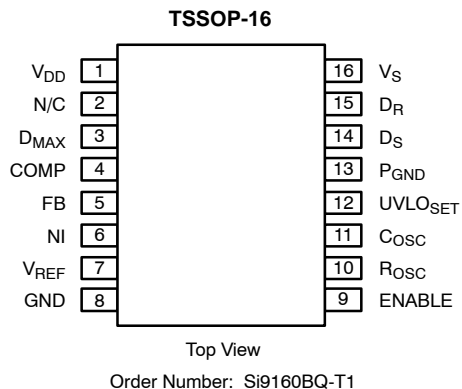


TYPICAL CHARACTERISTICS (25 °C UNLESS OTHERWISE NOTED)



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PIN CONFIGURATION AND ORDERING INFORMATION

PIN DESCRIPTION
Pin 1: V_{DD}

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1 μ F (minimum) is recommended.

Pin 2: N/C

There is no internal connection to this pin.

Pin 3: D_{MAX}

Used to set the maximum duty cycle.

Pin 4: COMP

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

Pin 5: FB

The inverting input of the error amplifier. An external resistor divider is connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

Pin 6: NI

The non-inverting input of the error amplifier. In normal operation it is externally connected to V_{REF} or an external reference.

Pin 7: V_{REF}

This pin supplies a 1.5-V reference.

Pin 8: GND (Ground)
Pin 9: ENABLE

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode, normal

ORDERING INFORMATION		
Part Number	Temperature Range	Package
Si9160BQ-T1	-25 to 85°C	TSSOP-16
Si9160BQ-T1-E3		

operation is disabled, supply current is reduced, the oscillator stops, and D_S goes low while D_R goes high.

Pin 10: R_{osc}

A resistor connected from this pin to ground sets the oscillator's capacitor (C_{OSC}) charge and discharge current. See the oscillator section of the description of operation.

Pin 11: C_{osc}

An external capacitor is connected to this pin to set the oscillator frequency.

$$f_{osc} \approx \frac{0.70}{R_{osc} \times C_{osc}} \quad (\text{at } V_{DD} = 5.0 \text{ V})$$

Pin 12: UVLO_{SET}

This pin will place the chip in the standby mode if the UVLO_{SET} voltage drops below 1.2 V. Once the UVLO_{SET} voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

Pin 13: P_{GND}

The negative return for the V_S supply.

Pin 14: D_S

This CMOS push-pull output pin drives the external n-channel MOSFET. This pin will be low in the standby mode. A break-before-make function between D_S and D_R is built-in.

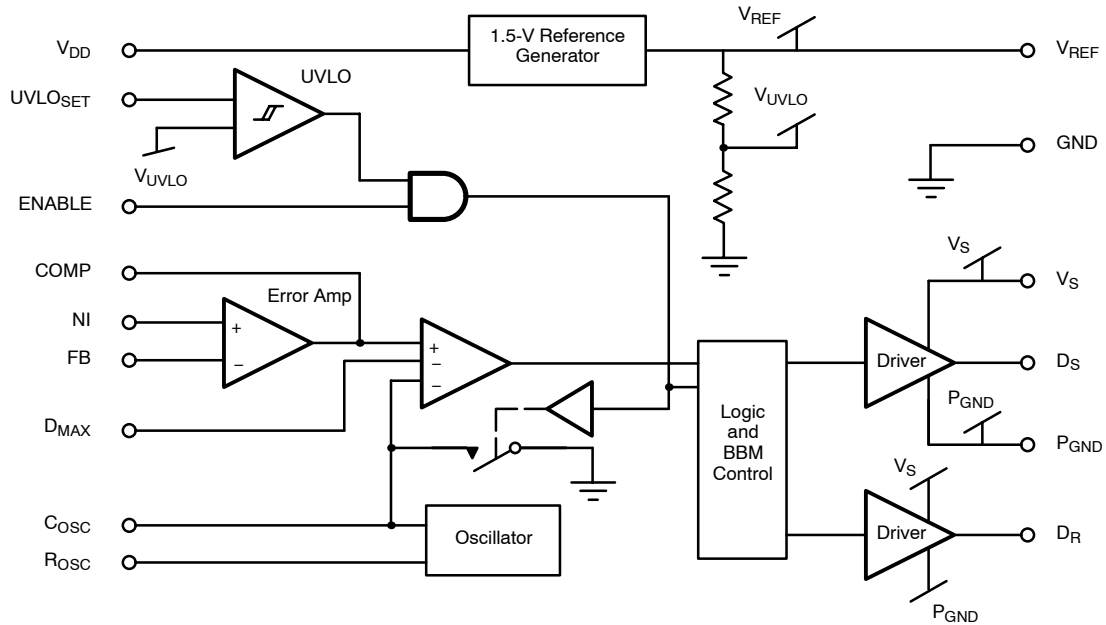
Pin 15: D_R

This CMOS push-pull output pin drives the external p-channel MOSFET. This pin will be high in the standby mode. A break-before-make function between the D_S and D_R is built-in.

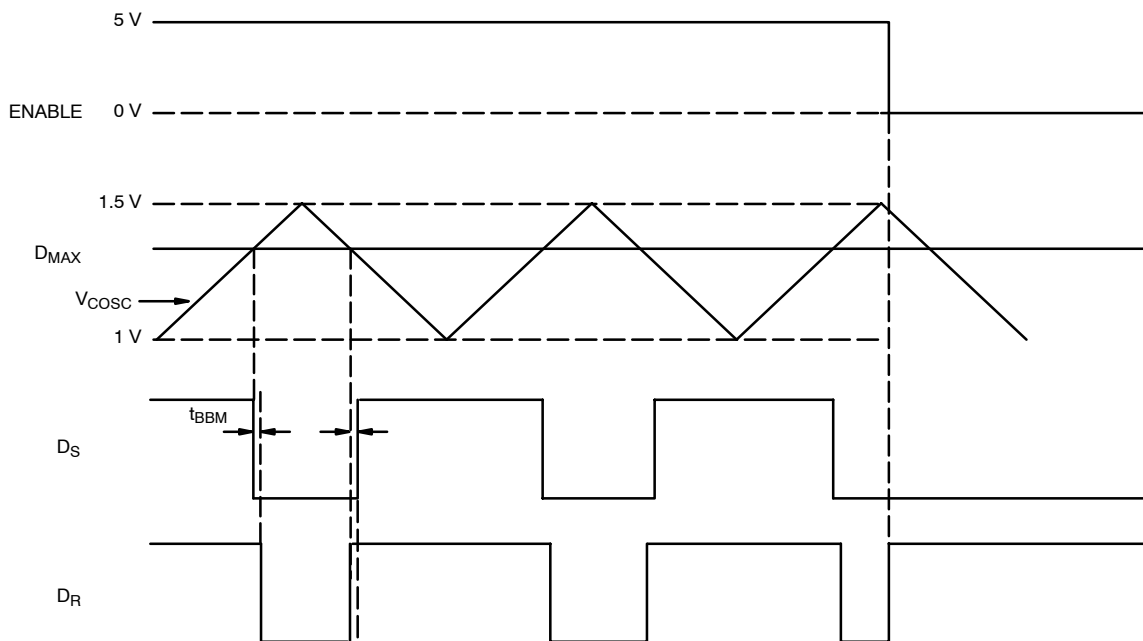
Pin 16: V_S

The positive terminal of the power supply which powers the CMOS output drivers. A bypass capacitor is required.

FUNCTIONAL BLOCK DIAGRAM



TIMING WAVEFORMS



Another benefit of powering from the output voltage is it provides minimum load on the converter. This prevents the converter from skipping frequency pulses typically referred to as Burst or Pulse-Skipping modes. Pulse skipping mode could be dangerous, especially if it generates noise in RF, IF, or signal processing frequency bands.

Enable and Under Voltage Shutdown

The Si9160 is designed with programmable under-voltage lockout and enable features. These features give designers flexibility to customize the converter design. The under-voltage lockout threshold is 1.2 V. With a simple resistor divider from V_{DD} , Si9160 can be programmed to turn-on at any V_{DD} voltage. The ENABLE pin, a TTL logic compatible input, allows remote shutdown as needed.

Gate Drive and MOSFETs

The gate drive section is designed to drive the high-side p-channel switch and low-side n-channel switch. The internal 40 ns break-before-make (BBM) timing prevents both MOSFETs from turning-on simultaneously. The BBM circuit monitors both drive voltages, once the gate-to-source voltage drops below 2.5 V, the other gate drive is delayed 40-ns before it is allowed to drive the external MOSFET (see Figure 2 for timing diagram). This smart gate drive control provides additional assurance that shoot-through current will not occur.

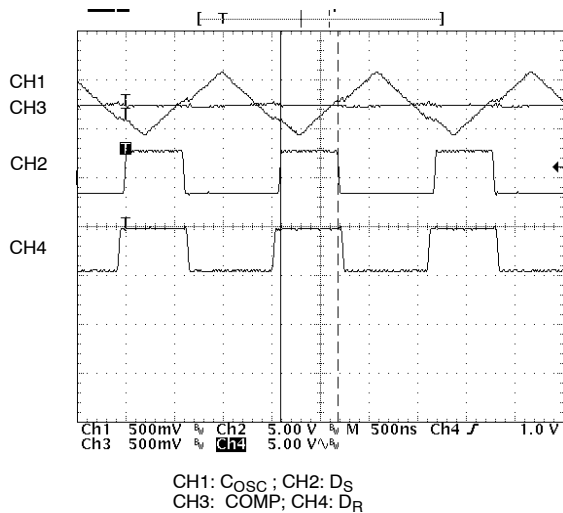
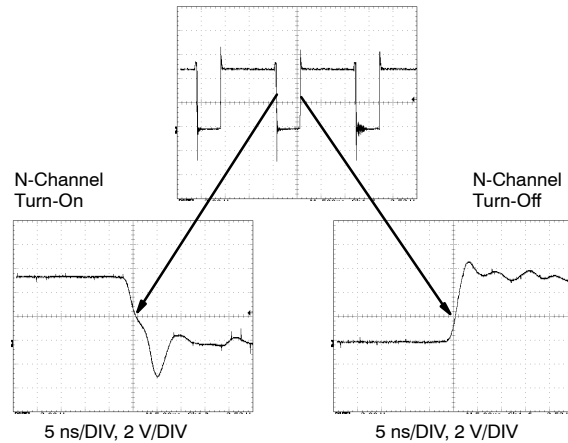


FIGURE 2. Gate Drive Timing Diagrams

The MOSFET used is the Si6801, an n- and p-channel in a single package TSSOP-8. The Si6801 is optimized to have very low gate charge and gate resistance. This results in a great reduction in gate switching power losses. The average time to switch on and off a MOSFET in a conventional structure is about 20 ns. The Si6801 will switch on and off in < 5 ns, see Figure 3.



Note the Speed

These MOSFETs have switching speeds of <5 ns. This high speed is due to the fast, high current output drive of the Si9160 and the optimized gate charge of the Si6801.

FIGURE 3. Gate Switching Times

Stability Components

A voltage mode boost converter is normally stabilized with simple lag compensation due to the additional 90° phase lag introduced by the additional right hand plane zero, as well as having a duty factor dependent resonant frequency for the output filter. The stability components shown in Figure 1 have been chosen to ensure stability under all battery conditions while maintaining maximum transient response. To do this we have used a 2-pole-zero pair configuration (type 3 amplifier configuration). Figure 4 shows the bode plot for the above circuit, maintaining > 50° phase margin over the entire battery voltage range.

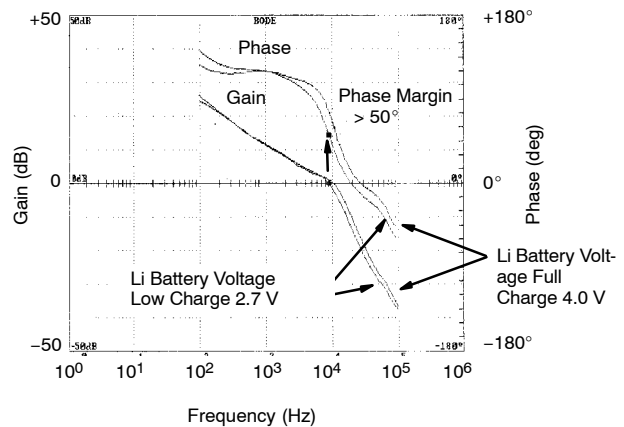


FIGURE 4. Stability, with 1-cell Li battery input, 5 V @ 600-mA output.

Energy Storage Components

The input and output ripple voltage is determined by the switching frequency, and the inductor and capacitor values. The higher the frequency, inductance, or capacitance values, the lower the ripple. The efficiency of the converter is also improved with higher inductance by reducing the conduction loss in the switch, synchronous rectifier, and the inductor itself. In the past, Tantalum was the preferred material for the input and output capacitors. Now, with 2-MHz switching frequencies, Tantalum capacitors are being replaced with smaller surface mount ceramic capacitors. Ceramic capacitors have almost no equivalent series resistance (ESR). Tantalum capacitors have at least 0.1-Ω ESR. By reducing ESR, converter efficiency is improved while decreasing the input and output ripple voltage. With ceramic capacitors, output ripple voltage is a function of capacitance only. The equation for determining output capacitance is stated below.

$$C = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot \Delta V_{RIPPLE} \cdot f}$$

I_{OUT} = output dc load current
 V_{OUT} = output voltage
 V_{IN} = input voltage
 ΔV_{RIPPLE} = desired output ripple voltage
 f = switching frequency

The inductance value for the converter is a function of the desired ripple voltage and efficiency as stated below. In order to keep the ripple small and improve efficiency, the inductance needs to be large enough to maintain continuous current mode. Continuous current mode has lower RMS current compared to discontinuous current mode since the peak current is lower. This lowers the conduction loss and improves

efficiency. The equation that shows the critical inductance which separates continuous and discontinuous current mode at any given output current is stated below. This equation is also plotted in Figure 5 as a function of input voltage.

$$L = \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{2 \cdot V_{OUT}^2 \cdot I_{OUT} \cdot f}$$

η = efficiency

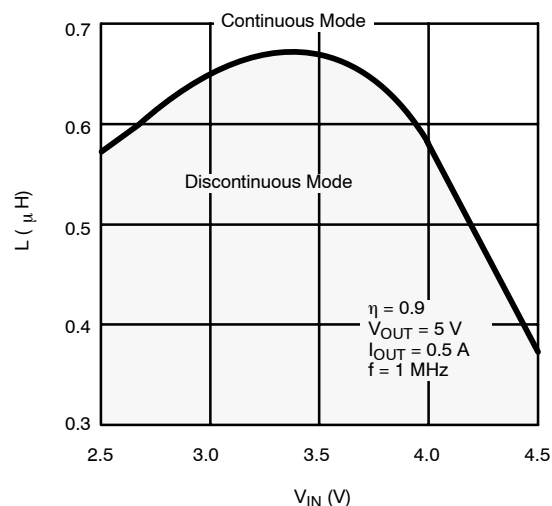


FIGURE 5. Continuous and Discontinuous Inductance Curve

RESULTS SECTION

The following section shows the actual results obtained with the circuit diagram shown in Figure 1.

Efficiency

The Figure 6 shows the efficiency of the above design at various constant switching frequencies. The frequencies were generated using a 3-V square wave of the desired frequency to the sync input to the circuit. The input voltage to the circuit is 3.6-V dc.

Output Noise

The noise generated by a dc-dc converter is always an issue within the mobile phone. The Si9160 offers two benefits.

The noise spectrum is a constant, i.e. no random noise or random harmonic generation.

The switching fundamental can be synchronized to a known frequency, e.g. 812.5 kHz which is $1/16$ -th of the GSM/DCS system clock, 1.23 MHz which is the channel spacing frequency for CDMA, etc.

Figures 7 through 9 show the output noise and output spectrum analysis.

Output Noise Spectrum

Note there is no random noise, only switching frequency harmonics. This is very good news for the RF stages, where an unknown, or random noise spectrum will cause problems.

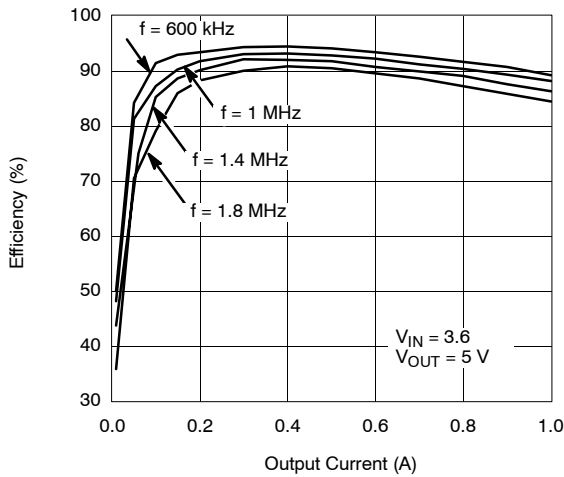
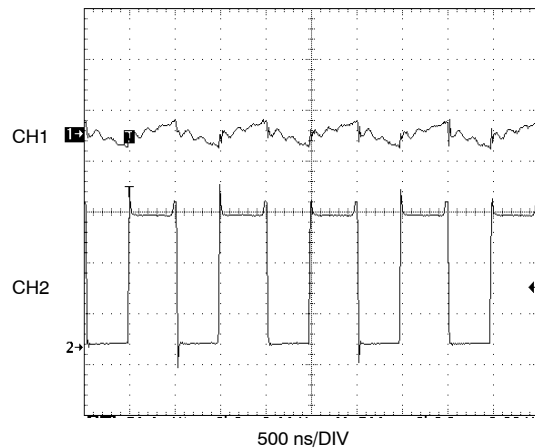


FIGURE 6. Efficiency of Si9160 and Si6801 Boost converter at various fixed frequencies



CH1: Output Ripple (50 mV/DIV)
CH2: P- and N-Channel Drain Voltage (2 V/DIV)

FIGURE 7. Output noise of the Si9160 demo board

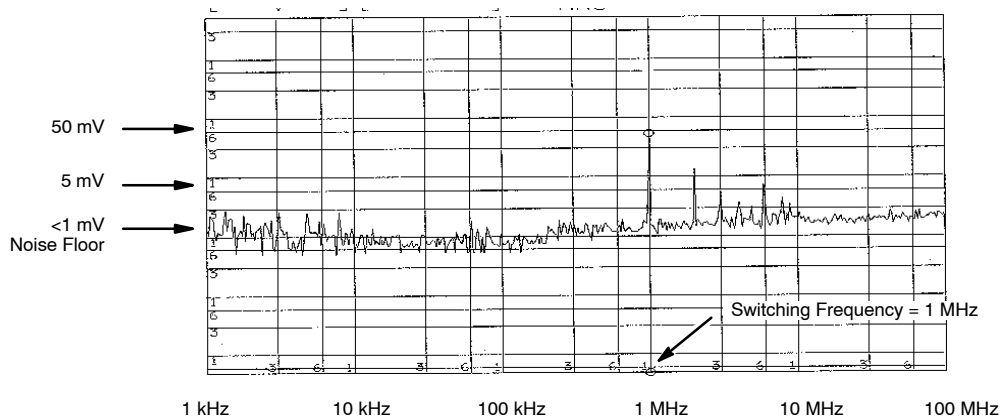


FIGURE 8. Spectrum response for the Si9160 demo board output voltage

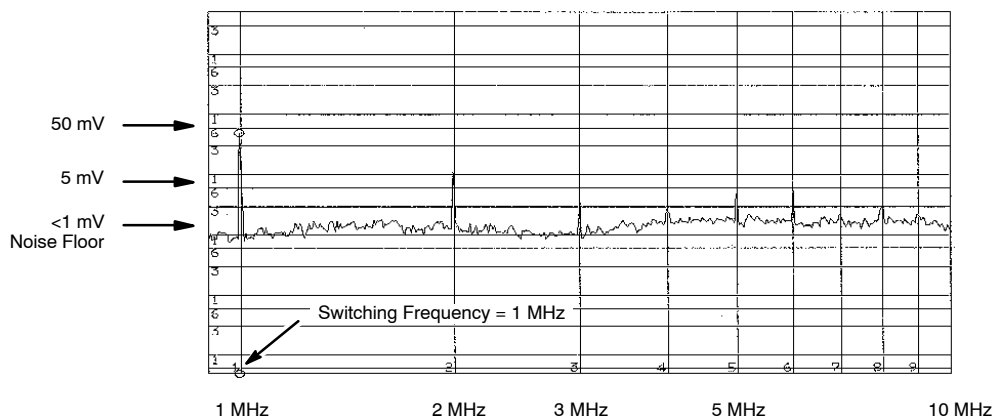


FIGURE 9. Higher resolution of noise spectrum

Conclusion

Switching at high, known frequencies results in a smaller footprint while maintaining high efficiency. Efficiencies at high switching frequencies can be improved by using Si6801

optimized low gate charge and low gate resistance MOSFET. Additionally, synchronization to an external high frequency clock eliminates or greatly reduces any radio interference concerns and pushes harmonics out beyond signal processing frequencies.



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