

Structure Silicon monolithic integrated circuit
 Product USB high side switch IC
 Type **BD2056AFJ**
 Features Dual-channel Nch Power MOSFET
 Low on-state resistance (Typ = 100mΩ)
 250mA minimum continuous load current
 Over Current Detection (OCD), Under Voltage Lockout (UVLO)
 Thermal shutdown (TSD), Soft start circuit
 Control Logic : Active High

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V _{IN}	-0.3 ~ 6.0	V
Enable voltage	V _{EN}	-0.3 ~ 6.0	V
/OC voltage	V _{/OC}	-0.3 ~ 6.0	V
/OC current	I _{S/OC}	10	mA
OUT voltage	V _{OUT}	-0.3 ~ 6.0	V
Storage temperature	T _{STG}	-55 ~ 150	°C
Power dissipation *1	PD	560	mW

*1 Derating : 4.48mW/°C for operation above Ta = 25°C

* This product is not designed for protection against radioactive rays.

* Operation is not guaranteed.

●Operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V _{IN}	2.7	5.0	5.5	V
Operating temperature	T _{OPR}	-40	-	85	°C
Load current	I _{LO}	0	-	250	mA

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

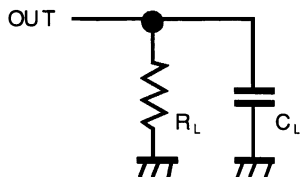
Application example

- ROHM cannot provide adequate confirmation of patents.
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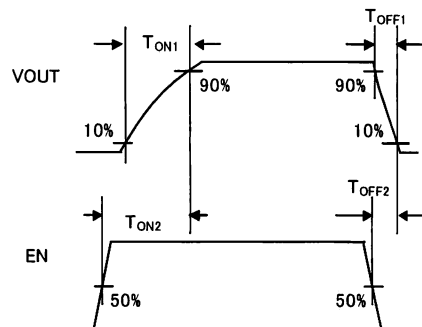
● Electric characteristics (Unless otherwise specified VIN = 5.0V, Ta = 25°C)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Supply Current						
Operating Current	IDD	-	110	140	μA	VEN = 5V, OUT = OPEN
Standby Current	ISTB	-	0.01	1	μA	VEN = 0V, OUT = OPEN
I/O						
EN input voltage	VEN	2.0	-	-	V	High level input
		-	-	0.8	V	Low level input
		-	-	0.4	V	Low level input 2.7V ≤ VIN ≤ 4.5V
EN input current	IEN	-1.0	0.01	1.0	μA	VEN = 0V or VEN = 5V
/OC output LOW voltage	V/OC	-	-	0.5	V	I/OC = 5mA
/OC output Leak current	IL/OC	-	0.01	1	μA	V/OC = 5V
Power Switch						
On-state resistance	RON	-	100	130	mΩ	IOUT = 250mA
Short circuit current	ISC	0.3	0.5	0.7	A	VIN = 5V, VOUT = 0V CL = 100μF (RMS)
Output rise time	TON1	-	1.8	10	ms	RL = 20Ω, CL = OPEN
Output turn on time	TON2	-	2.1	20	ms	RL = 20Ω, CL = OPEN
Output fall time	TOFF1	-	1	20	μs	RL = 20Ω, CL = OPEN
Output turn off time	TOFF2	-	3	40	μs	RL = 20Ω, CL = OPEN
UVLO						
UVLO Threshold	VTUVH	2.1	2.3	2.5	V	VIN rising to high voltage
	VTUVL	2.0	2.2	2.4	V	VIN falling to low voltage

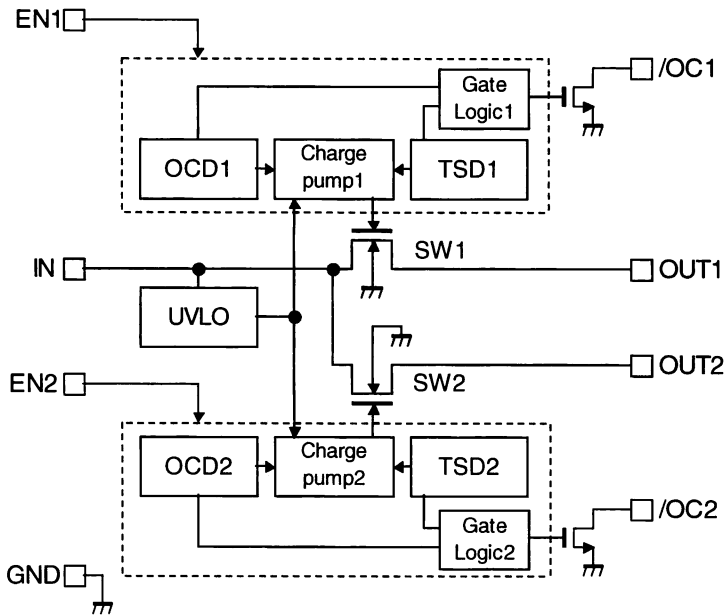
● Measurement circuit



● Timing diagram



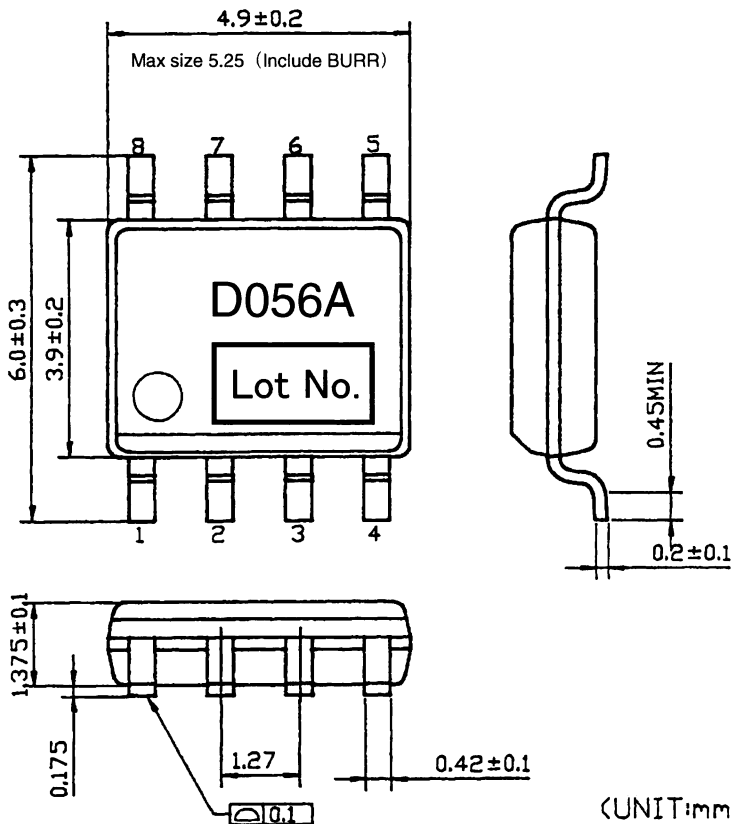
●Block Diagram



●Pin description

Pin No.	Pin Name	Function
1	GND	Ground
2	IN	Power supply input Switch input
3	EN1	Switch enable input1
4	EN2	Switch enable input2
5	/OC2	Error flag output2
6	OUT2	Switch output2
7	OUT1	Switch output1
8	/OC1	Error flag output1

●Package



(UNIT:mm)

●Cautions on use**(1) Absolute Maximum Ratings**

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become detected temperatures or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (PD) in actual states of use.

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