PIC16F785/HV785 Data Sheet

20-Pin Flash-Based, 8-Bit

CMOS Microcontroller with

Two-Phase Asynchronous Feedback PWM

Dual High-Speed Comparators and

Dual Operational Amplifiers

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PIC16F785/HV785

20-Pin Flash-Based 8-Bit CMOS Microcontroller

High-Performance RISC CPU:

- Only 35 instructions to learn:
  - All single-cycle instructions except branches
- Operating speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%
  - Software selectable frequency range of 8 MHz to 32 kHz
  - Software tunable
  - Two-Speed Start-up mode
  - Crystal fail detect for critical applications
  - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High-Endurance Flash/EEPROM cell:
  - 100,000 write Flash endurance
  - 1,000,000 write EEPROM endurance
  - Flash/Data EEPROM retention: > 40 years

Low-Power Features:

- Standby Current:
  - 30 nA @ 2.0V, typical
- Operating Current:
  - 8.5 µA @ 32 kHz, 2.0V, typical
  - 100 µA @ 1 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 µA @ 2.0V, typical
- Timer1 Oscillator Current:
  - 2 µA @ 32 kHz, 2.0V, typical

Peripheral Features:

- High-speed Comparator module with:
  - Two independent analog comparators
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - 1.2V band gap voltage reference
  - Comparator inputs and outputs externally accessible
  - < 40 ns propagation delay
  - 2 mv offset, typical
- Operational Amplifier module with 2 independent op amps:
  - 3 MHz GBWP, typical
  - All I/O pins externally accessible
- Two-Phase Asynchronous Feedback PWM module:
  - Complementary output with programmable dead band delay
  - Infinite resolution analog duty cycle
  - Sync Output/Input for multi-phase PWM
  - F_{OSC}/2 maximum PWM frequency
- A/D Converter:
  - 10-bit resolution and 14 channels (2 internal)
- 17 I/O pins and 1 input-only pin:
  - High-current source/sink for direct LED drive
  - Interrupt-on-pin change
  - Individually programmable weak pull-ups
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Gate Input mode
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module:
  - 16-bit Capture, max resolution 12.5 ns
  - Compare, max resolution 200 ns
  - 10-bit PWM with 1 output channel, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins
- Shunt Voltage Regulator (PIC16HV785 only)
  - 5 volt regulation
  - 4 mA to 50 mA shunt range

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Op Amps	Comparators	CCP	Two-Phase PWM	Timers 8/16-bit	Shunt Reg.
	Flash (words)	SRAM (bytes)	EEPROM (bytes)								
PIC16F785	2048	128	256	17+1	12+2	2	2	1	1	2/1	0
PIC16HV785	2048	128	256	17+1	12+2	2	2	1	1	2/1	1

Dual in Line Pin Diagram

20-pin PDIP, SOIC, SSOP

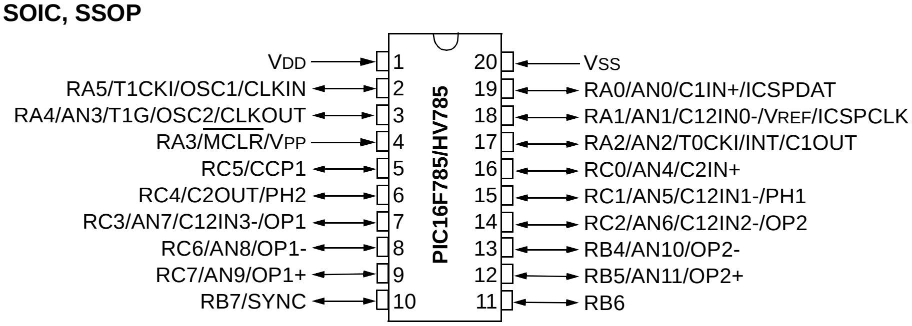

TABLE 1: DUAL IN LINE PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	19	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	18	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	17	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3(1)	4	—	—	—	—	—	—	IOC	Y	MCLR/VPP
RA4	3	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	2	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	13	AN10	—	OP2-	—	—	—	—	—	—
RB5	12	AN11	—	OP2+	—	—	—	—	—	—
RB6(2)	11	—	—	—	—	—	—	—	—	—
RB7	10	—	—	—	SYNC	—	—	—	—	—
RC0	16	AN4	C2IN+	—	—	—	—	—	—	—
RC1	15	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	14	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	7	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	6	—	C2OUT	—	PH2	—	—	—	—	—
RC5	5	—	—	—	—	—	CCP1	—	—	—
RC6	8	AN8	—	OP1-	—	—	—	—	—	—
RC7	9	AN9	—	OP1+	—	—	—	—	—	—
—	1	—	—	—	—	—	—	—	—	VDD
—	20	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Open drain.

QFN (4x4x0.9) Pin Diagram

20-PIN QFN

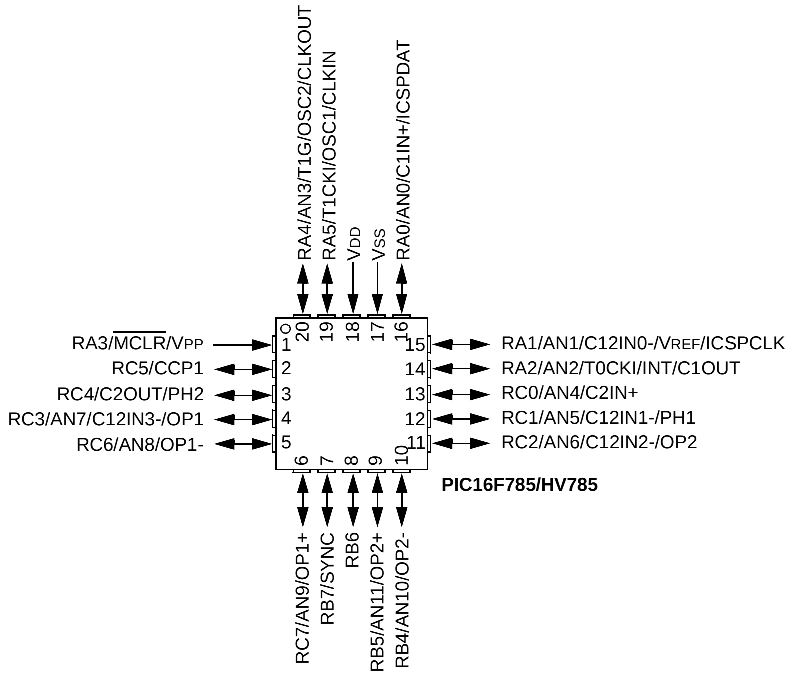

TABLE 2: QFN PIN SUMMARY

I/O	Pin	Analog	Comp.	Op Amps	PWM	Timers	CCP	Interrupt	Pull-ups	Basic
RA0	16	AN0	C1IN+	—	—	—	—	IOC	Y	ICSPDAT
RA1	15	AN1/VREF	C12IN0-	—	—	—	—	IOC	Y	ICSPCLK
RA2	14	AN2	C1OUT	—	—	T0CKI	—	INT/IOC	Y	—
RA3[(1)]	1	—	—	—	—	—	—	IOC	Y	$\overline{\text{MCLR}}$/VPP
RA4	20	AN3	—	—	—	T1G	—	IOC	Y	OSC2/CLKOUT
RA5	19	—	—	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
RB4	10	AN10	—	OP2-	—	—	—	—	—	—
RB5	9	AN11	—	OP2+	—	—	—	—	—	—
RB6[(2)]	8	—	—	—	—	—	—	—	—	—
RB7	7	—	—	—	SYNC	—	—	—	—	—
RC0	13	AN4	C2IN+	—	—	—	—	—	—	—
RC1	12	AN5	C12IN1-	—	PH1	—	—	—	—	—
RC2	11	AN6	C12IN2-	OP2	—	—	—	—	—	—
RC3	4	AN7	C12IN3-	OP1	—	—	—	—	—	—
RC4	3	—	C2OUT	—	PH2	—	—	—	—	—
RC5	2	—	—	—	—	—	CCP1	—	—	—
RC6	5	AN8	—	OP1-	—	—	—	—	—	—
RC7	6	AN9	—	OP1+	—	—	—	—	—	—
—	18	—	—	—	—	—	—	—	—	VDD
—	17	—	—	—	—	—	—	—	—	VSS

Note 1: Input only.
2: Open drain.

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1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC16F785/HV785. Additional information may be found in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this Data Sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F785/HV785 is covered by this Data Sheet. It is available in 20-pin PDIP, SOIC, SSOP and QFN packages. Figure 1-1 shows a block diagram of the PIC16F785/HV785 device. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC16F785/HV785 BLOCK DIAGRAM

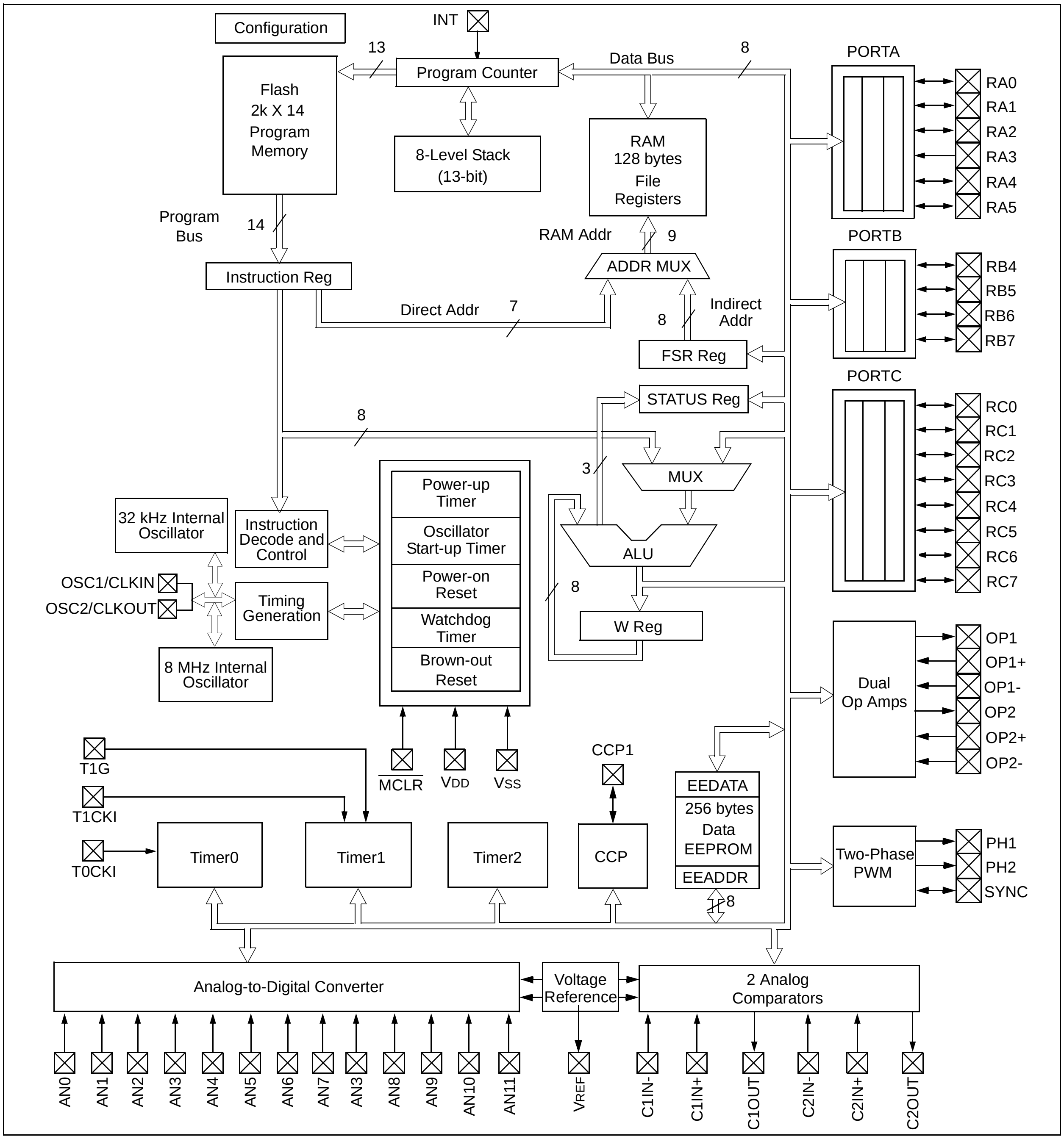


TABLE 1-1: PIC16F785/HV785 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	C1IN+	AN	—	Comparator 1 non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
RA1/AN1/C12IN0-/VREF/ ICSPCLK	RA1	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	C12IN0-	AN	—	Comparator 1 and 2 inverting input
	VREF	AN	AN	External Voltage Reference for A/D, buffered reference output
	ICSPCLK	ST	—	Serial Programming Clock
RA2/AN2/T0CKI/INT/C1OUT	RA2	ST	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	C1OUT	—	CMOS	Comparator 1 output
RA3/$\overline{\text{MCLR}}$/Vpp	RA3	TTL	—	PORTA input with prog. pull-up and interrupt-on-change
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
	VPP	HV	—	Programming voltage
RA4/AN3/T1G/OSC2/ CLKOUT	RA4	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	T1G	ST	—	Timer1 gate
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
RA5/T1CKI/OSC1/CLKIN	RA5	TTL	CMOS	PORTA I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
RB4/AN10/OP2-	RB4	TTL	CMOS	PORTB I/O
	AN10	AN	—	A/D Channel 10 input
	OP2-	—	AN	Op Amp 2 inverting input
RB5/AN11/OP2+	RB5	TTL	CMOS	PORTB I/O
	AN11	AN	—	A/D Channel 11 input
	OP2+	—	AN	Op Amp 2 non-inverting input
RB6	RB6	TTL	OD	PORTB I/O. Open drain output
RB7/SYNC	RB7	TTL	CMOS	PORTB I/O
	SYNC	ST	CMOS	Master PWM Sync output or slave PWM Sync input
RC0/AN4/C2IN+	RC0	TTL	CMOS	PORTC I/O
	AN4	AN	—	A/D Channel 4 input
	C2IN+	AN	—	Comparator 2 non-inverting input

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, AN = Analog, OD = Open Drain output, HV = High Voltage

TABLE 1-1: PIC16F785/HV785 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC1/AN5/C12IN1-/PH1	RC1	TTL	CMOS	PORTC I/O
	AN5	AN	—	A/D Channel 5 input
	C12IN1-	AN	—	Comparator 1 and 2 inverting input
	PH1	—	CMOS	PWM phase 1 output
RC2/AN6/C12IN2-/OP2	RC2	TTL	CMOS	PORTC I/O
	AN6	AN	—	A/D Channel 6 input
	C12IN2-	AN	—	Comparator 1 and 2 inverting input
	OP2	—	AN	Op Amp 2 output
RC3/AN7/C12IN3-/OP1	RC3	TTL	CMOS	PORTC I/O
	AN7	AN	—	A/D Channel 7 input
	C12IN3-	AN	—	Comparator 1 and 2 inverting input
	OP1	—	AN	Op Amp 1 output
RC4/C2OUT/PH2	RC4	TTL	CMOS	PORTC I/O
	C2OUT	—	CMOS	Comparator 2 output
	PH2	—	CMOS	PWM phase 2 output
RC5/CCP1	RC5	TTL	CMOS	PORTC I/O
	CCP1	ST	CMOS	Capture input/Compare output
RC6/AN8/OP1-	RC6	TTL	CMOS	PORTC I/O
	AN8	AN	—	A/D Channel 8 input
	OP1-	AN	—	Op Amp 1 inverting input
RC7/AN9/OP1+	RC7		CMOS	PORTC I/O
	AN9	AN	—	A/D Channel 9 input
	OP1+	AN	—	Op Amp 1 non-inverting input
VSS	VSS	Power	—	Ground reference
VDD	VDD	Power	—	Positive supply

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, AN = Analog, OD = Open Drain output, HV = High Voltage

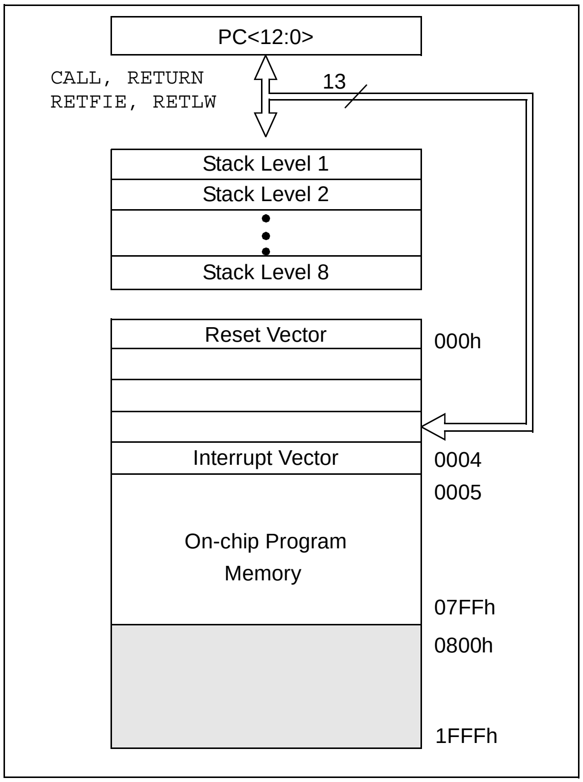
NOTES:

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F785/HV785 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC16F785/HV785 is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 2k x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC16F785/HV785



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into four banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. The last sixteen register locations in Bank 1 (F0h-FFh), Bank 2 (170h-17Fh), and Bank 3 (1F0h-1FFh) point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read.

Seven address bits are required to access any location in a data memory bank. Two additional bits are required to access the four banks. When data memory is accessed directly, the seven Least Significant address bits are contained within the opcode and the two Most Significant bits are contained in the STATUS register. RP0 and RP1 (STATUS<5> and STATUS<6>) are the two Most Significant data memory address bits and are also known as the bank select bits. Table 2-1 lists how to access the four banks of registers.

TABLE 2-1: BANK SELECTION

	RP1	RP0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file banks are organized as 128 x 8 in the PIC16F785/HV785. Each register is accessed, either directly, by seven address bits within the opcode, or indirectly, through the File Select Register (FSR). When the FSR is used to access data memory, the eight Least Significant data memory address bits are contained in the FSR and the ninth Most Significant address bit is contained in the IRP bit (STATUS<7>) of the STATUS register. (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-2). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC16F785/HV785

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(1)	00h	Indirect addr.(1)	80h	Indirect addr.(1)	100h	Indirect addr.(1)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	PORTA	105h	TRISA	185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h	PORTC	107h	TRISC	187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch		10Ch	PIE1	18Ch
	0Dh		8Dh		10Dh		18Dh
TMR1L	0Eh	PCON	8Eh		10Eh		18Eh
TMR1H	0Fh	OSCCON	8Fh		10Fh		18Fh
T1CON	10h	OSCTUNE	90h	PWMCON1	110h		190h
TMR2	11h	ANSEL0	91h	PWMCON0	111h		191h
T2CON	12h	PR2	92h	PWMCLK	112h		192h
CCPR1L	13h	ANSEL1	93h	PWMPH1	113h		193h
CCPR1H	14h		94h	PWMPH2	114h		194h
CCP1CON	15h	WPUA	95h		115h		195h
	16h	IOCA	96h		116h		196h
	17h		97h		117h		197h
WDTCON	18h	REFCON	98h		118h		198h
	19h	VRCON	99h	CM1CON0	119h		199h
	1Ah	EEDAT	9Ah	CM2CON0	11Ah		19Ah
	1Bh	EEADR	9Bh	CM2CON1	11Bh		19Bh
	1Ch	EECON1	9Ch	OPA1CON	11Ch		19Ch
	1Dh	EECON2(1)	9Dh	OPA2CON	11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 32 Bytes	A0h		120h		1A0h
			BFh				
			C0h				
	6Fh		EFh		16Fh		1EFh
	70h	accesses Bank 0	F0h	accesses Bank 0	170h	accesses Bank 0	1F0h
	7Fh		FFh		17Fh		1FFh

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

TABLE 2-2: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
01h	TMR0	Timer0 Module's Register								xxxx xxxx	49,114
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
03h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	15,114
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
05h	PORTA(1)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	35,114
06h	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xx00 ----	42,114
07h	PORTC(1)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00xx 0000	45,114
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
0Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	19,114
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	52,114
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	52,114
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	53,114
11h	TMR2	Timer2 Module Register								0000 0000	55,114
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	55,114
13h	CCPR1L	Capture/Compare/PWM Register1 Low Byte								xxxx xxxx	58,114
14h	CCPR1H	Capture/Compare/PWM Register1 High Byte								xxxx xxxx	58,114
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	58,114
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	122,114
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	Most Significant 8 bits of the left justified A/D result or 2 bits of right justified result								xxxx xxxx	81,114
1Fh	ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	83,114

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Port pins with analog functions controlled by the ANSEL0 and ANSEL1 registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

TABLE 2-3: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
81h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	16,114
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
83h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	15,114
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
85h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	35,114
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	42,114
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	45,114
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	18,114
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---1 --qq	20,114
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS(1)	HTS	LTS	SCS	-110 q000	33,114
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	28,114
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	82,114
92h	PR2	Timer2 Module Period Register								1111 1111	55,114
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	82,114
94h	—	Unimplemented								—	—
95h	WPUA	—	—	WPUA5	WPUA4	WPUA3(2)	WPUA2	WPUA1	WPUA0	--11 1111	36,114
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	37,114
97h	—	Unimplemented								—	—
98h	REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	72,114
99h	VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000- 0000	71,114
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	103,114
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	103,114
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	104,114
9Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	104,114
9Eh	ADRESL	Least Significant 2 bits of the left justified A/D result or 8 bits of the right justified result								xxxx xxxx	81,114
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	84,114

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled, otherwise this bit resets to '1'.

2: RA3 pull-up is enabled when MCLRE is '1' in Configuration Word.

TABLE 2-4: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 2											
100h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
101h	TMR0	Timer0 Module's Register								xxxx xxxx	49,114
102h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
103h	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	15,114
104h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
105h	PORTA(1)	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--x0 x000	35,114
106h	PORTB(1)	RB7	RB6	RB5	RB4	—	—	—	—	xx00 ----	42,114
107h	PORTC(1)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00xx 0000	45,114
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
10Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
10Ch	—	Unimplemented								—	—
10Dh	—	Unimplemented								—	—
10Eh	—	Unimplemented								—	—
10Fh	—	Unimplemented								—	—
110h	PWMCON1	—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0	-000 0000	101,114
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	93,114
112h	PWMCLK	PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0	0000 0000	94,114
113h	PWMPH1	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	95,114
114h	PWMPH2	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	96,114
115h	—	Unimplemented								—	—
116h	—	Unimplemented								—	—
117h	—	Unimplemented								—	—
118h	—	Unimplemented								—	—
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	65,114
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	67,114
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	68,114
11Ch	OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	76,114
11Eh	—	Unimplemented								—	—
11Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: Port pins with analog functions controlled by the ANSEL0 and ANSEL1 registers will read '0' immediately after a Reset even though the data latches are either undefined (POR) or unchanged (other Resets).

TABLE 2-5: PIC16F785/HV785 SPECIAL FUNCTION REGISTERS SUMMARY BANK 3

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Page
Bank 3											
180h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	22,114
181h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	16,114
182h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	21,114
183h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	15,114
184h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	22,114
185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	36,114
186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	42,114
187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	45,114
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	21,114
18Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	17,114
18Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	18,114
18Dh	—	Unimplemented								—	—
18Eh	—	Unimplemented								—	—
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	—	Unimplemented								—	—
192h	—	Unimplemented								—	—
193h	—	Unimplemented								—	—
194h	—	Unimplemented								—	—
195h	—	Unimplemented								—	—
196h	—	Unimplemented								—	—
197h	—	Unimplemented								—	—
198h	—	Unimplemented								—	—
199h	—	Unimplemented								—	—
19Ah	—	Unimplemented								—	—
19Bh	—	Unimplemented								—	—
19Ch	—	Unimplemented								—	—
19Dh	—	Unimplemented								—	—
19Eh	—	Unimplemented								—	—
19Fh	—	Unimplemented								—	—

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

2.2.2.1 STATUS Register

The STATUS register contains arithmetic status of the ALU, the Reset status and the bank select bits for data memory (SRAM).

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see **Section 17.0 "Instruction Set Summary"**.

Note:	The C and DC bits operate as a $\overline{\text{Borrow}}$ and $\overline{\text{Digit Borrow}}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER (ADDRESS: 03h, 83h, 103h OR 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC(1)	C(1)
bit 7							bit 0

bit 7 **IRP:** Register Bank Select bit (used for Indirect addressing)
`1` = Bank 2,3 (100h-1FFh)
`0` = Bank 0,1 (00h-FFh)

bit 6-5 **RP<1:0>:** Register Bank Select bits (used for Direct addressing)
`11` = Bank 3 (180h-1FFh)
`10` = Bank 2 (100h-17Fh)
`01` = Bank 1 (80h-FFh)
`00` = Bank 0 (00h-7Fh)

bit 4 **$\overline{\text{TO}}$:** Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$:** Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
For $\overline{\text{borrow}}$, the polarity is reversed.
`1` = A carry-out from the 4th low-order bit of the result occurred
`0` = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(1)
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.2 OPTION_REG Register

The Option register is a readable and writable register, which contains various control bits to configure the TMR0/WDT prescaler, the external RA2/INT interrupt, the TMR0 and the weak pull-ups on PORTA.

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' (OPTION_REG<3>). See **Section 5.4 "Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER (ADDRESS: 81h OR 181h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RAPU}}$:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual port latch values in WPUA register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/AN2/T0CKI/INT/C1OUT pin
0 = Interrupt on falling edge of RA2/AN2/T0CKI/INT/C1OUT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/AN2/T0CKI/INT/C1OUT pin
0 = Increment on low-to-high transition on RA2/AN2/T0CKI/INT/C1OUT pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate[(1)]
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available for the PIC16F785/HV785. See **Section 15.5 "Watchdog Timer (WDT)"** for more information.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.2.2.3 INTCON Register

The Interrupt Control register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, PORTA change and external RA2/INT pin interrupts.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh, 8Bh, 10Bh OR 183h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	T0IE	INTE	RAIE(1)	T0IF(2)	INTF	RAIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Enable bit
1 = Enables the RA2/AN2/T0CKI/INT/C1OUT external interrupt
0 = Disables the RA2/AN2/T0CKI/INT/C1OUT external interrupt

bit 3 **RAIE:** PORTA Change Interrupt Enable bit(1)
1 = Enables the PORTA change interrupt
0 = Disables the PORTA change interrupt

bit 2 **T0IF:** TMR0 Overflow Interrupt Flag bit(2)
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF:** RA2/AN2/T0CKI/INT/C1OUT External Interrupt Flag bit
1 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt occurred (must be cleared in software)
0 = The RA2/AN2/T0CKI/INT/C1OUT external interrupt did not occur

bit 0 **RAIF:** PORTA Change Interrupt Flag bit
1 = When at least one of the PORTA <5:0> pins changed state (must be cleared in software)
0 = None of the PORTA <5:0> pins have changed state

Note 1: IOCA register must also be enabled.

2: T0IF bit is set when Timer0 rolls over. Timer0 is unchanged on Reset and should be initialized before clearing T0IF bit.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

2.2.2.4 PIE1 Register

The Peripheral Interrupt Enable Register 1 contains the interrupt enable bits, as shown in Register 2-4.

Note:	Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS: 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit
1 = Enables the EE write complete interrupt
0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter Interrupt Enable bit
1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **C2IE:** Comparator 2 Interrupt Enable bit
1 = Enables the Comparator 2 interrupt
0 = Disables the Comparator 2 interrupt

bit 3 **C1IE:** Comparator 1 Interrupt Enable bit
1 = Enables the Comparator 1 interrupt
0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail interrupt
0 = Disables the Oscillator Fail interrupt

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

2.2.2.5 PIR1 Register

The Peripheral Interrupt Register 1 contains the interrupt flag bits.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REGISTER 1 (ADDRESS: 0Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started

bit 6 **ADIF:** A/D Interrupt Flag bit
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **C2IF:** Comparator 2 Interrupt Flag bit
1 = Comparator 2 output has changed (must be cleared in software)
0 = Comparator 2 output has not changed

bit 3 **C1IF:** Comparator 1 Interrupt Flag bit
1 = Comparator 1 output has changed (must be cleared in software)
0 = Comparator 1 output has not changed

bit 2 **OSFIF:** Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = System clock operating

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

2.2.2.6 PCON Register

The Power Control register contains flag bits to allow differentiation between a Power-on Reset ($\overline{\text{POR}}$), a Brown-out Reset ($\overline{\text{BOR}}$), a Watchdog Timer (WDT) Reset (WDT) and an external $\overline{\text{MCLR}}$ Reset.

REGISTER 2-6: PCON: POWER CONTROL REGISTER (ADDRESS: 8Eh)

U-0	U-0	U-0	R/W-1	U-0	U-0	R/W-0	R/W-x
—	—	—	SBOREN(1)	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **SBOREN:** Software BOR Enable bit(1)
1 = BOR enabled
0 = BOR disabled

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: BOREN<1:0> = 01 in Configuration Word for this bit to control the $\overline{\text{BOR}}$.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.3 PCL and PCLATH

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The program counter is 13 bits wide. The low byte is called the PCL register. The PCL register is readable and writable. The high byte of the PC (PC<12:8>) is called the PCH register. This register contains PC<12:8> bits which are not directly readable or writable. All updates to the PCH register goes through the PCLATH register.

On any Reset, the PC is cleared. Figure 2-3 shows the two situations for loading the PC. The upper example of Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example of Figure 2-3 shows how the PC is loaded during a `CALL` or `GOTO` instruction (PCLATH<4:3> → PCH).

2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper 5 bits to the PCLATH register. When the lower 8 bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

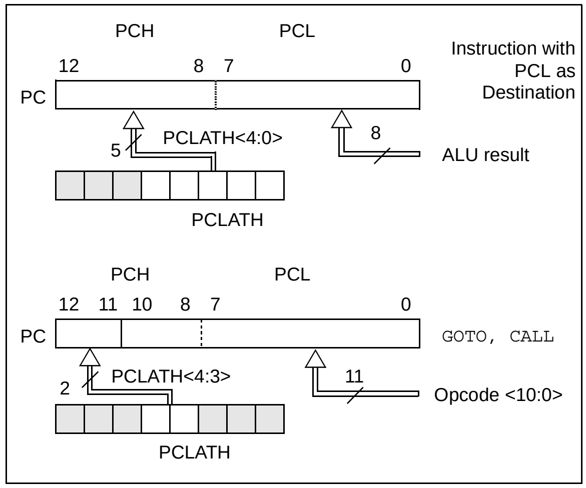
A computed `GOTO` is accomplished by adding an offset to the program counter (`ADDWF PCL`). Care should be exercised when jumping into a look-up table or program branch table (computed `GOTO`) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower 8 bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 PROGRAM MEMORY PAGING

The `CALL` and `GOTO` instructions provide 11 bits of address to allow branching within any 2K program memory page. When using a `CALL` or `GOTO` instruction, the Most Significant bits of the address are provided by PCLATH<4:3> (page select bits). When using a `CALL` or `GOTO` instruction, the user must ensure that the page select bits are programmed so that the desired destination program memory page is addressed. When the `CALL` instruction (or interrupt) is executed, the entire 13-bit PC return address is PUSHed onto the stack. Therefore, manipulation of the PCLATH<3> bit is not required for the `RETURN` or `RETFIE` instructions (which POPs the address from the stack).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.3 STACK

The PIC16F785/HV785 family has an 8-level deep x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or `RETFIE` instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth PUSH overwrites the value that was stored from the first PUSH. The tenth PUSH overwrites the second PUSH (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL`, `RETURN`, `RETLW` and `RETFIE` instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

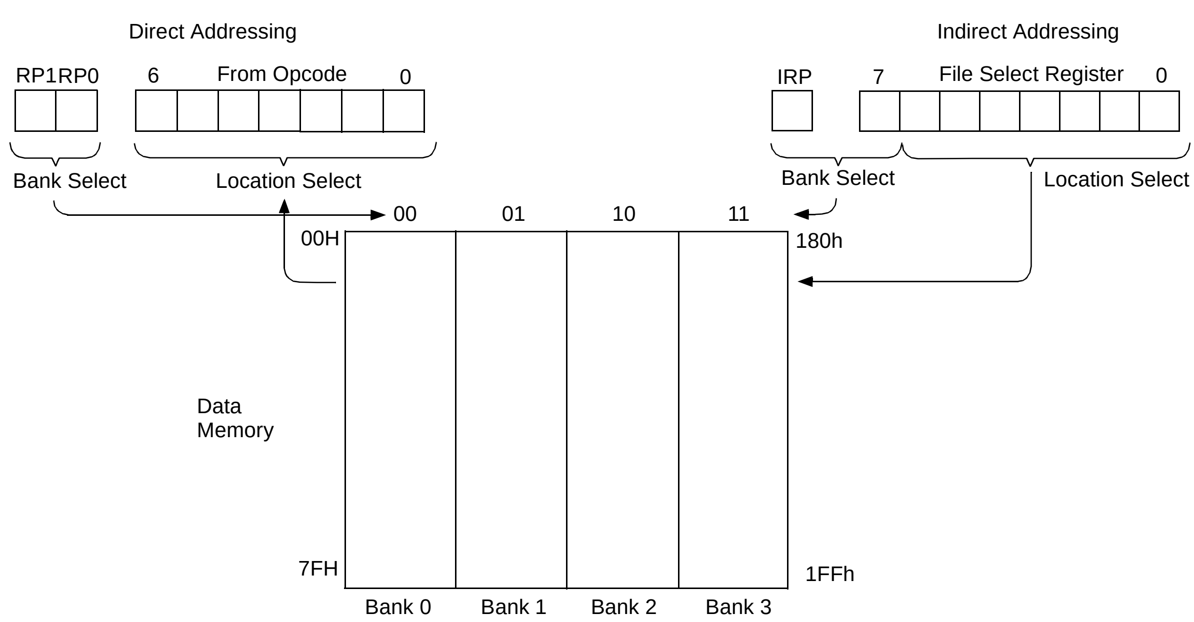
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit (STATUS<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
      MOVLW  0x20   ;initialize pointer
      MOVWF  FSR    ;to RAM
NEXT  CLRF   INDF   ;clear INDF register
      INCF   FSR    ;increment pointer
      BTFSS  FSR,4  ;all done?
      GOTO   NEXT   ;no clear next
CONTINUE            ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC16F785/HV785



Note: For memory map detail see Figure 2-2.

3.0 CLOCK SOURCES

3.1 Overview

The PIC16F785/HV785 has a wide variety of clock sources and selection features to allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the PIC16F785/HV785 clock sources.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

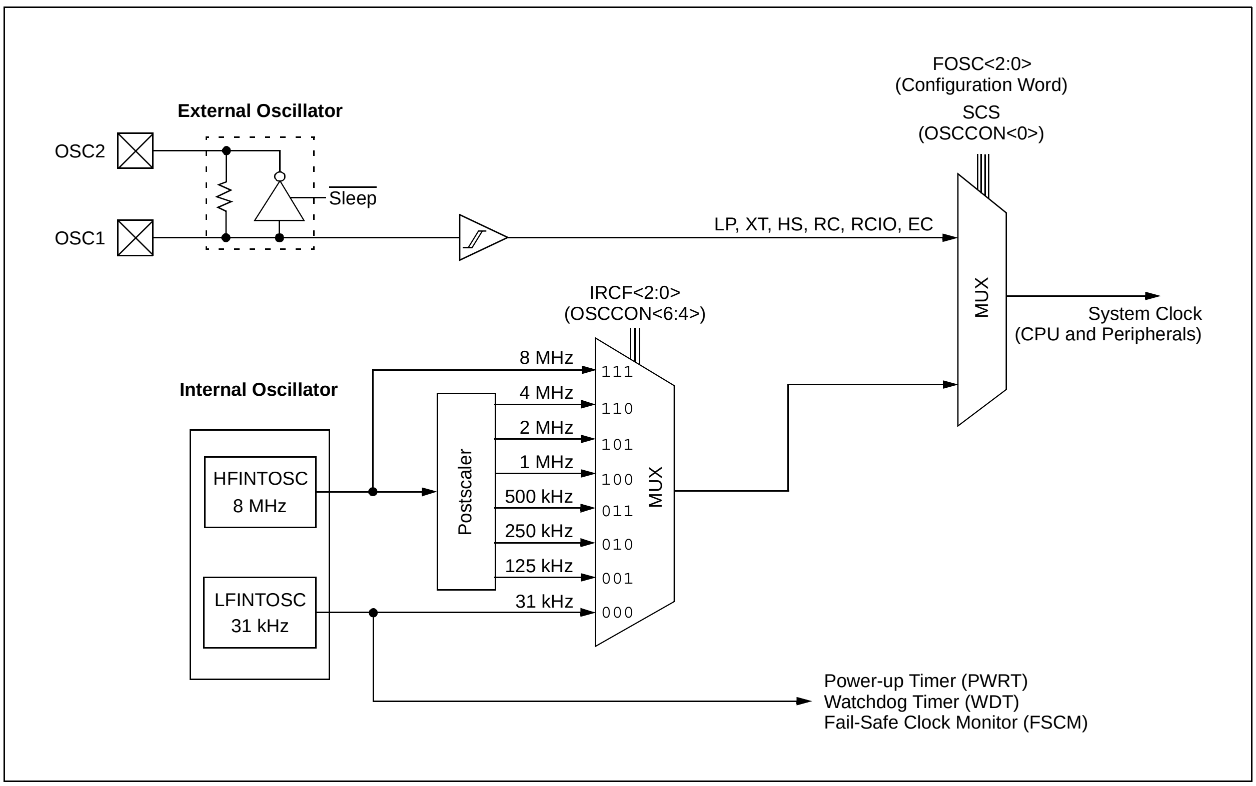
- Selectable system clock source between external or internal via software.
- Two-Speed Clock Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch to the internal oscillator.

The PIC16F785/HV785 can be configured in one of eight clock modes.

1. EC – External clock with I/O on RA4.
2. LP – 32.768 kHz Watch Crystal or Ceramic Resonator Oscillator mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with FOSC/4 output on RA4
6. RCIO – External Resistor-Capacitor with I/O on RA4.
7. INTOSC – Internal Oscillator with FOSC/4 output on RA4 and I/O on RA5.
8. INTOSCIO – Internal Oscillator with I/O on RA4 and RA5.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word (see **Section 15.0 “Special Features of the CPU”**). Once the PIC16F785/HV785 is programmed and the Clock Source mode configured, it cannot be changed in the software.

FIGURE 3-1: PIC16F785/HV785 CLOCK SOURCE BLOCK DIAGRAM



3.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT, and HS modes) and resistor-capacitor (RC mode) circuits.
- Internal clock sources are contained internally within the PIC16F785/HV785. The PIC16F785/HV785 has two internal oscillators; the 8 MHz High-frequency Internal Oscillator (HFINTOSC) and 31 kHz Low-frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 "Clock Switching"**).

3.3 External Clock Modes

3.3.1 OSCILLATOR START-UP TIMER (OST)

When the PIC16F785/HV785 is configured for any of the Crystal Oscillator modes (LP, XT or HS), the Oscillator Start-up Timer (OST) is enabled, which extends the Reset period to allow the oscillator additional time to stabilize. The OST counts 1024 clock periods present on the OSC1 pin following a Power-on Reset (POR), a wake from Sleep, or when the Power-up Timer (PWRT) has expired (if the PWRT is enabled). During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the PIC16F785/HV785. Table 3-1 shows examples where the oscillator delay is invoked.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 3.6 "Two-Speed Clock Start-up Mode"**).

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

Switch From	Switch To	Frequency	Oscillator Delay	Comments
Sleep/POR	INTRC INTOSC	31 kHz 125 kHz-8 MHz	5 µs-10 µs (approx.) CPU Start-up(1)	Following a wake-up from Sleep mode or POR, CPU start-up is invoked to allow the CPU to become ready for code execution.
Sleep	EC, RC	DC – 20 MHz		
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz		
Sleep/POR	LP, XT, HS	31 kHz-20 MHz	1024 Clock Cycles (OST)	
LFINTOSC (31 kHz)	INTOSC	125 kHz-8 MHz	1 µs (approx.)	

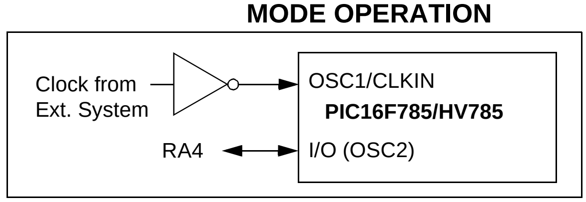
Note 1: The 5 µs-10 µs start-up delay is based on a 1 MHz System Clock.

3.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to OSC1 pin and the RA4 pin is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC16F785/HV785 design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



3.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to the OSC1 and OSC2 pins (Figure 3-1). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

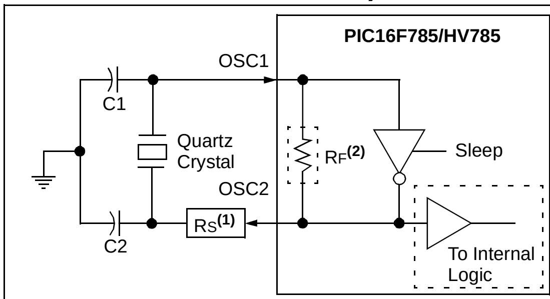
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is best suited to drive resonators with a low drive level specification, for example, tuning fork type crystals.

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification, for example, AT-cut quartz crystal resonators.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting, for example, AT-cut quartz crystal resonators or ceramic resonators.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)

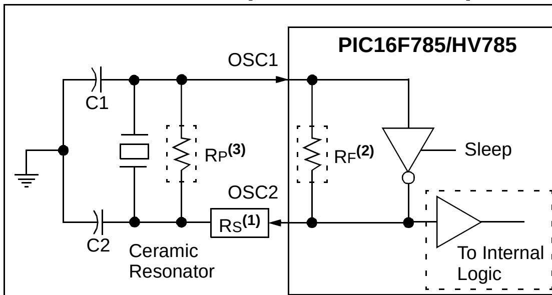


Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

> **Note 1:** Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
>
> **2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation (typical value 1 MΩ).

TABLE 3-2: CERAMIC RESONATORS

Mode	Freq.	OSC1 (C1)	OSC2 (C2)
XT	455 kHz 2.0 MHz	68-100 pF 15-68 pF	68-100 pF 15-68 pF
HS	4.0 MHz 8.0 MHz 16.0 MHz	10-68 pF 15-68 pF 10-22 pF	10-68 pF 15-68 pF 10-22 pF

Note: **These values are for design guidance only.** See notes following this table.

TABLE 3-3: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz	15-33 pF	15-33 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15-33 pF	15-33 pF
	4 MHz	15-33 pF	15-33 pF
HS	4 MHz	15-33 pF	15-33 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

Note: These values are for design guidance only. See notes following this table.

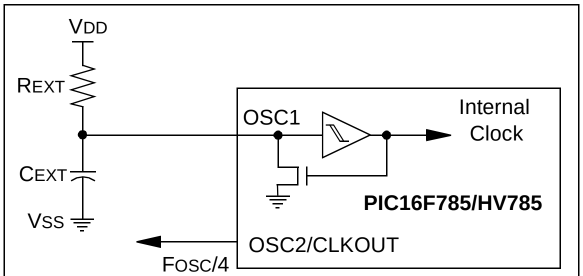
> **Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
>
> **2:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
>
> **3:** RS may be required to avoid overdriving crystals with low drive level specification.

3.3.4 EXTERNAL RC MODES

The External Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes, RC and RCIO.

In RC mode, the RC circuit connects to the OSC1 pin. The OSC2/CLKOUT pin outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the RC mode connections.

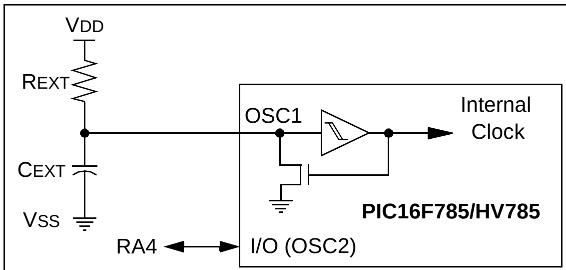
FIGURE 3-5: RC MODE



Recommended values: 3 kΩ ≤ REXT ≤ 100 kΩ (VDD ≥ 3.0V)
10 kΩ ≤ REXT ≤ 100 kΩ (VDD < 3.0V)
CEXT > 20 pF

In RCIO mode, the RC circuit is connected to the OSC1 pin. The OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 4 of PORTA (RA4). Figure 3-6 shows the RCIO mode connections.

FIGURE 3-6: RCIO MODE



Recommended values: 3 kΩ ≤ REXT ≤ 100 kΩ (VDD ≥ 3.0V)
10 kΩ ≤ REXT ≤ 100 kΩ (VDD < 3.0V)
CEXT > 20 pF

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal threshold voltage. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency or low CEXT values. The user also needs to take into account variation due to tolerance of external RC components used.

3.4 Internal Clock Modes

The PIC16F785/HV785 has two independent, internal oscillators that can be configured or selected as the system clock source.

1. The **HFINTOSC** (High-frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user adjusted ±12% via software using the OSCTUNE register (Register 3-1).
2. The **LFINTOSC** (Low-frequency Internal Oscillator) is uncalibrated and operates at approximately 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select (IRCF) bits.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit (see **Section 3.5 "Clock Switching"**).

3.4.1 INTRC AND INTRCIO MODES

The INTRC and INTRCIO modes configure the internal oscillators as the system clock source when the device is programmed using the Oscillator Selection (FOSC) bits in the Configuration Word (Register 12-1).

In **INTRC** mode, the OSC1 pin is available for general purpose I/O. The OSC2/CLKOUT pin outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTRCIO** mode, the OSC1 and OSC2 pins are available for general purpose I/O.

3.4.2 HFINTOSC

The High-frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered approximately ±12% via software using the OSCTUNE register (Register 3-1).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF bits (see **Section 3.4.4 "Frequency Select Bits (IRCF)"**).

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz (IRCF ≠ `000`) as the system clock source (SCS = `1`) or when Two-Speed Start-up is enabled (IESO = `1` and IRCF ≠ `000`).

The HF Internal Oscillator (HTS) bit, (OSCCON<2>), indicates whether the HFINTOSC is stable or not.

3.4.2.1 Calibration Bits

The 8 MHz High-frequency Internal Oscillator (HFINTOSC) is factory calibrated. The HFINTOSC calibration bits are stored in the Calibration Word (CALIB) located in program memory location 2008h. The Calibration Word is not erased using the specified bulk erase sequence in the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) and does not require reprogramming. Reference the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information on the Calibration Word register.

Note:	Address 2008h is beyond the user program memory space. It belongs to the special Configuration Memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

3.4.2.2 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-1).

The OSCTUNE register has a nominal tuning range of ±12%. The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number. Due to process variation, the monotonicity and frequency step cannot be specified.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. The HFINTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER (ADDRESS 90h)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits
01111 = Maximum frequency
01110 =
•
•
•
00001 =
00000 = Center frequency. Oscillator module is running at the calibrated frequency.
11111 =
•
•
•
10000 = Minimum frequency

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 Preliminary

3.4.3 LFINTOSC

The Low-frequency Internal Oscillator (LFINTOSC) is an uncalibrated (approximate) 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). 31 kHz can be selected via software using the IRCF bits (see **Section 3.4.4 "Frequency Select Bits (IRCF)"**). The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF = `000`) as the system clock source (SCS = `1`), or when any of the following are enabled:

- Two-Speed Start-up (IESO = `1` and IRCF = `000`)
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit, (OSCCON<1>), indicates whether the LFINTOSC is stable or not.

3.4.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connect to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency select bits IRCF<2:0> (OSCCON<6:4>) select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz

Note:	Following any Reset, the IRCF bits are set to '`110`' and the frequency selection is forced to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.4.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power. If this is the case, there is a 10 μs delay after the IRCF bits are modified before the frequency selection takes place. The LTS/HTS bits will reflect the current active status of the LFINTOSC and the HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. IRCF bits are modified.
2. If the new clock is shut down, a 10 μs clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. HTS/LTS bits are updated as required.
6. Clock switch is complete.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and the new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

Note:	Care must be taken to ensure an invalid voltage or frequency selection is not selected. An example of an invalid configuration is selecting 8 MHz when V_{DD} is 2.0V.

3.5 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit.

3.5.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit, (OSCCON<0>), selects the system clock source that is used for the CPU and peripherals.

- When SCS = `0`, the system clock source is determined by configuration of the FOSC<2:0> bits in Configuration Word (CONFIG).
- When SCS = `1`, the system clock source is chosen by the internal oscillator frequency selected by the IRCF bits. After a Reset, SCS is always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit. The user can monitor the OSTS (OSCCON<3>) to determine the current system clock source.

3.5.2 OSCILLATOR START-UP TIME-OUT STATUS BIT

The Oscillator Start-up Time-out Status (OSTS) bit, (OSCCON<3>), indicates whether the system clock is running from the external clock source as defined by the FOSC bits, or from internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.6 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note:	Executing a `SLEEP` instruction will abort the Oscillator Start-up Time and will cause the OSTS bit (OSCCON<3>) to remain clear.

When the PIC16F785/HV785 is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.3.1 "Oscillator Start-up Timer (OST)"**). The OST timer will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit (OSCCON<3>) is set, program execution switches to the external oscillator.

3.6.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO = `1` (CONFIG<10>) Internal/External Switch Over bit.
- SCS = `0`.
- FOSC configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after PWRT has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

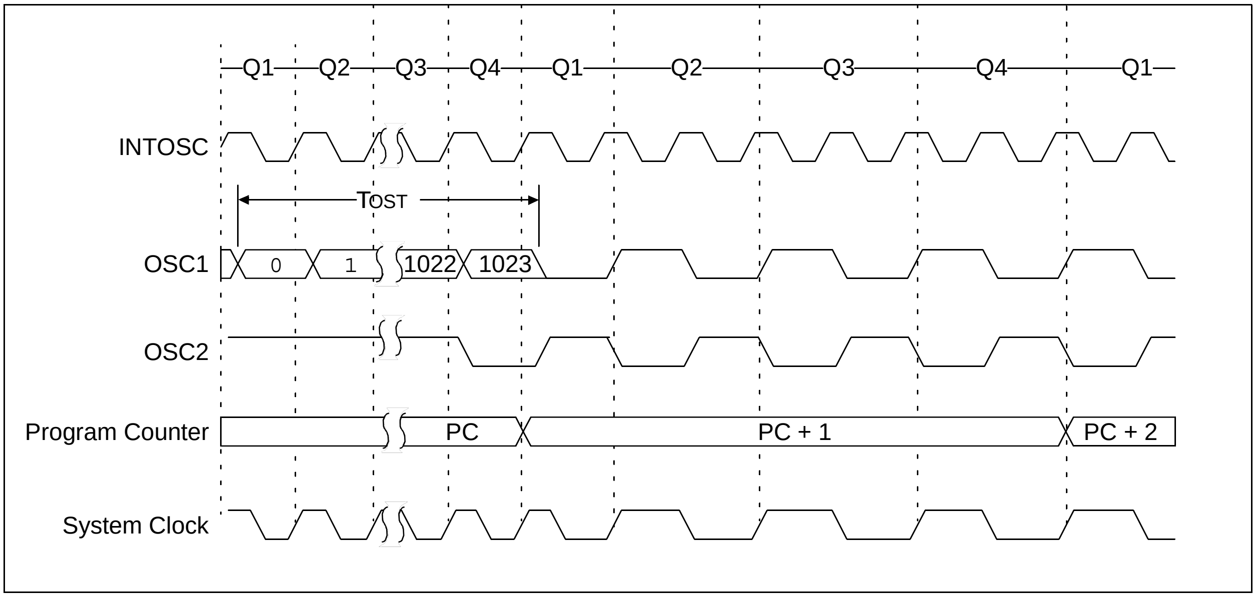
3.6.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF bits (OSCCON<6:4>).
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (LP, XT or HS mode).
7. System clock is switched to external clock source.

3.6.3 CHECKING EXTERNAL/INTERNAL CLOCK STATUS

Checking the state of the OSTS bit (OSCCON<3>) will confirm if the PIC16F785/HV785 is running from the external clock source as defined by the FOSC bits in the Configuration Word (CONFIG) or the internal oscillator.

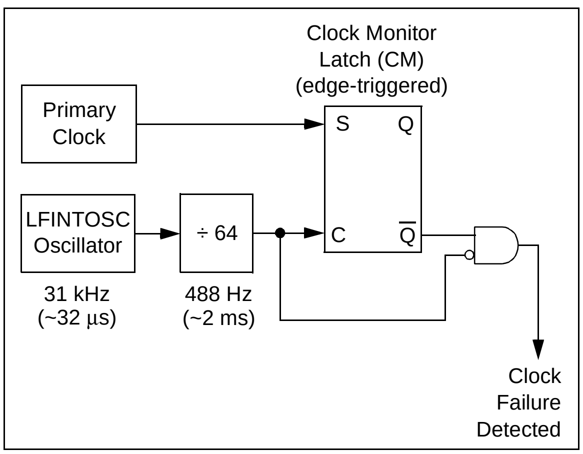
FIGURE 3-7: TWO-SPEED START-UP



3.7 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate in the event of an oscillator failure. The FSCM can detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired.

FIGURE 3-8: FSCM BLOCK DIAGRAM



The FSCM function is enabled by setting the FCMEN bit in Configuration Word (CONFIG). It is applicable to all external clock options (LP, XT, HS, EC, RC or I/O modes).

In the event of an external clock failure, the FSCM will set the OSFIF bit (PIR1<2>) and generate an oscillator fail interrupt if the OSFIE bit (PIE1<2>) is set. The device will then switch the system clock to the internal oscillator. The system clock will continue to come from the internal oscillator unless the external clock recovers and the Fail-Safe condition is exited.

The frequency of the internal oscillator will depend upon the value contained in the IRCF bits (OSCCON<6:4>). Upon entering the Fail-Safe condition, the OSTS bit (OSCCON<3>) is automatically cleared to reflect that the internal oscillator is active and the WDT is cleared. The SCS bit (OSCCON<0>) is not updated. Enabling FSCM does not affect the LTS bit.

The FSCM sample clock is generated by dividing the LFINTOSC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur. Figure 3-8 shows the FSCM block diagram.

On the rising edge of the sample clock, the monitoring latch (CM = 0) will be cleared. On a falling edge of the primary system clock, the monitoring latch will be set (CM = 1). In the event that a falling edge of the sample clock occurs, and the monitoring latch is not set, a clock failure has been detected. The assigned internal oscillator is enabled when FSCM is enabled as reflected by the IRCF bits.

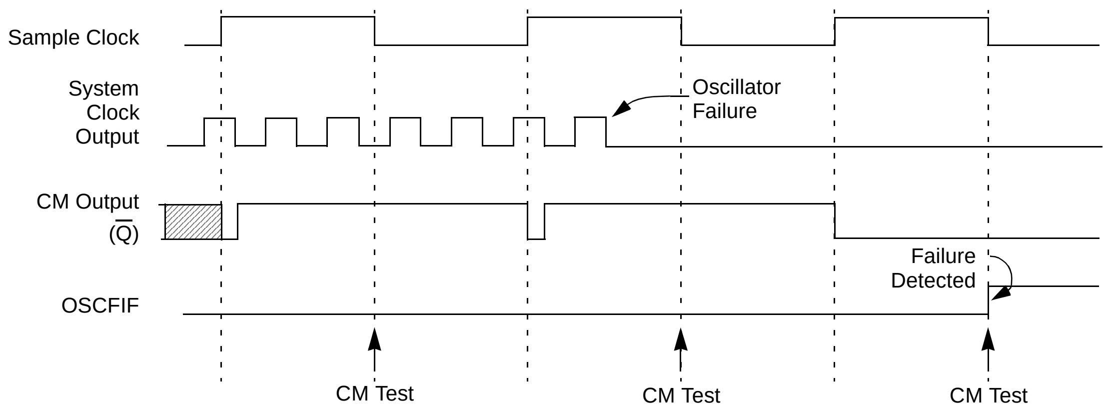
Note:	Two-Speed Start-up is automatically enabled when the Fail-Safe Clock Monitor mode is enabled.

3.7.1 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, the execution of a `SLEEP` instruction, or a modification of the SCS bit. While in Fail-Safe condition, the PIC16F785/HV785 uses the internal oscillator as the system clock source. The IRCF bits (OSCCON<6:4>) can be modified to adjust the internal oscillator frequency without exiting the Fail-Safe condition.

The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

FIGURE 3-9: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

3.7.2 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited a Reset or Sleep condition and the Oscillator Start-up Timer (OST) has expired. If the external clock is EC or RC mode, monitoring will begin immediately following these events.

For LP, XT or HS mode, the external oscillator may require a start-up time considerably longer than the FSCM sample clock time; a false clock failure may be detected (see Figure 3-9). To prevent this, the internal oscillator is automatically configured as the system clock and functions until the external clock is stable (the OST has timed out). This is identical to Two-Speed Start-up mode. Once the external oscillator is stable, the LFINTOSC returns to its role as the FSCM source.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit (OSCCON<3>) to verify the oscillator start-up and system clock switchover has successfully completed.

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REGISTER 3-2: OSCCON: OSCILLATOR CONTROL REGISTER (ADDRESS: 8Fh)

U-0	R/W-1	R/W-1	R/W-0	R-q	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS[(1)]	HTS	LTS	SCS
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal Oscillator Frequency Select bits
- 000 = 31 kHz
- 001 = 125 kHz
- 010 = 250 kHz
- 011 = 500 kHz
- 100 = 1 MHz
- 101 = 2 MHz
- 110 = 4 MHz
- 111 = 8 MHz

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit[(1)]
- 1 = Device is running from the external system clock defined by FOSC<2:0>
- 0 = Device is running from the internal system clock (HFINTOSC or LFINTOSC)

bit 2 **HTS:** HFINTOSC (High Frequency – 8 MHz to 125 kHz) Status bit
- 1 = HFINTOSC is stable
- 0 = HFINTOSC is not stable

bit 1 **LTS:** LFINTOSC (Low Frequency – 31 kHz) Stable bit
- 1 = LFINTOSC is stable
- 0 = LFINTOSC is not stable

bit 0 **SCS:** System Clock Select bit
- 1 = Internal oscillator is used for system clock
- 0 = Clock source defined by FOSC<2:0>

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled, otherwise this bit resets to '1'.

Legend:	q = value depends on condition		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 3-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 q000	-110 q000
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
2007h[(1)]	CONFIG	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0', q = value depends on condition. Shaded cells are not used by oscillators.

Note 1: See Register 15-1 for operation of all Configuration Word bits.

NOTES:

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4.0 I/O PORTS

There are seventeen general purpose I/O pins and one input only pin available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Note:	Additional information on I/O ports may be found in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

4.1 PORTA and TRISA Registers

PORTA is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 4-2). Setting a TRISA bit (= `1`) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= `0`) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin). The exception is RA3, which is input only and its TRIS bit will always read as '`1`'. Example 4-1 shows how to initialize PORTA.

Reading the PORTA register (Register 4-1) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read; this value is modified and then written to the port data latch. RA3 reads '`0`' when MCLRE = `1`.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '`0`'.

When RA1 is configured as a voltage reference output, the RA1 digital output driver will automatically be disabled while not affecting the TRISA<1> value.

Note:	The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '`0`'.

EXAMPLE 4-1: INITIALIZING PORTA

```
BCF     STATUS,RP0   ;Bank 0
BCF     STATUS,RP1   ;
CLRF    PORTA        ;Init PORTA
MOVLW   F8h          ;Set RA<2:0> to
ANDWF   ANSEL0,f     ; digital I/O
BSF     STATUS,RP0   ;Bank 1
MOVLW   0Ch          ;Set RA<3:2> as inputs
MOVWF   TRISA        ; and set RA<5:4,1:0>
                     ; as outputs
BCF     STATUS,RP0   ;Bank 0
```

REGISTER 4-1: PORTA: PORTA REGISTER (ADDRESS: 05h, 105h)

U-0	U-0	R/W-x	R/W-x(1)	R/W-x	R/W-x(1)	R/W-x(1)	R/W-x(1)
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as '`0`'

bit 5-0 **RA<5:0>**: PORTA I/O Pin bits
`1` = Port pin is greater than V_{IH}
`0` = Port pin is less than V_{IL}

Note 1: Data latches are unknown after a POR, but each port bit reads '`0`' when the corresponding analog select bit is '`1`' (see Register 12-1).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-2: TRISA: PORTA TRI-STATE REGISTER (ADDRESS: 85h, 185h)

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISA5(2)	TRISA4(2)	TRISA3(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TRISA<5:0>:** PORTA Tri-State Control bit(1), (2)

1 = PORTA pin configured as an input (tri-stated)
0 = PORTA pin configured as an output

Note 1: TRISA<3> always reads '1'.

2: TRISA<5:4> always reads '1' in XT, HS and LP OSC modes.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2 Additional Pin Functions

Every PORTA pin on the PIC16F785/HV785 has an interrupt-on-change option and a weak pull-up option. The next three sections describe these functions.

4.2.1 WEAK PULL-UPS

Each of the PORTA pins has an individually configurable internal weak pull-up. Control bits WPUAx enable or disable each pull-up. Refer to Register 4-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the $\overline{\text{RAPU}}$ bit (OPTION_REG<7>). The weak pull-up on RA3 is automatically enabled when RA3 is configured as $\overline{\text{MCLR}}$.

REGISTER 4-3: WPUA: WEAK PULL-UP REGISTER (ADDRESS: 95h)(1), (2)

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	WPUA5(4)	WPUA4(4)	WPUA3(3)	WPUA2	WPUA1	WPUA0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUA<5:0>:** Weak Pull-up Register bits

1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{RAPU}}$ must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISA = 0).

3: The RA3 pull-up is automatically enabled when configured as $\overline{\text{MCLR}}$ in the Configuration Word.

4: WPUA<5:4> always reads '1' in XT, HS and LP OSC modes.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2.2 INTERRUPT-ON-CHANGE

Each of the PORTA pins is individually configurable as an interrupt-on-change pin. Control bits IOCAx enable or disable the interrupt function for each pin. Refer to Register 4-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of PORTA. The 'mismatch' outputs of the last read are OR'd together to set, the PORTA Change Interrupt flag bit (RAIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

a) Any read or write of PORTA. This will end the mismatch condition, then,

b) Clear the flag bit RAIF.

A mismatch condition will continue to set flag bit RAIF. Reading PORTA will end the mismatch condition and allow flag bit RAIF to be cleared. The latch holding the last read value is neither affected by an $\overline{MCLR}$ nor BOR Reset. After these resets, the RAIF flag will continue to be set if a mismatch is present.

Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

REGISTER 4-4: IOCA: INTERRUPT-ON-CHANGE PORTA REGISTER (ADDRESS: 96h)(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOCA5(2)	IOCA4(2)	IOCA3	IOCA2	IOCA1	IOCA0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCA<5:0>:** Interrupt-on-change PORTA Control bits(2)

1 = Interrupt-on-change enabled
0 = Interrupt-on-change disabled

Note 1: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOCA<5:4> always reads '1' in XT, HS and LP OSC modes.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.2.3 PORTA PIN DESCRIPTIONS AND DIAGRAMS

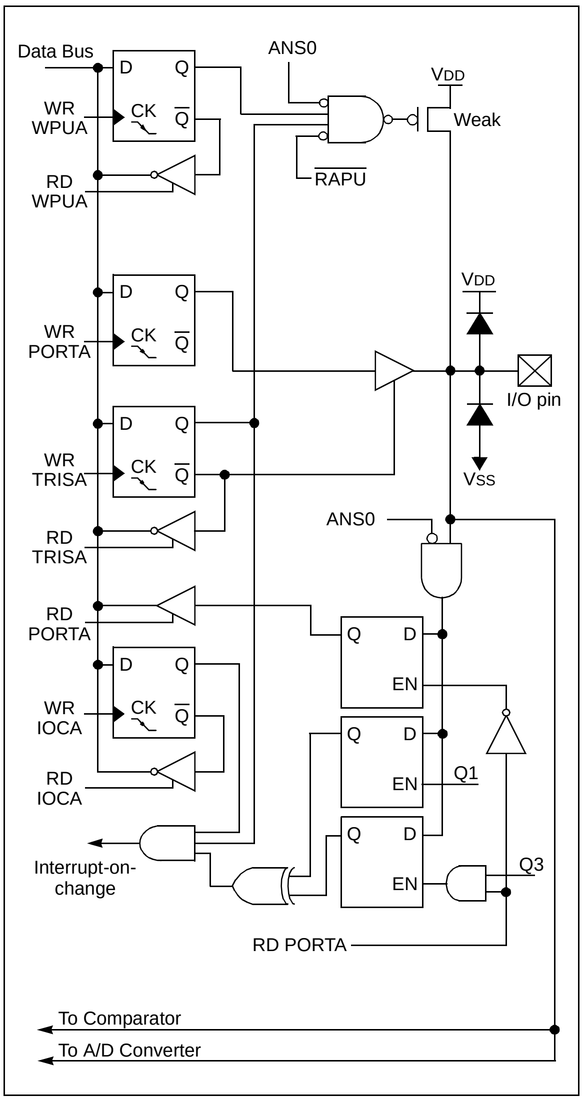
Each PORTA pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.

4.2.3.1 RA0/AN0/C1IN+/ICSPDAT

Figure 4-1 shows the diagram for this pin. The RA0 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- Analog input to Comparator 1
- In-Circuit Serial Programming™ data

FIGURE 4-1: BLOCK DIAGRAM OF RA0

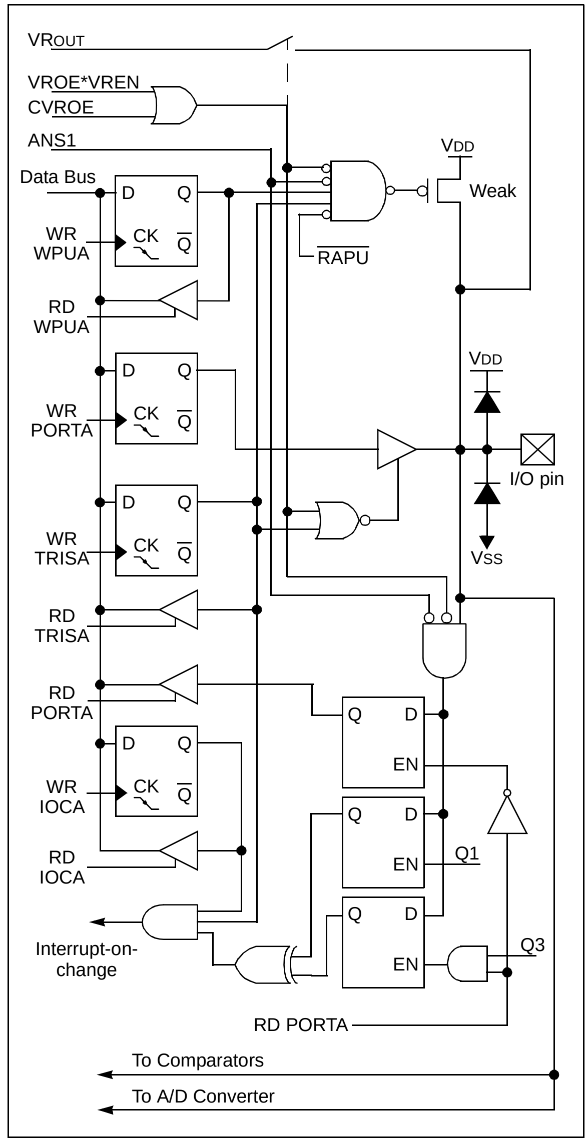


4.2.3.2 RA1/AN1/C12IN0-/VREF/ICSPCLK

Figure 4-1 shows the diagram for this pin. The RA1 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- Analog input to Comparators 1 and 2
- Voltage reference input for the A/D
- Buffered or unbuffered voltage reference output
- In-Circuit Serial Programming clock

FIGURE 4-2: BLOCK DIAGRAM OF RA1

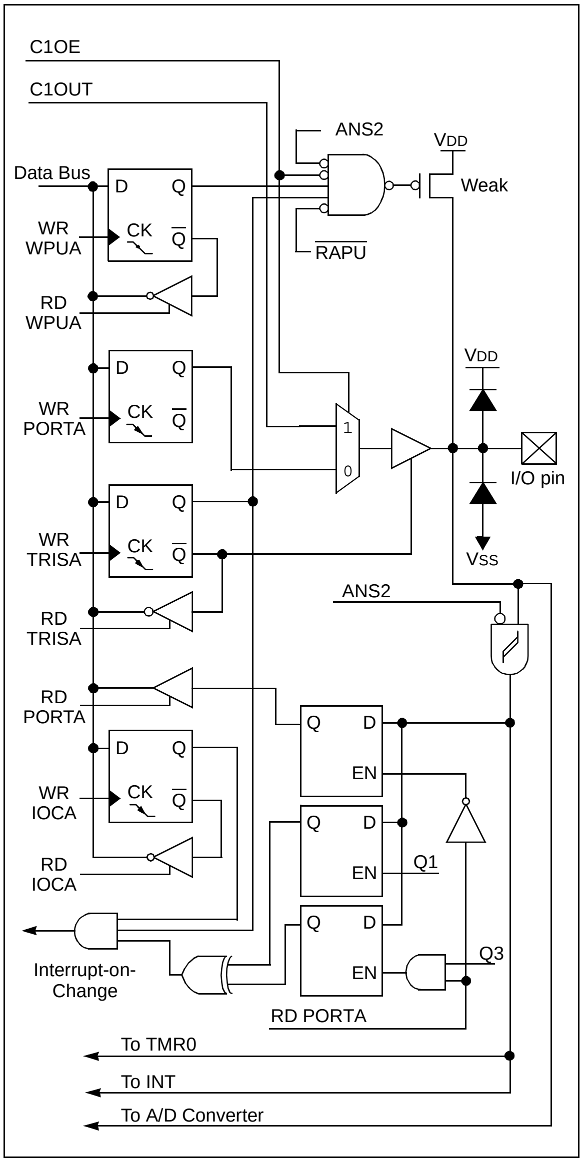


4.2.3.3 RA2/AN2/T0CKI/INT/C1OUT

Figure 4-3 shows the diagram for this pin. The RA2 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- Clock input for TMR0
- External edge triggered interrupt
- Digital output from Comparator 1

FIGURE 4-3: BLOCK DIAGRAM OF RA2

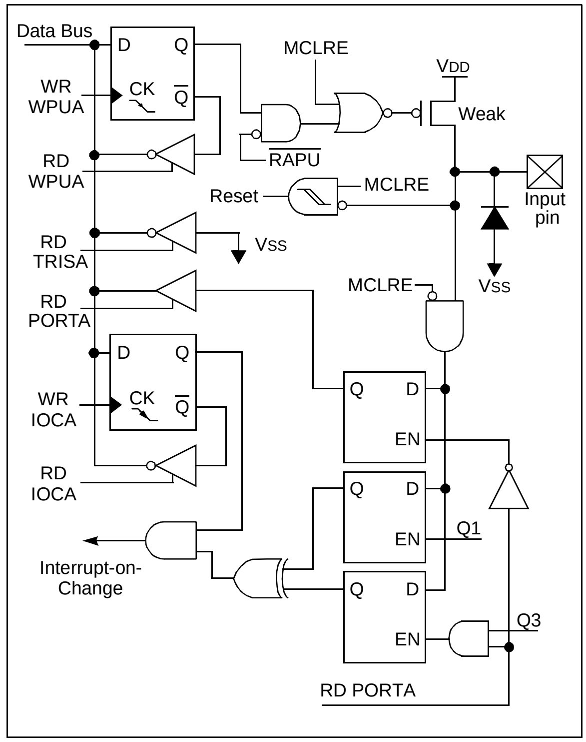


4.2.3.4 RA3/$\overline{\text{MCLR}}$/VPP

Figure 4-4 shows the diagram for this pin. The RA3 pin is configurable to function as one of the following:

- General purpose input
- Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF RA3

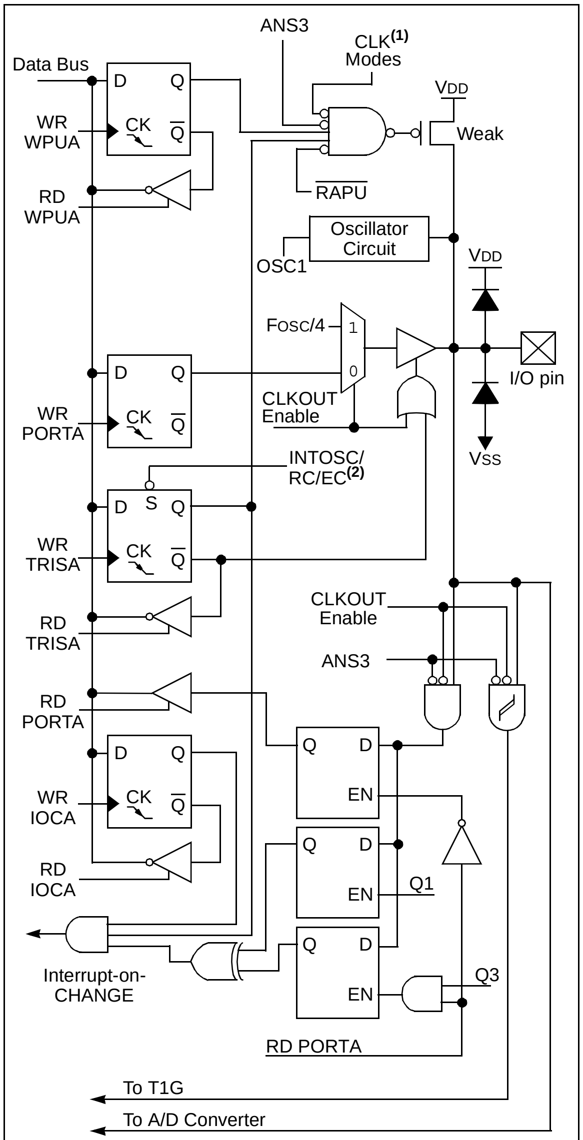


4.2.3.5 RA4/AN3/T1G/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- TMR1 gate input
- Crystal/resonator connection
- Clock output

FIGURE 4-5: BLOCK DIAGRAM OF RA4



Note 1: CLK modes are XT, HS, LP, LPTMR1 and CLKOUT Enable.

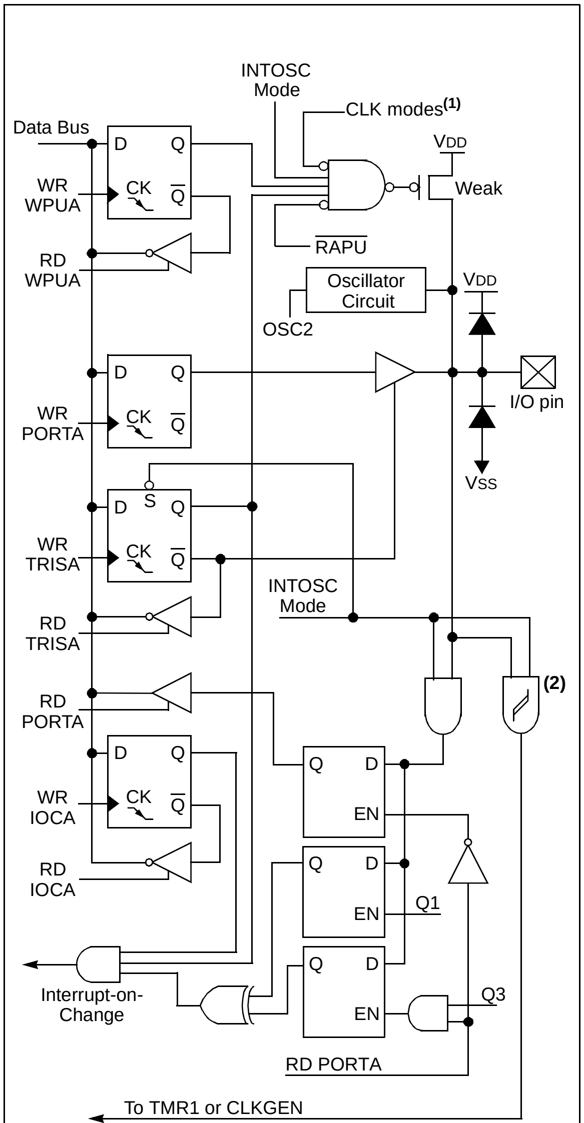
2: With CLKOUT option.

4.2.3.6 RA5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- General purpose I/O
- TMR1 clock input
- Crystal/resonator connection
- Clock input

FIGURE 4-6: BLOCK DIAGRAM OF RA5



Note 1: CLK modes are XT, HS, LP and LPTMR1.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
05h, 105h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	0000 0000
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
81h, 181h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h, 185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
95h	WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	--11 1111	--11 1111
96h	IOCA	—	—	IOCA5	IOCA4	IOCA3	IOCA2	IOCA1	IOCA0	--00 0000	--00 0000
98h	REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	--00 000-
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

4.3 PORTB and TRISB Registers

PORTB is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 4-6). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Example 4-2 shows how to initialize PORTB.

Reading the PORTB register (Register 4-5) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch.

Pin RB6 is an open drain output. All other PORTB pins have full CMOS output drivers.

The TRISB register controls the direction of the PORTB pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read ‘0’.

Note:	The ANSEL1 (93h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’.

EXAMPLE 4-2: INITIALIZING PORTB

```
BCF    STATUS,RP0    ;Bank 0
BCF    STATUS,RP1    ;
CLRF   PORTB         ;Init PORTB
BSF    STATUS,RP0    ;Bank 1
BCF    ANSEL1,2      ;digital I/O - RB4
BCF    ANSEL1,3      ;digital I/O - RB5
MOVLW  30h           ;Set RB<5:4> as inputs
MOVWF  TRISB         ;and set RB<7:6>
                     ;as outputs
BCF    STATUS,RP0    ;Bank 0
```

REGISTER 4-5: PORTB: PORTB REGISTER (ADDRESS: 06h, 106h)

R/W-x	R/W-x	R/W-x(1)	R/W-x(1)	U-0	U-0	U-0	U-0
RB7	RB6	RB5	RB4	—	—	—	—
bit 7							bit 0

bit 7-4 **RB<7:4>:** PORTB General Purpose I/O Pin bits
1 = Port pin is greater than V_{IH}
0 = Port pin is less than V_{IL}

bit 3-0 **Unimplemented**: Read as ‘0’

Note 1: Data latches are unknown after a POR, but each port bit reads ‘0’ when the corresponding analog select bit is ‘1’ (see Register 12-2 on page 82).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 4-6: TRISB: PORTB TRI-STATE REGISTER (ADDRESS: 86h, 186h)

R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0	U-0	U-0
TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—
bit 7							bit 0

bit 7-4 **TRISB<7:4>:** PORTB Tri-State Control bits
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

bit 3-0 **Unimplemented**: Read as ‘0’

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

4.3.1 PORTB PIN DESCRIPTIONS AND DIAGRAMS

Each PORTB pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the PWM, operational amplifier, or the A/D, refer to the appropriate section in this Data Sheet.

4.3.1.1 RB4/AN10/OP2-

The RB4/AN10/OP2- pin is configurable to function as one of the following:

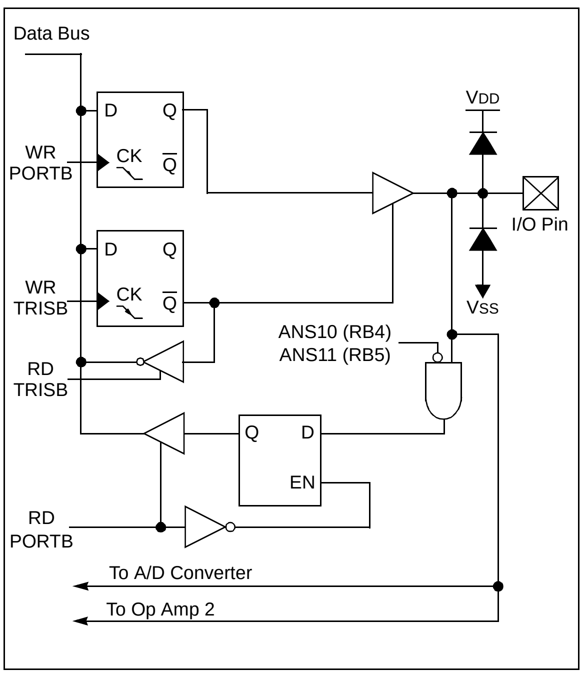
- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

4.3.1.2 RB5/AN11/OP2+

The RB5/AN11/OP2+ pin is configurable to function as one of the following:

- General purpose I/O
- Analog input to the A/D
- Analog input to Op Amp 2

FIGURE 4-7: BLOCK DIAGRAM OF RB4 AND RB5

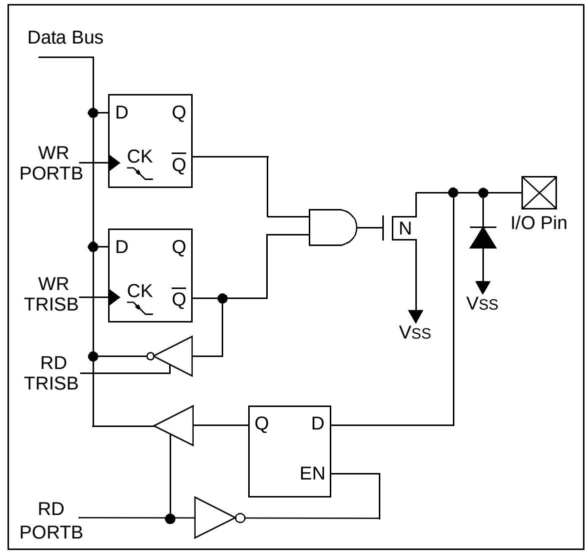


4.3.1.3 RB6

The RB6 pin is configurable to function as the following:

- Open drain general purpose I/O

FIGURE 4-8: BLOCK DIAGRAM OF RB6



4.3.1.4 RB7/SYNC

The RB7/SYNC pin is configurable to function as one of the following:

- General purpose I/O
- PWM synchronization input and output

FIGURE 4-9: BLOCK DIAGRAM OF RB7

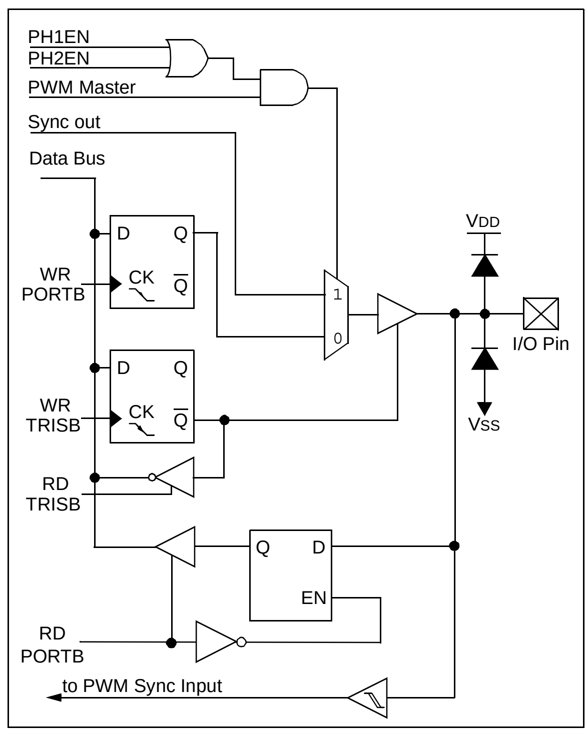


TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	uuuu ----
86h, 186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

4.4 PORTC and TRISC Registers

PORTC is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISC (Register 4-8). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin). Example 4-3 shows how to initialize PORTC.

Reading the PORTC register (Register 4-7) reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch.

The TRISC register controls the direction of the PORTC pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

When RC4 or RC5 is configured as an op amp output, the corresponding RC4 or RC5 digital output driver will automatically be disabled regardless of the TRISC<4> or TRISC<5> value.

Note:	The ANSEL0 (91h) and ANSEL1 (93h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-3: INITIALIZING PORTC

```
BCF     STATUS,RP0     ;Bank 0
BCF     STATUS,RP1
CLRF    PORTC          ;Init PORTC
BSF     STATUS,RP0     ;Bank 1
CLRF    ANSEL0         ;digital I/O
CLRF    ANSEL1         ;digital I/O
MOVLW   0Ch            ;Set RC<3:2> as inputs
MOVWF   TRISC          ; and set RC<5:4,1:0>
                       ; as outputs
BCF     STATUS,RP0     ;Bank 0
```

REGISTER 4-7: PORTC: PORTC REGISTER (ADDRESS: 07h, 107h)

R/W-x(1)	R/W-x(1)	R/W-x	R/W-x	R/W-x(1)	R/W-x(1)	R/W-x(1)	R/W-x(1)
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

bit 7-0 **RC<7:0>:** PORTC General Purpose I/O Pin bits
1 = Port pin is greater than V_{IH}
0 = Port pin is less than V_{IL}

Note 1: Data latches are unknown after a POR, but each port bit reads '0' when the corresponding analog select bit is '1' (see Registers 12-1 and 12-2 on page 82).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 4-8: TRISC: PORTC TRI-STATE REGISTER (ADDRESS: 87h, 187h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.4.1 PORTC PIN DESCRIPTIONS AND DIAGRAMS

Each PORTC pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.

4.4.1.1 RC0/AN4/C2IN+

The RC0 is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D Converter
- Non-inverting input to Comparator 2

4.4.1.2 RC6/AN8/OP1-

The RC6/AN8/OP1- pin is configurable to function as one of the following:

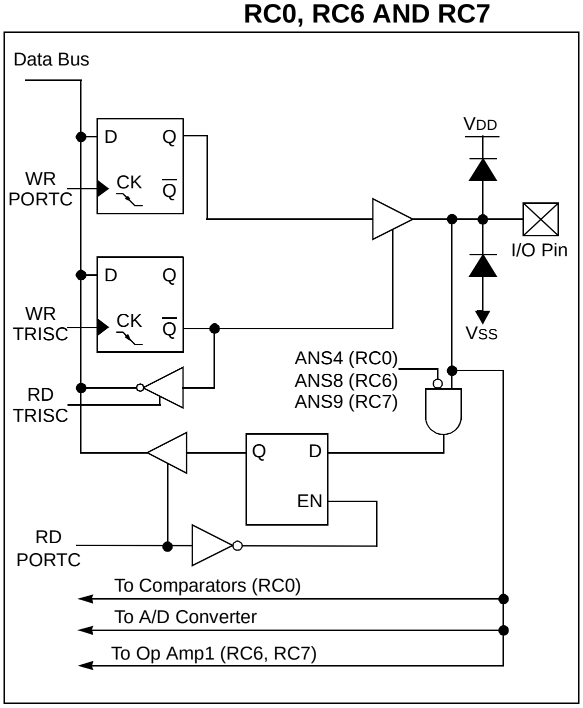
- General purpose I/O
- Analog input for the A/D
- Inverting input for Op Amp 1

4.4.1.3 RC7/AN9/OP1+

The RC7/AN9/OP1+ pin is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D
- Non-inverting input for Op Amp 1

FIGURE 4-10: BLOCK DIAGRAM OF RC0, RC6 AND RC7

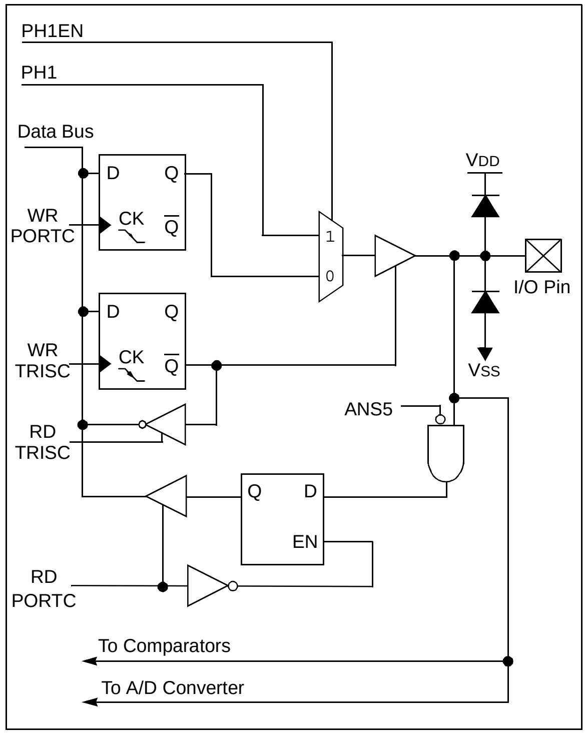


4.4.1.4 RC1/AN5/C12IN1-/PH1

The RC1 is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D Converter
- Analog input to Comparators 1 and 2
- Digital output from the Two-Phase PWM

FIGURE 4-11: BLOCK DIAGRAM OF RC1



4.4.1.5 RC2/AN6/C12IN2-/OP2

The RC2 is configurable to function as one of the following:

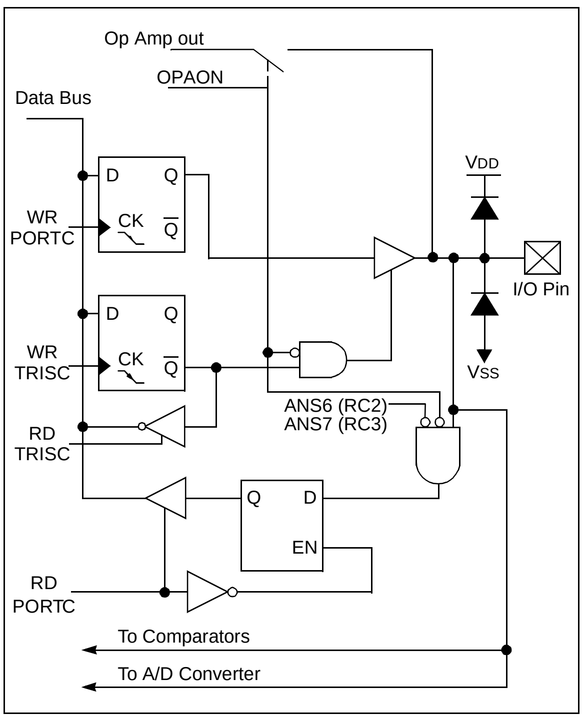
- General purpose I/O
- Analog input for the A/D Converter
- Analog input to Comparators 1 and 2
- Analog output from Op Amp 2

4.4.1.6 RC3/AN7/C12IN3-/OP1

The RC3 is configurable to function as one of the following:

- General purpose I/O
- Analog input for the A/D Converter
- Analog input to Comparators 1 and 2
- Analog output for Op Amp 1

FIGURE 4-12: BLOCK DIAGRAM OF RC2 AND RC3

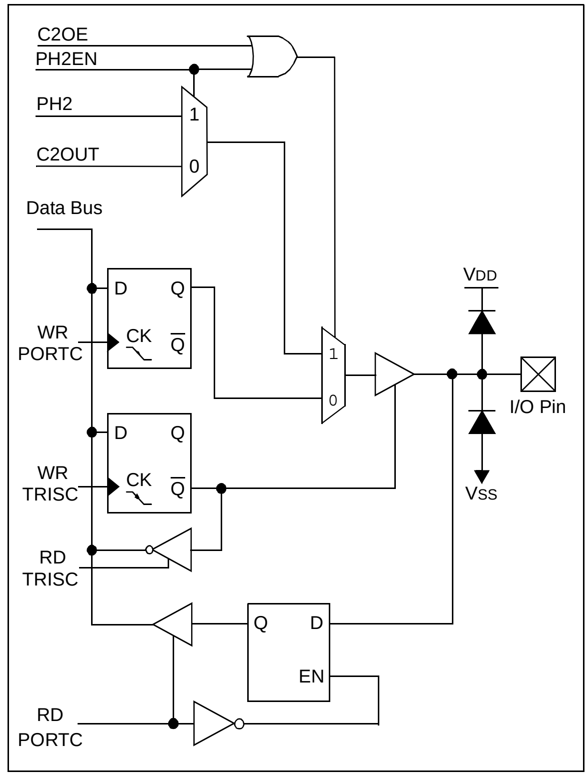


4.4.1.7 RC4/C2OUT/PH2

The RC4 is configurable to function as one of the following:

- General purpose I/O
- Digital output from Comparator 2
- Digital output from the Two-Phase PWM

FIGURE 4-13: BLOCK DIAGRAM OF RC4



4.4.1.8 RC5/CCP1

The RC5 is configurable to function as one of the following:

- General purpose I/O
- Digital input for the capture/compare
- Digital output for the CCP

FIGURE 4-14: BLOCK DIAGRAM OF RC5

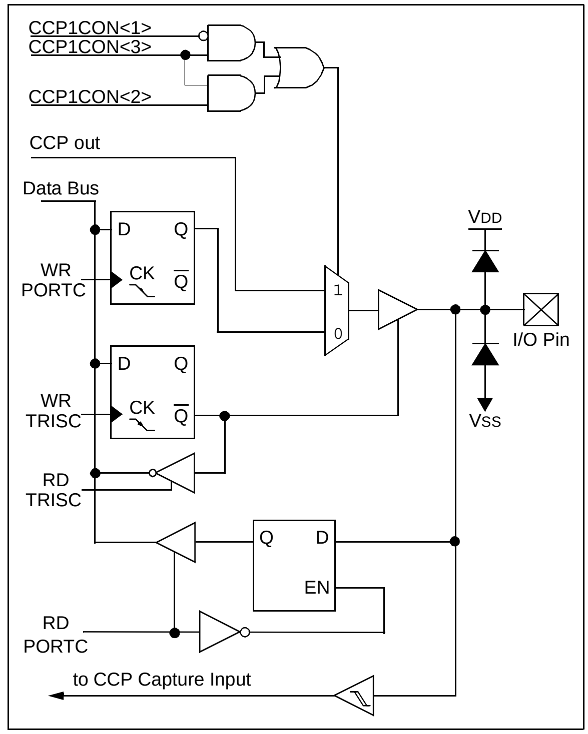


TABLE 4-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
07h, 107h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
87h, 187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
11Ch	OPA1CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	0--- ----	0--- ----

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

5.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 5-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note:	Additional information on the Timer0 module is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

5.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

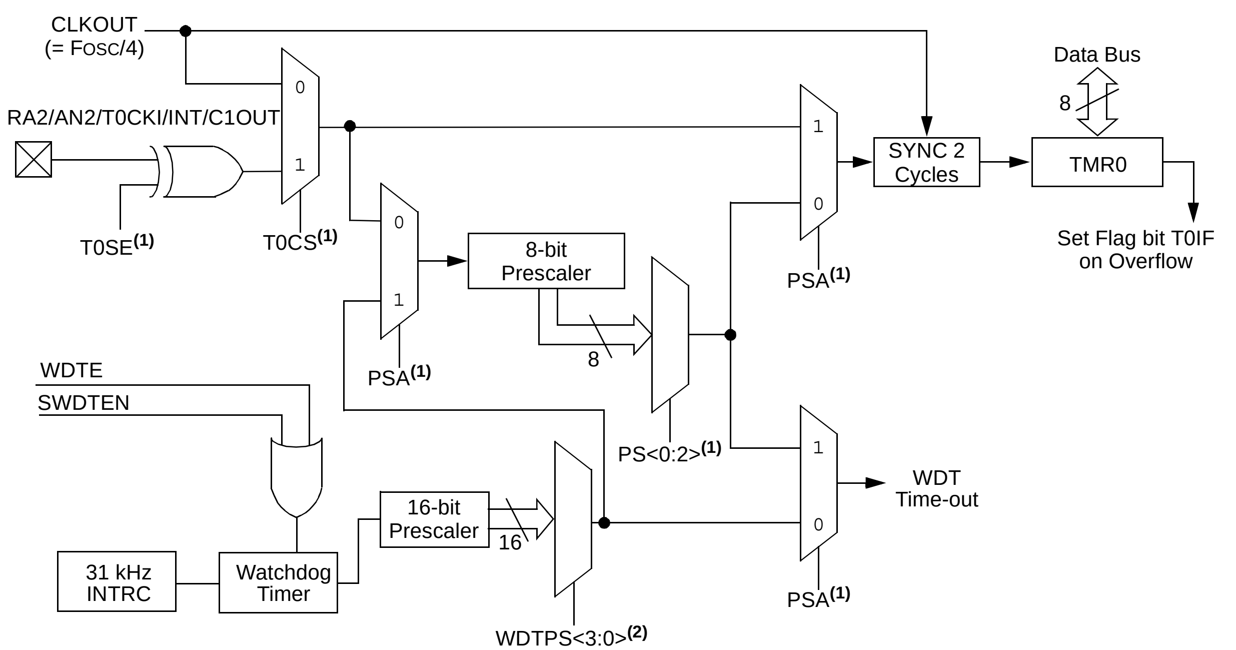
Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/AN2/T0CKI/INT/C1OUT. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note 1:	Counter mode has specific external clock requirements. Additional information on these requirements is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).
2:	The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

5.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit (INTCON<2>). The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep since the timer is shut-off during Sleep.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION_REG (see Register 2-2).
2: WDTPS<3:0> are bits in the WDTCON register (see Register 15-2).

5.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as "prescaler" throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS<2:0> bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x....etc.`) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer.

5.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 5-1 and Example 5-2) must be executed when changing the prescaler assignment between Timer0 and WDT.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF     STATUS,RP0      ;Bank 0
BCF     STATUS,RP1      ;
CLRWDT                  ;Clear WDT
CLRF    TMR0            ;Clear TMR0 and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1

MOVLW   b'00101111'     ;Required if desired
MOVWF   OPTION_REG      ; PS2:PS0 is
CLRWDT                  ; 000 or 001
                        ;
MOVLW   b'00101xxx'     ;Set postscaler to
MOVWF   OPTION_REG      ; desired WDT rate
BCF     STATUS,RP0      ;Bank 0
```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 5-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 5-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                  ;Clear WDT and
                        ; prescaler
BSF     STATUS,RP0      ;Bank 1
BCF     STATUS,RP1      ;

MOVLW   b'xxxx0xxx'     ;Select TMR0,
                        ; prescale, and
                        ; clock source
MOVWF   OPTION_REG      ;
BCF     STATUS,RP0      ;Bank 0
```

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
01h, 101h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
81h, 181h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
85h, 185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

6.0 TIMER1 MODULE WITH GATE CONTROL

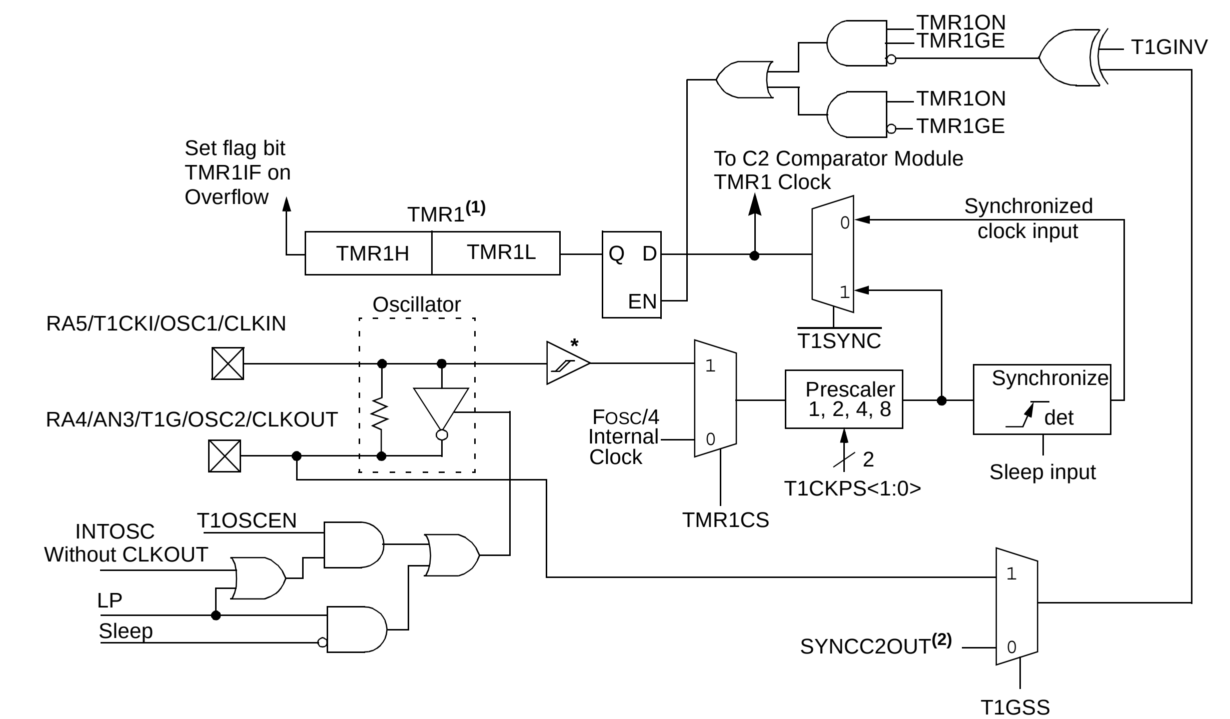
The Timer1 module is the 16-bit counter of the PIC16F785/HV785. Figure 6-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input:
  - Selectable gate source; T1G or C2 output (T1GSS)
  - Selectable gate polarity (T1GINV)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 6-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note:	Additional information on timer modules is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

FIGURE 6-1: TIMER1 ON THE PIC16F785/HV785 BLOCK DIAGRAM



* ST Buffer is low power type when using LP OSC, or high-speed type when using T1CKI.

Note 1: Timer1 increments on the rising edge.

2: SYNCC2OUT is the synchronized output from Comparator 2 (See Figure 9-2 on 66).

6.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:

- 16-bit Timer with prescaler
- 16-bit Synchronous counter
- 16-bit Asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the Timer1 gate, which can be selected as either the T1G pin or Comparator 2 output.

If an external clock oscillator is needed (and the microcontroller is using the LP oscillator or INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

> **Note:** In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after any one or more of the following conditions.
>
> - Timer1 enabled after POR Reset
> - Write to TMR1H or TMR1L
> - Timer1 is disabled (TMR1ON = `0`) when T1CKI is high then Timer1 is enabled (TMR1ON = `1`) when T1CKI is low. See Figure 6-2.

6.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 Interrupt Enable bit (PIE1<0>)
- PEIE bit (INTCON<6>)
- GIE bit (INTCON<7>)

The interrupt is cleared by clearing the TMR1IF in the Interrupt Service Routine.

> **Note:** The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

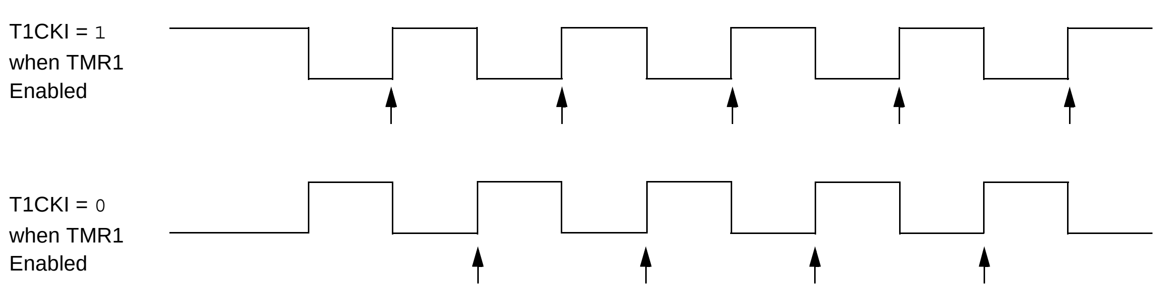
6.4 Timer1 Gate

Timer1 gate source is software configurable to be T1G pin or the output of Comparator 2. This allows the device to directly time external events using T1G or analog events using Comparator 2. See CM2CON1 (Register 9-3) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D Converter and many other applications. For more information on Delta-Sigma A/D Converters, see the Microchip web site (www.microchip.com).

> **Note:** TMR1GE bit (T1CON<6>) must be set to use either T1G or C2OUT as the Timer1 gate source. See Register 9-3 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit (T1CON<7>), whether it originates from the T1G pin or Comparator 2 output. This configures Timer1 to measure either the active high or active low time between events.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: See note box in **Section 6.1 “Timer1 Modes of Operation”**.

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS: 10h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV(1)	TMR1GE(2)	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **T1GINV:** Timer1 Gate Invert bit (1)
1 = Timer1 gate is high true (see bit 6)
0 = Timer1 gate is low true (see bit 6)

bit 6 **TMR1GE:** Timer1 Gate Enable bit (2)
If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 is on if Timer1 gate is true (see bit 7)
0 = Timer1 is on independent of Timer1 gate

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If System Clock is INTOSC without CLKOUT or LP mode:
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
Else:
This bit is ignored

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
1 = Do not synchronize external clock input
0 = Synchronize external clock input
TMR1CS = 0:
This bit is ignored. Timer1 uses the internal clock.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
1 = External clock from T1CKI pin (on the rising edge)
0 = Internal clock (FOSC/4)

bit 0 **TMR1ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.
2: TMR1GE bit must be set to use either T1G pin or C2OUT, as selected by T1GSS bit (CM2CON1<1>), as a Timer1 gate source.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (**Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	The ANSEL0 (91h) register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

6.6 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated for 32.768 kHz. It will continue to run during Sleep. It is primarily intended for a 32.768 kHz tuning fork crystal.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is also the LP oscillator or is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

Sleep mode will not disable the system clock when the system clock and Timer1 share the LP oscillator.

TRISA<5> and TRISA<4> bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA<5> and TRISA<4> bits read as '1'.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine (0004h) on an overflow. If the GIE bit is clear, execution will continue with the next instruction.

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

7.0 TIMER2 MODULE

The Timer2 module timer is an 8-bit timer with the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16 by `1`'s)
- Interrupt on TMR2 match with PR2

Timer2 has a control register shown in Register 7-1. TMR2 can be shut-off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption. Figure 7-1 is a simplified block diagram of the Timer2 module. The prescaler and postscaler selection of Timer2 are controlled by this register.

7.1 Timer2 Operation

Timer2 can be used as the PWM time base for the PWM mode of the CCP module. The TMR2 register is readable and writable, and is cleared on any device Reset. The input clock (FOSC/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS<1:0> (T2CON<1:0>). The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS: 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscale Select bits
`0000` = 1:1 Postscale
`0001` = 1:2 Postscale
•
•
•
`1111` = 1:16 Postscale

bit 2 **TMR2ON:** Timer2 On bit
`1` = Timer2 is on
`0` = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
`00` = Prescaler is 1
`01` = Prescaler is 4
`1x` = Prescaler is 16

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

7.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM

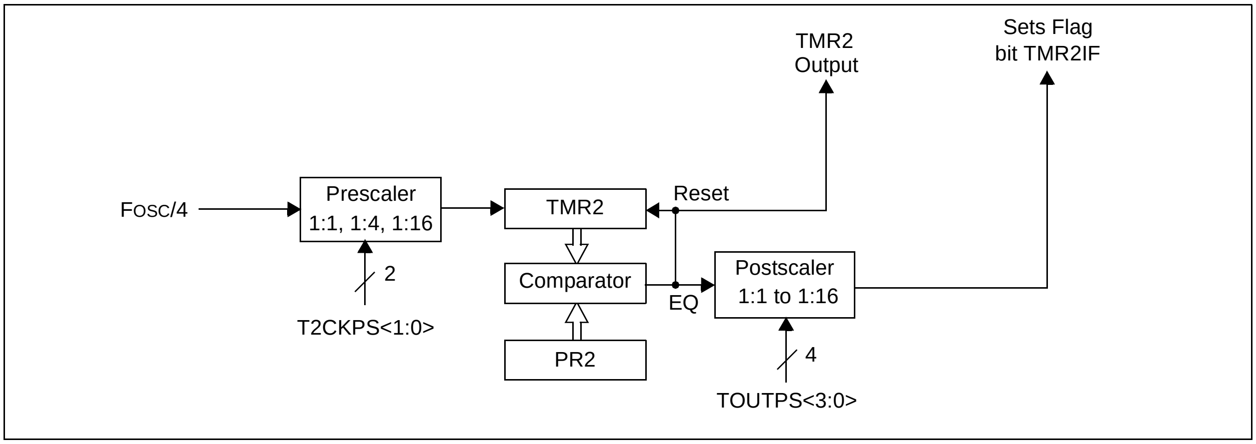


TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
11h	TMR2	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
92h	PR2	Timer2 Module Period register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, – = unimplemented, read as ‘0’. Shaded cells are not used by the Timer2 module.

8.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP. The special event trigger is generated by a compare match and will clear both TMR1H and TMR1L registers.

TABLE 8-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 8-1: CCP1CON: CCP OPERATION REGISTER (ADDRESS: 15h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as ‘0’.

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP Mode Select bits

`0000` = Capture/Compare/PWM off (resets CCP module)
`0001` = Unused (reserved)
`0010` = Compare mode, toggle output on match (CCP1IF bit is set)
`0011` = Unused (reserved)
`0100` = Capture mode, every falling edge
`0101` = Capture mode, every rising edge
`0110` = Capture mode, every 4th rising edge
`0111` = Capture mode, every 16th rising edge
`1000` = Compare mode, set output on match (CCP1IF bit is set)
`1001` = Compare mode, clear output on match (CCP1IF bit is set)
`1010` = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
`1011` = Compare mode, trigger special event (CCP1IF bit is set; TMR1 is reset, and A/D conversion is started if the A/D module is enabled. CCP1 pin is unaffected.)
`110x` = PWM mode: CCP1 output is high true.
`111x` = PWM mode: CCP1 output is low true.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

8.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC5/CCP1. An event is defined as one of the following and is configured by CCP1CON<3:0>:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

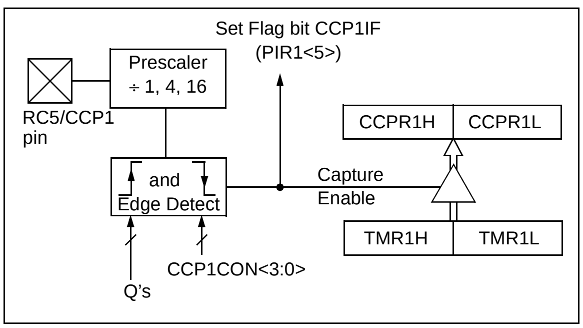
When a capture is made, the interrupt request flag bit CCP1IF (PIR1<5>) is set. The interrupt flag must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

8.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the RC5/CCP1 pin should be configured as an input by setting the TRISC<5> bit.

> **Note:** If the RC5/CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 8-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



8.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

8.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<5>) clear to avoid false interrupts and should clear the flag bit CCP1IF (PIR1<5>) following any such change in Operating mode.

8.1.4 CCP PRESCALER

There are four prescaler settings specified by bits CCP1M<3:0> (CCP1CON<3:0>). Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 8-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 8-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON     ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                    ; the new prescaler
                    ; move value and CCP ON
MOVWF   CCP1CON     ;Load CCP1CON with this
                    ; value
```

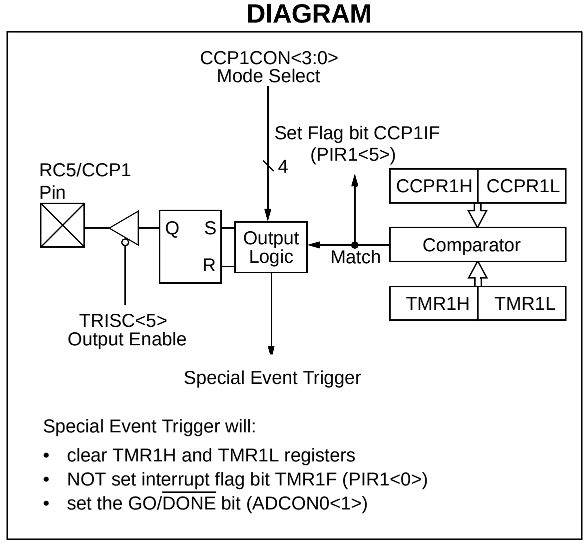
8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC5/CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M<3:0> (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF (PIR1<5>) is set.

FIGURE 8-2: COMPARE MODE OPERATION BLOCK DIAGRAM



8.2.1 CCP1 PIN CONFIGURATION

The user must configure the RC5/CCP1 pin as an output by clearing the TRISC<5> bit.

> **Note:** Clearing the CCP1CON register will force the RC5/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

8.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = `1010`), the RC5/CCP1 pin is not affected. The CCP1IF (PIR1<5>) bit is set, causing a CCP interrupt (if enabled). See Register 8-1.

8.2.4 SPECIAL EVENT TRIGGER

In this mode (CCP1M<3:0> = `1011`), an internal hardware trigger is generated, which may be used to initiate an action. See Register 8-1.

The special event trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the TMR1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1. The special event trigger output also starts an A/D conversion provided that the A/D module is enabled.

> **Note 1:** The special event trigger from the CCP module will not set interrupt flag bit TMR1IF (PIR1<0>).
>
> **2:** Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair between the clock edge that generates the special event trigger and the clock edge that generates the TMR1 Reset, will preclude the Reset from occurring.

TABLE 8-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
13h	CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
14h	CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
87h, 187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture, Compare or Timer1 module.

8.3 CCP PWM Mode

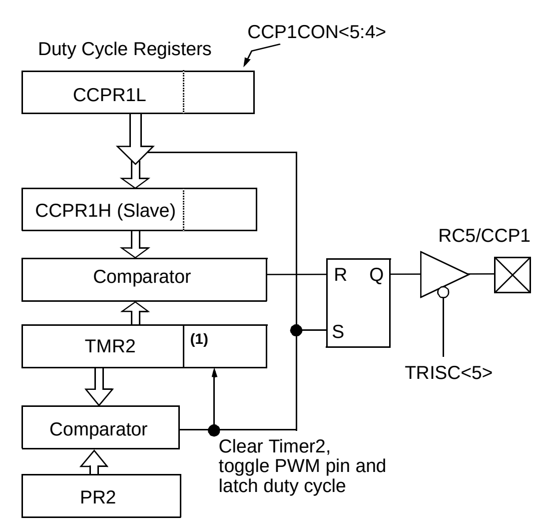
In Pulse Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the RC5/CCP1 pin. Since the RC5/CCP1 pin is multiplexed with the PORTC data latch, the TRISC<5> must be cleared to make the RC5/CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the PWM output latch to the default inactive levels. This is not the PORTC I/O data latch.

Figure 8-3 shows a simplified block diagram of PWM operation.

For a step by step procedure on how to set up the CCP module for PWM operation, see **Section 8.3.5 “Setup for PWM Operation”**.

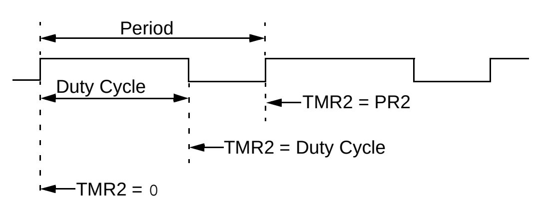
FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal Q clock, or 2 bits of the prescaler, to create the 10-bit time base.

The PWM output (Figure 8-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 8-4: CCP PWM OUTPUT



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the formula of Equation 8-1.

EQUATION 8-1: PWM PERIOD

$$PWM\ period = [(PR2) + 1] \bullet 4 \bullet T_{OSC} \bullet (TMR2\ prescale\ value)$$

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The RC5/CCP1 pin is set. (exception: if PWM duty cycle = 0%, the pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see **Section 7.1 “Timer2 Operation”**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the DC1B<1:0> (CCP1CON<5:4>) bits. Up to 10 bits of resolution is available. The CCPR1L contains the eight MSbs and the DC1B<1:0> contains the two LSbs. CCPR1L and DC1B<1:0> can be written to at any time. In PWM mode, CCPR1H is a read-only register. This 10-bit value is represented by CCPR1L (CCP1CON<5:4>).

Equation 8-2 is used to calculate the PWM duty cycle in time.

EQUATION 8-2: PWM DUTY CYCLE

$$PWM\ duty\ cycle = (CCPR1L{:}CCP1CON<5{:}4>) \bullet T_{OSC} \bullet (TMR2\ prescale\ value)$$

CCPR1L and DC1B<1:0> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e. the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

Because of the buffering, the module waits until the timer resets, instead of starting immediately. This means that enhanced PWM waveforms do not exactly match the standard PWM waveforms, but are instead offset by one full instruction cycle (4 T_{OSC}).

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the RC5/CCP1 pin is cleared.

The maximum PWM resolution is a function of PR2 as shown by Equation 8-3.

EQUATION 8-3: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

Note: If the PWM duty cycle value is longer than the PWM period, the assigned PWM pin(s) will remain unchanged.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (F_{OSC} = 20 MHz)

PWM Frequency	1.22 kHz(1)	4.88 kHz(1)	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

Note 1: Changing duty cycle will cause a glitch.

8.3.3 OPERATION IN SLEEP MODE

In Sleep mode, all clock sources are disabled. Timer2 will not increment and the state of the module will not change. If the RC5/CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state.

8.3.3.1 OPERATION WITH FAIL-SAFE CLOCK MONITOR

If the Fail-Safe Clock Monitor is enabled, a clock failure will force the CCP to be clocked from the internal oscillator clock source, which may have a different clock frequency than the primary clock.

See **Section 3.0 “Clock Sources”** for additional details.

8.3.4 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

8.3.5 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Configure the PWM pin (RC5/CCP1) as an input by setting the TRISC<5> bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and CCP1CON<5:4> bits.
5. Configure and start TMR2:
   - Clear the TMR2 interrupt flag bit by clearing the TMR2IF bit (PIR1<1>).
   - Set the TMR2 prescale value by loading the T2CKPS bits (T2CON<1:0>).
   - Enable Timer2 by setting the TMR2ON bit (T2CON<2>).
6. Enable PWM output after a new PWM cycle has started:
   - Wait until TMR2 overflows (TMR2IF bit is set).
   - Enable the RC5/CCP1 pin output by clearing the TRISC<5> bit.

TABLE 8-4: REGISTERS ASSOCIATED WITH CCP AND TIMER2

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
13h	CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
14h	CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0000 0000	0000 0000
87h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
92h	PR2	Timer2 Module Period Register								1111 1111	1111 1111

Legend: – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the CCP or Timer2 modules.

9.0 COMPARATOR MODULE

The Comparator module has two separate voltage comparators: Comparator 1 (C1) and Comparator 2 (C2).

Each comparator offers the following list of features:

- Control and Configuration register
- Comparator output available externally
- Programmable output polarity
- Interrupt-on-change flags
- Wake-up from Sleep
- Configurable as feedback input to the PWM
- Programmable four input multiplexer
- Programmable two input reference selections
- Programmable speed/power
- Output synchronization to Timer1 clock input (Comparator C2 only)

9.1 Control Registers

Both comparators have separate control and Configuration registers: CM1CON0 for C1 and CM2CON0 for C2. In addition, Comparator C2 has a second control register, CM2CON1, for synchronization control and simultaneous reading of both comparator outputs.

9.1.1 COMPARATOR C1 CONTROL REGISTER

The CM1CON0 register (shown in Register 9-1) contains the control and Status bits for the following:

- Comparator enable
- Comparator input selection
- Comparator reference selection
- Output mode
- Comparator speed

Setting C1ON (CM1CON0<7>) enables Comparator C1 for operation.

Bits C1CH<1:0> (CM1CON0<1:0>) select the comparator input from the four analog pins AN<7:5,1>.

> **Note:** To use AN<7:5,1> as analog inputs the appropriate bits must be programmed to '1' in the ANSEL0 register.

Setting C1R (CM1CON0<2>) selects the C1VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C1R selects the C1IN+ input on the RA0/AN0/C1IN+/ICSPDAT pin.

The output of the comparator is available internally via the C1OUT flag (CM1CON0<6>). To make the output available for an external connection, the C1OE bit (CM1CON0<5>) must be set.

The polarity of the comparator output can be inverted by setting the C1POL bit (CM1CON0<4>). Clearing C1POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

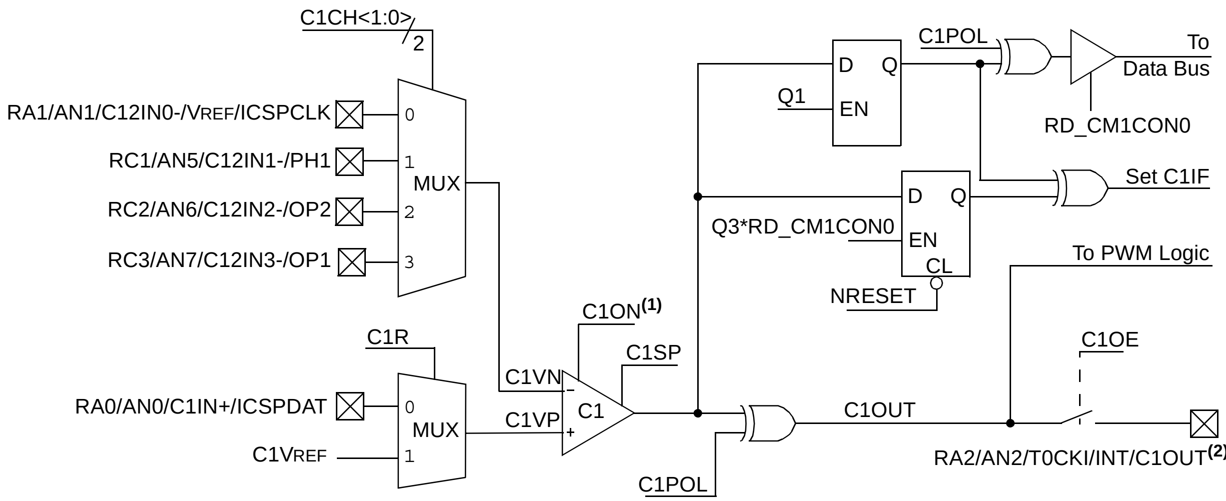
TABLE 9-1: C1 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C1POL	C1OUT
C1VN > C1VP	0	0
C1VN < C1VP	0	1
C1VN > C1VP	1	1
C1VN < C1VP	1	0

> **Note 1:** The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
>
> **2:** The C1 interrupt will operate correctly with C1OE set or cleared.
>
> **3:** To output C1 on RA2/AN2/T0CKI/INT/C1OUT:(C1OE = 1) and (C1ON = 1) and (TRISA<2> = 0).

C1SP (CM1CON0<3>) configures the speed of the comparator. When C1SP is set, the comparator operates at its normal speed. Clearing C1SP operates the comparator in a slower, low-power mode.

FIGURE 9-1: COMPARATOR C1 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C1ON = 0, the C1 comparator will produce a '0' output to the XOR Gate.

2: Output shown for reference only. For more detail, see Figure 4-3.

REGISTER 9-1: CM1CON0: COMPARATOR C1 CONTROL REGISTER 0 (ADDRESS: 119h)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0
bit 7							bit 0

bit 7 **C1ON:** Comparator C1 Enable bit
1 = C1 Comparator is enabled
0 = C1 Comparator is disabled

bit 6 **C1OUT:** Comparator C1 Output bit
If C1POL = 1 (inverted polarity):
C1OUT = 1, C1VP < C1VN
C1OUT = 0, C1VP > C1VN
If C1POL = 0 (non-inverted polarity):
C1OUT = 1, C1VP > C1VN
C1OUT = 0, C1VP < C1VN

bit 5 **C1OE:** Comparator C1 Output Enable bit
1 = C1OUT is present on the RA2/AN2/T0CKI/INT/C1OUT pin(1)
0 = C1OUT is internal only

bit 4 **C1POL:** Comparator C1 Output Polarity Select bit
1 = C1OUT logic is inverted
0 = C1OUT logic is not inverted

bit 3 **C1SP:** Comparator C1 Speed Select bit
1 = C1 operates in normal speed mode
0 = C1 operates in low-power, slow speed mode

bit 2 **C1R:** Comparator C1 Reference Select bit (non-inverting input)
1 = C1VP connects to C1VREF output
0 = C1VP connects to RA0/AN0/C1IN+/ICSPDAT

bit 1-0 **C1CH<1:0>:** Comparator C1 Channel Select bits
00 = C1VN of C1 connects to RA1/AN1/C12IN0-/VREF/ICSPCLK
01 = C1VN of C1 connects to RC1/AN5/C12IN1-/PH1
10 = C1VN of C1 connects to RC2/AN6/C12IN2-/OP2
11 = C1VN of C1 connects to RC3/AN7/C12IN3-/OP1

Note 1: C1OUT will only drive RA2/AN2/T0CKI/INT/C1OUT if: (C1OE = 1) and (C1ON = 1) and (TRISA<2> = 0).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

9.1.2 COMPARATOR C2 CONTROL REGISTERS

The CM2CON0 register is a functional copy of the CM1CON0 register described in **Section 9.1.1 "Comparator C1 Control Register"**. A second control register, CM2CON1, is also present for control of an additional synchronizing feature, as well as mirrors of both comparator outputs.

9.1.2.1 Control Register CM2CON0

The CM2CON0 register, shown in Register 9-2, contains the control and Status bits for Comparator C2.

Setting C2ON (CM2CON0<7>) enables Comparator C2 for operation.

Bits C2CH<1:0> (CM2CON0<1:0>) select the comparator input from the four analog pins, AN<7:5,1>.

Note:	To use AN<7:5,1> as analog inputs, the appropriate bits must be programmed to 1 in the ANSEL0 register.

C2R (CM2CON0<2>) selects the reference to be used with the comparator. Setting C2R (CM2CON0<2>) selects the C2VREF output of the comparator voltage reference module as the reference voltage for the comparator. Clearing C2R selects the C2IN+ input on the RC0/AN4/C2IN+ pin.

The output of the comparator is available internally via the C2OUT bit (CM2CON0<6>). To make the output available for an external connection, the C2OE bit (CM2CON0<5>) must be set.

The comparator output, C2OUT, can be inverted by setting the C2POL bit (CM2CON0<4>). Clearing C2POL results in a non-inverted output.

A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-2.

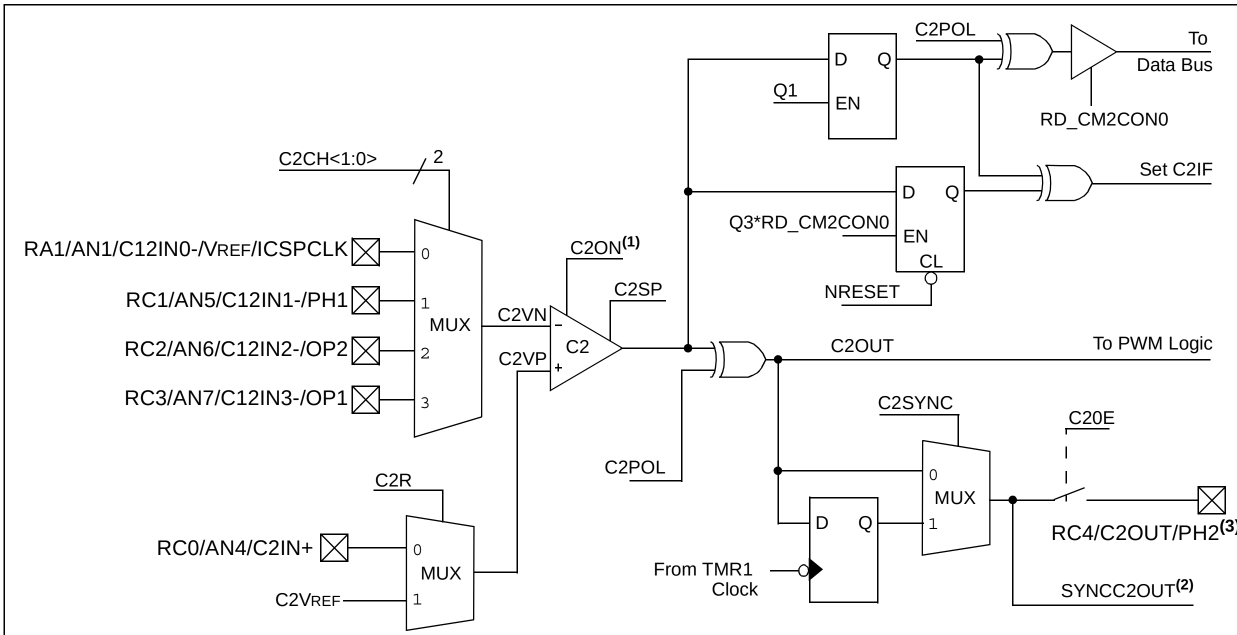
TABLE 9-2: C2 OUTPUT STATE VERSUS INPUT CONDITIONS

Input Condition	C2POL	C2OUT
C2VN > C2VP	0	0
C2VN < C2VP	0	1
C2VN > C2VP	1	1
C2VN < C2VP	1	0

Note 1:	The internal output of the comparator is latched at the end of each instruction cycle. External outputs are not latched.
2:	The C2 interrupt will operate correctly with C2OE set or cleared. An external output is not required for the C2 interrupt.
3:	For C2 output on RC4/C2OUT/PH2: (C2OE = 1) and (C2ON = 1) and (TRISA<4> = 0).

C2SP (CM2CON0<3>) configures the speed of the comparator. When C2SP is set, the comparator operates at its normal speed. Clearing C2SP operates the comparator in low-power mode.

FIGURE 9-2: COMPARATOR C2 SIMPLIFIED BLOCK DIAGRAM



Note 1: When C2ON = 0, the C2 comparator will produce a '0' output to the XOR Gate.
2: Timer1 gate control (see Figure 6-1).
3: Output shown for reference only. For more detail, see Figure 4-13.

REGISTER 9-2: CM2CON0: COMPARATOR C2 CONTROL REGISTER 0 (ADDRESS: 11Ah)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0
bit 7							bit 0

bit 7 **C2ON:** Comparator C2 Enable bit
1 = C2 Comparator is enabled
0 = C2 Comparator is disabled

bit 6 **C2OUT:** Comparator C2 Output bit
<u>If C2POL = 1 (inverted polarity):</u>
C2OUT = 1, C2VP < C2VN
C2OUT = 0, C2VP > C2VN
<u>If C2POL = 0 (non-inverted polarity):</u>
C2OUT = 1, C2VP > C2VN
C2OUT = 0, C2VP < C2VN

bit 5 **C2OE:** Comparator C2 Output Enable bit
1 = C2OUT is present on RC4/C2OUT/PH2[(1)]
0 = C2OUT is internal only

bit 4 **C2POL:** Comparator C2 Output Polarity Select bit
1 = C2OUT logic is inverted
0 = C2OUT logic is not inverted

bit 3 **C2SP:** Comparator C2 Speed Select bit
1 = C2 operates in normal speed mode
0 = C2 operates in low power, slow speed mode.

bit 2 **C2R:** Comparator C2 Reference Select bits (non-inverting input)
1 = C2VP connects to C2VREF
0 = C2VP connects to RC0/AN4/C2IN+

bit 1-0 **C2CH<1:0>:** Comparator C2 Channel Select bits
00 = C2VN of C2 connects to RA1/AN1/C12IN0-/VREF/ICSPCLK
01 = C2VN of C2 connects to RC1/AN5/C12IN1-/PH1
10 = C2VN of C2 connects to RC2/AN6/C12IN2-/OP2
11 = C2VN of C2 connects to RC3/AN7/C12IN3-/OP1

Note 1: C2OUT will only drive RC4/C2OUT/PH2 if: (C2OE = 1) and (C2ON = 1) and (TRISC<4> = 0).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.1.2.2 Control Register CM2CON1

Comparator C2 has one additional feature: its output can be synchronized to the Timer1 clock input. Setting C2SYNC (CM2CON1<0>) synchronizes the output of Comparator 2 to the falling edge of the Timer1 clock input (see Figure 9-2 and Register 9-3).

The CM2CON1 register also contains mirror copies of both comparator outputs, MC1OUT and MC2OUT (CM2CON1<7:6>). The ability to read both outputs simultaneously from a single register eliminates the timing skew of reading separate registers.

Note:	Obtaining the status of C1OUT or C2OUT by reading CM2CON1 does not affect the comparator interrupt mismatch registers.

REGISTER 9-3: CM2CON1: COMPARATOR C2 CONTROL REGISTER 1 (ADDRESS: 11Bh)

R-0	R-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC
bit 7							bit 0

bit 7 **MC1OUT**: Mirror Copy of C1OUT bit (CM1CON0<6>)

bit 6 **MC2OUT**: Mirror Copy of C2OUT bit (CM2CON0<6>)

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1 **T1GSS**: Timer1 Gate Source Select bit
1 = Timer1 gate source is RA4/AN3/T1G/OSC2/CLKOUT
0 = Timer1 gate source is SYNCC2OUT.

bit 0 **C2SYNC**: C2 Output Synchronous Mode bit
1 = C2 output is synchronous to falling edge of TMR1 clock
0 = C2 output is asynchronous

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

9.2 Comparator Outputs

The comparator outputs are read through the CM1CON0, COM2CON0 or CM2CON1 registers. CM1CON0 and CM2CON0 each contain the individual comparator output of Comparator 1 and Comparator 2, respectively. CM2CON2 contains a mirror copy of both comparator outputs facilitating a simultaneous read of both comparators. These bits are read-only. The comparator outputs may also be directly output to the RA2/AN2/T0CKI/INT/C1OUT and RC4/C2OUT/PH2 I/O pins. When enabled, multiplexers in the output path of the RA2 and RC4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 9-1 and Figure 9-2 show the output block diagrams for Comparators 1 and 2, respectively.

The TRIS bits will still function as an output enable/ disable for the RA2/AN2/T0CKI/INT/C1OUT and RC4/ C2OUT/PH2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C1POL and C2POL bits (CMxCON0<4>).

Timer1 gate source can be configured to use the T1G pin or Comparator 2 output as selected by the T1GSS bit (CM2CON1<1>). The Timer1 gate feature can be used to time the duration or interval of analog events. The output of Comparator 2 can also be synchronized with Timer1 by setting the C2SYNC bit (CM2CON1<0>). When enabled, the output of Comparator 2 is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, Comparator 2 is latched after the prescaler. To prevent a race condition, the Comparator 2 output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator 2 Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

It is recommended to synchronize Comparator 2 with Timer1 by setting the C2SYNC bit when Comparator 2 is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if Comparator 2 changes during an increment.

9.3 Comparator Interrupts

The comparator interrupt flags are set whenever there is a change in the output value of its respective comparator. Software will need to maintain information about the status of the output bits, as read from CM2CON0<7:6>, to determine the actual change that has occurred. The CxIF bits, PIR1<4:3>, are the Comparator Interrupt Flags. Each comparator interrupt bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CxIE bits (PIE1<4:3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupts. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CxIF bits will still be set if an interrupt condition occurs.

The comparator interrupt of the PIC16F785/HV785 differs from previous designs in that the interrupt flag is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMxCON0 register to clear the mismatch registers. When the mismatch registers are not cleared, an interrupt will not occur when the comparator output returns to the previous state. When the mismatch registers are cleared, an interrupt will occur when the comparator returns to the previous state.

> **Note 1:** If a change in the CMxCON0 register (CxOUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CxIF (PIR1<4:3>) interrupt flag may not get set.
>
> **2:** When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μs for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.4 Effects of Reset

A Reset forces all registers to their Reset state. This disables both comparators.

10.0 VOLTAGE REFERENCES

There are two voltage references available in the PIC16F785/HV785: The voltage referred to as the comparator reference (CVREF) is a variable voltage based on VDD; The voltage referred to as the VR reference (VR) is a fixed voltage derived from a stable band gap source. Each source may be individually routed internally to the comparators or output, buffered or unbuffered, on the RA1/AN1/C12IN0-/VREF/ICSPCLK pin.

10.1 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The VRCON register (Register 10-1) controls the voltage reference module shown in Figure 10-1.

10.1.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equation determines the output voltages:

EQUATION 10-1: CVREF OUTPUT VOLTAGE

$V_{RR} = 1$ (low range):

$$CV_{REF} = VR<3:0> \times V_{DD}/24$$

$V_{RR} = 0$ (high range):

$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

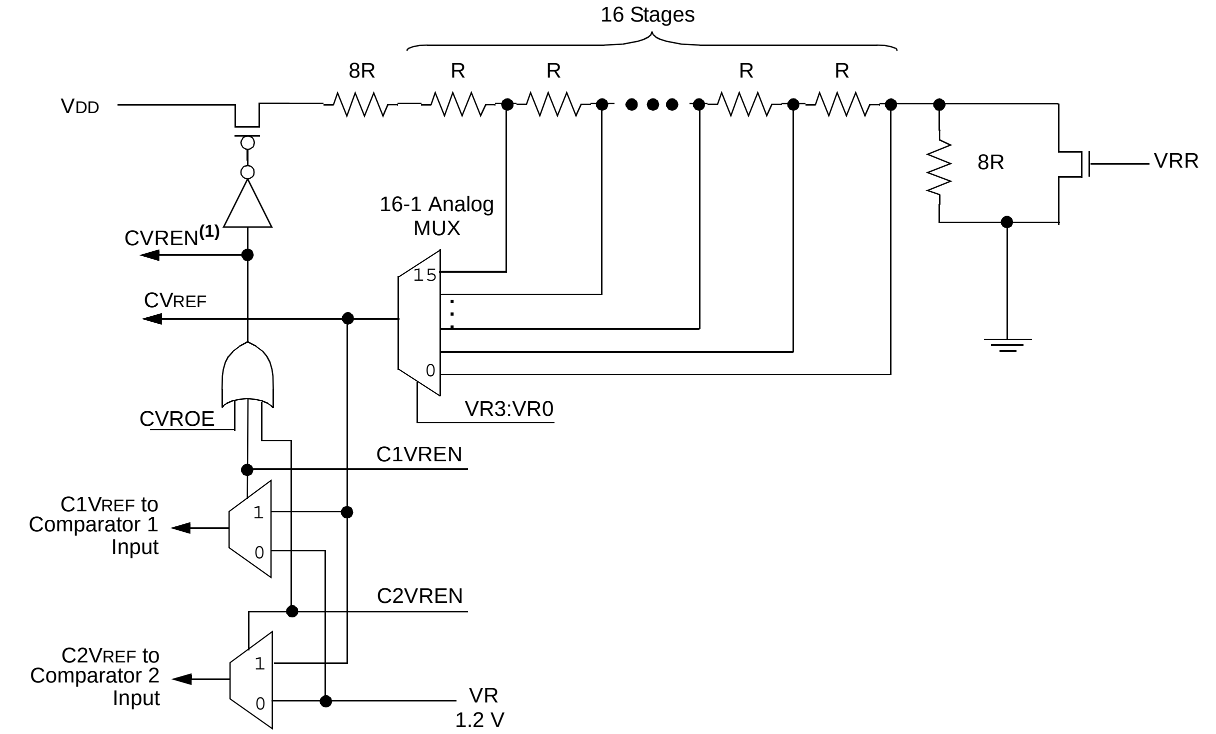
10.1.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 10-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing all CVROE, C1VREN and C2VREN bits. When disabled, the reference voltage is VSS when VR<3:0> is '0000' and the VRR (VRCON<5>) bit is set. This allows the comparators to detect a zero-crossing and not consume CVREF module current.

The voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in Table 19-8.

 Preliminary

FIGURE 10-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: See Register 10-1, bits 3-0.

REGISTER 10-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 99h)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
C1VREN(1)	C2VREN(1)	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

bit 7 **C1VREN**: Comparator 1 Voltage Reference Enable bit(1)
1 = CVREF circuit powered on and routed to C1VREF input of comparator 1
0 = 1.2 Volt VR routed to C1VREF input of comparator 1

bit 6 **C2VREN**: Comparator 2 Voltage Reference Enable bit(1)
1 = CVREF circuit powered on and routed to C2VREF input of comparator 2
0 = 1.2 Volt VR routed to C2VREF input of comparator 2

bit 5 **VRR**: Comparator Voltage Reference CVREF Range Selection bit
1 = Low Range
0 = High Range

bit 4 **Unimplemented**: Read as '0'

bit 3-0 **VR<3:0>**: Comparator Voltage Reference CVREF Value Selection 0 ≤ VR<3:0> ≤ 15
When VRR = 1 and CVREN = 1: CVREF = (VR<3:0> x VDD/24)
When VRR = 0 and CVREN = 1: CVREF = (VDD/4) + (VR<3:0> x VDD/32)
When CxVREN = 0 and VREN = 1: CxVREF = 1.2V from VR module

Note 1: When C1VREN, C2VREN and CVROE (Register 10-2) are all low, the CVREF circuit is powered down and does not contribute to IDD current.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = bit is set	'0' = bit is cleared	x = bit is unknown

10.2 VR Reference Module

The VR Reference module generates a 1.2V nominal output voltage for use by the ADC and comparators. The output voltage can also be brought out to the VREF pin for user applications. This module uses a bandgap as a reference. See Table 19-9 for detailed specifications. Register 10-2 shows the control register for the VR module.

REGISTER 10-2: REFCON: VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 98h)

U-0	U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	BGST	VRBB	VREN	VROE	CVROE	—
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **BGST:** Band Gap Reference Voltage Stable Flag bit
1 = Reference is stable
0 = Reference is not stable

bit 4 **VRBB:** Voltage Reference Buffer Bypass bit
1 = VREF output is not buffered. Power is removed from buffer amplifier.
0 = VREF output is buffered(1)

bit 3 **VREN:** Voltage Reference Enable bit (VR = 1.2V nominal)(2)
1 = VR reference is enabled
0 = VR reference is disabled and does not consume any current

bit 2 **VROE:** Voltage Reference Output Enable bit
<u>If CVROE = 0:</u>
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is 1.2 volt VR analog reference
0 = Disabled, 1.2 volt VR analog reference is used internally only
<u>If CVROE = 1:</u>
VROE has no effect.

bit 1 **CVROE**: Comparator Voltage Reference Output Enable bit (see Figure 10-2)
1 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is CVREF voltage
0 = VREF output on RA1/AN1/C12IN0-/VREF/ICSPCLK pin is controlled by VROE

bit 0 **Unimplemented:** Read as '0'

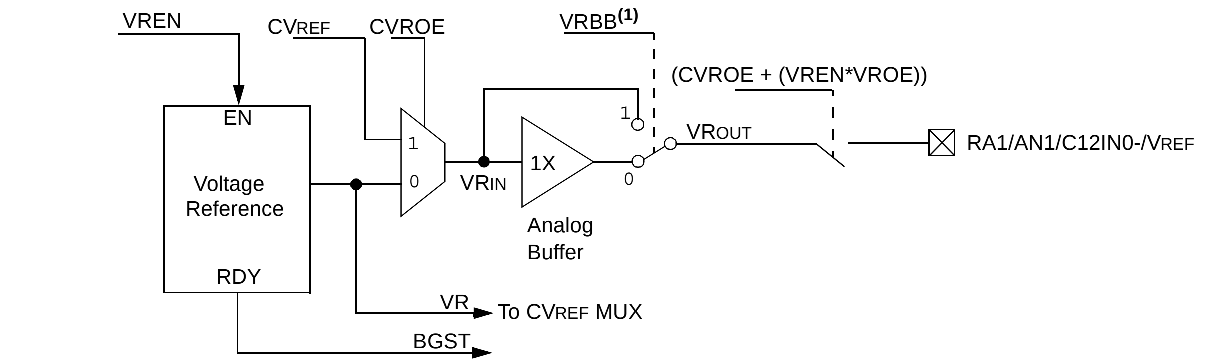
Note 1: Buffer amplifier common mode limitations require VREF ≤ (VDD - 1.4)V for buffered output.
2: VREN is fixed high for PIC16HV785 device.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

10.2.1 VR STABILIZATION PERIOD

When the Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 19.0 “Electrical Specifications”** for the minimum delay requirement.

FIGURE 10-2: VR REFERENCE BLOCK DIAGRAM



Note 1: Buffered output requires VRIN = (VDD - 1.4)V.
2: VREN is fixed high for PIC16HV785 device.

TABLE 10-1: REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
11Bh	CM2CON1	MC1OUT	MC2OUT	—	—	—	—	T1GSS	C2SYNC	00-- --10	00-- --10
85h, 185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
87h, 187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
05h, 105h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
07h, 107h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 ---0	0000 ---0
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 ---0	0000 ---0
98h	REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	--00 000-
99h	VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as ‘0’. Shaded cells are not used for comparator.

NOTES:

11.0 OPERATIONAL AMPLIFIER (OPA) MODULE

The OPA module has the following features:

- Two independent Operational Amplifiers
- External connections to all ports
- 3 MHz Gain Bandwidth Product (GBWP)

11.1 Control Registers

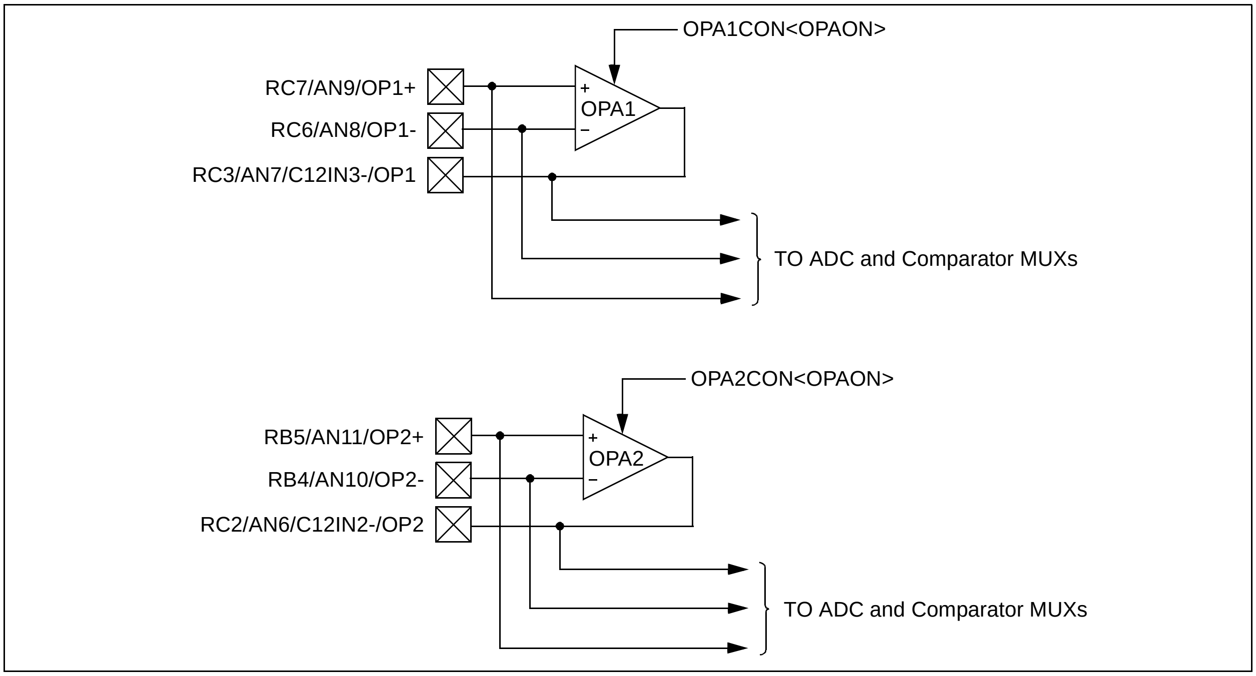
The OPA1CON register, shown in Register 11-1, controls OPA1. OPA2CON, shown in Register 11-2, controls OPA2.

11.2 OPAxCON Register

The OPA module is enabled by setting the OPAON bit (OPAxCON<7>). When enabled, OPAON forces the output driver of RC3/AN7/C12IN3-/OP1 for OPA1, and RC2/AN6/C12IN2-/OP2 for OPA2, into tri-state to prevent contention between the driver and the OPA output.

Note:	When OPA1 or OPA2 is enabled, the RC3/AN7/C12IN3-/OP1 pin, or RC2/AN6/C12IN2-/OP2 pin, respectively, is driven by the op amp output, not by the PORTC driver. Refer to Table 19-11 for the electrical specifications for the op amp output drive capability.

FIGURE 11-1: OPA MODULE BLOCK DIAGRAM



REGISTER 11-1: OPA1CON: OP AMP 1 CONTROL REGISTER (ADDRESS: 11Ch)

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
OPAON	—	—	—	—	—	—	—
bit 7							bit 0

bit 7 **OPAON:** Op Amp Enable bit
1 = Op Amp 1 is enabled
0 = Op Amp 1 is disabled

bit 6-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 11-2: OPA2CON: OP AMP 2 CONTROL REGISTER (ADDRESS: 11Dh)

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
OPAON	—	—	—	—	—	—	—
bit 7							bit 0

bit 7 **OPAON:** Op Amp Enable bit
1 = Op Amp 2 is enabled
0 = Op Amp 2 is disabled

bit 6-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

11.3 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables both op amps.

11.4 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product (GBWP)

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.4V. Behavior for common mode voltages greater than V_{DD}-1.4V, or below 0V, are beyond the normal operating range.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the common mode voltage.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB.

11.5 Effects of Sleep

When enabled, the op amps continue to operate and consume current while the processor is in Sleep mode.

TABLE 11-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
11Ch	OPA1CON	OPAON	—	—	—	—	—	—	—	`0--- ----`	`0--- ----`
11Dh	OPA2CON	OPAON	—	—	—	—	—	—	—	`0--- ----`	`0--- ----`
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	`1111 1111`	`1111 1111`
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	`---- 1111`	`---- 1111`
86h, 186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	`1111 ----`	`1111 ----`
87h, 187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	`1111 1111`	`1111 1111`

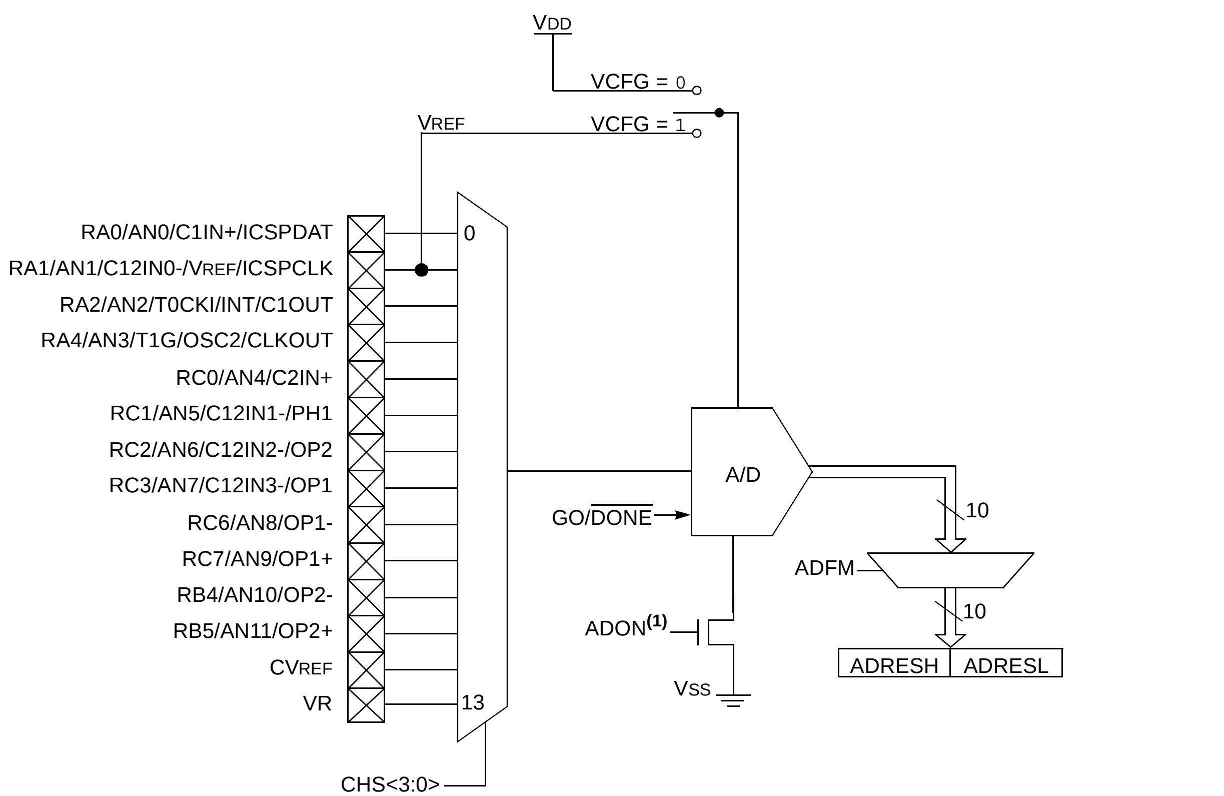
Legend: `x` = unknown, `u` = unchanged, `-` = unimplemented, read as '`0`'. Shaded cells are not used for the OPA module.

NOTES:

12.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC16F785/HV785 has twelve analog I/O inputs, plus two internal inputs, multiplexed into one sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 12-1 shows the block diagram of the A/D on the PIC16F785/HV785.

FIGURE 12-1: A/D BLOCK DIAGRAM



Note 1: When ADON = 0 all input channels are disconnected from ADC (no loading).

12.1 A/D Configuration and Operation

There are four registers available to control the functionality of the A/D module:

1. ANSEL0 (Register 12-1)
2. ANSEL1 (Register 12-2)
3. ADCON0 (Register 12-3)
4. ADCON1 (Register 12-4)

12.1.1 ANALOG PORT PINS

The ANS<11:0> bits (ANSEL1<3:0> and ANSEL0<7:0>) and the TRISA<4,2:0>, TRISB<5:4> and TRISC<7:6,3:0>> bits control the operation of the A/D port pins. Set the corresponding TRISx bits to '1' to set the pin output driver to its high-impedance state. Likewise, set the corresponding ANSx bit to disable the digital input buffer.

Note:	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

12.1.2 CHANNEL SELECTION

There are fourteen analog channels on the PIC16F785/HV785. The CHS<3:0> bits (ADCON0<5:2>) control which channel is connected to the sample and hold circuit.

12.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either VDD is used or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>) controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference.

12.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ADCON1<6:4>). There are seven possible clock options:

- FOSC/2
- FOSC/4
- FOSC/8
- FOSC/16
- FOSC/32
- FOSC/64
- FRC (dedicated internal oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 μs. Table 12-1 shows a few TAD calculations for selected frequencies.

TABLE 12-1: TAD VS. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Device Frequency			
Operation	**ADCS2:ADCS0**	**20 MHz**	**5 MHz**	**4 MHz**	**1.25 MHz**
2 TOSC	`000`	100 ns(2)	400 ns(2)	500 ns(2)	1.6 μs
4 TOSC	`100`	200 ns(2)	800 ns(2)	1.0 μs(2)	3.2 μs
8 TOSC	`001`	400 ns(2)	1.6 μs	2.0 μs	6.4 μs
16 TOSC	`101`	800 ns(2)	3.2 μs	4.0 μs	12.8 μs(3)
32 TOSC	`010`	1.6 μs	6.4 μs	8.0 μs(3)	25.6 μs(3)
64 TOSC	`110`	3.2 μs	12.8 μs(3)	16.0 μs(3)	51.2 μs(3)
A/D RC	`x11`	2-6 μs(1), (4)	2-6 μs(1), (4)	2-6 μs(1), (4)	2-6 μs(1), (4)

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 μs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during Sleep.

12.1.5 STARTING A CONVERSION

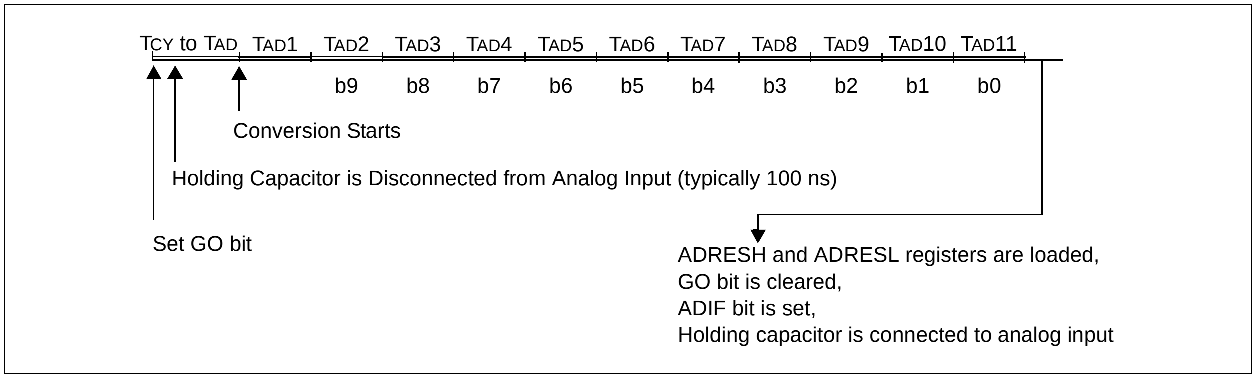
The A/D conversion is initiated by setting the GO/$\overline{\text{DONE}}$ bit (ADCON0<1>). When the conversion is complete, the A/D module:

- Clears the GO/$\overline{\text{DONE}}$ bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled)

If the conversion must be aborted, the GO/$\overline{\text{DONE}}$ bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the previous conversion. After an aborted conversion, a 2 TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

> **Note:** The GO/$\overline{\text{DONE}}$ bit should not be set in the same instruction that turns on the A/D.

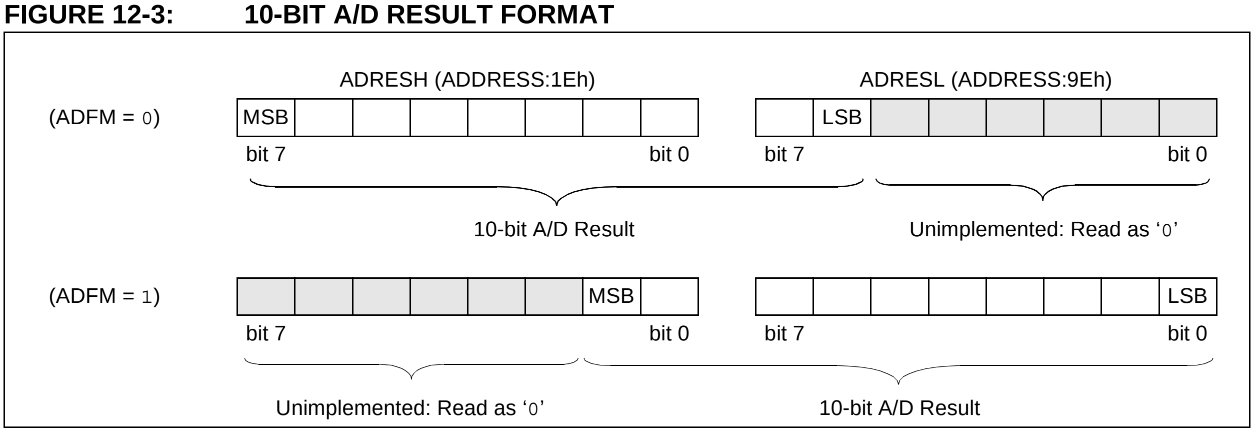
FIGURE 12-2: A/D CONVERSION TAD CYCLES



12.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right justified. The ADFM bit (ADCON0<7>) controls the output format. Figure 12-3 shows the output formats.

FIGURE 12-3: 10-BIT A/D RESULT FORMAT



REGISTER 12-1: ANSEL0: ANALOG SELECT REGISTER (ADDRESS: 91h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0

bit 7 bit 0

bit 7-0 **ANS<7:0>**: Analog Select bits

Analog select between analog or digital function on pins AN<7:0>, respectively.

`1` = Analog input. Pin is assigned as analog input.(1)

`0` = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin. Port reads of pins configured assigned as analog inputs will read as '`0`'.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 12-2: ANSEL1: ANALOG SELECT REGISTER (ADDRESS: 93h)

U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ANS11	ANS10	ANS9	ANS8

bit 7 bit 0

bit 7-4 **Unimplemented:** Read as '`0`'

bit 3-0 **ANS<11:8>**: Analog Select bits

Analog select between analog or digital function on pins AN<11:8>, respectively.

`1` = Analog input. Pin is assigned as analog input.(1)

`0` = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin. Port reads of pins assigned as analog inputs will read as '`0`'.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 12-2: ANALOG SELECT CROSS REFERENCE

Mode	Reference											
Analog Select	ANS11	ANS10	ANS9	ANS8	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
Analog Channel	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
I/O Pin	RB5	RB4	RC7	RC6	RC3	RC2	RC1	RC0	RA4	RA2	RA1	RA0

REGISTER 12-3: ADCON0: A/D CONTROL REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

bit 7 **ADFM:** A/D Result Formed Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG**: Voltage Reference bit
1 = VREF pin
0 = VDD

bit 5-2 **CHS<3:0>:** Analog Channel Select bits
0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)
0110 = Channel 06 (AN6)
0111 = Channel 07 (AN7)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = CVREF
1101 = VR
1110 = Reserved. Do not use.
1111 = Reserved. Do not use.

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** A/D Enable bit
1 = A/D converter module is enabled
0 = A/D converter is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 12-4: ADCON1: A/D CONTROL REGISTER 1 (ADDRESS: 9Fh)

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	ADCS2	ADCS1	ADCS0	—	—	—	—
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = FOSC/2
001 = FOSC/8
010 = FOSC/32
x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)
100 = FOSC/4
101 = FOSC/16
110 = FOSC/64

bit 3-0 **Unimplemented:** Read as '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1.7 CONFIGURING THE A/D

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see Table 19-16 and Table 19-17. After this sample time has elapsed, the A/D conversion can be started.

These steps should be followed for an A/D conversion:

1. Configure the A/D module:
   - Configure analog/digital I/O (ANSx)
   - Select A/D conversion clock (ADCON1<6:4>)
   - Configure voltage reference (ADCON0<6>)
   - Select A/D input channel (ADCON0<5:2>)
   - Select result format (ADCON0<7>)
   - Turn on A/D module (ADCON0<0>)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit (PIR1<6>)
   - Set ADIE bit (PIE1<6>)
   - Set PEIE and GIE bits (INTCON<7:6>)
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0<1>)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared (with interrupts disabled); OR
   - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as T_{AD}. A minimum wait of 2 T_{AD} is required before the next acquisition starts.

EXAMPLE 12-1: A/D CONVERSION

```
;This code block configures the A/D
;for polling, Vdd reference, R/C clock
;and RA0 input.
;
;Conversion start and wait for complete
;polling code included.
;
 BCF     STATUS,RP1   ;Bank 1
 BSF     STATUS,RP0   ;
 MOVLW   B'01110000'  ;A/D RC clock
 MOVWF   ADCON1
 BSF     TRISA,0      ;Set RA0 to input
 BSF     ANSEL0,0     ;Set RA0 to analog
 BCF     STATUS,RP0   ;Bank 0
 MOVLW   B'10000001'  ;Right, Vdd Vref, AN0
 MOVWF   ADCON0
 CALL    SampleTime   ;Wait min sample time
 BSF     ADCON0,GO    ;Start conversion
 BTFSC   ADCON0,GO    ;Is conversion done?
 GOTO    $-1          ;No, test again
 MOVF    ADRESH,W     ;Read upper 2 bits
 MOVWF   RESULTHI
 BSF     STATUS,RP0   ;Bank 1
 MOVF    ADRESL,W     ;Read lower 8 bits
 BCF     STATUS,RP0   ;Bank 0
 MOVWF   RESULTLO
```

12.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 12-4. **The maximum recommended impedance for analog sources is 10 kΩ**. As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

EQUATION 12-1: ACQUISITION TIME EXAMPLE

Assumptions: *Temperature* = *50°C and external impedance of 10kΩ 5.0V VDD*

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$
$$= 5\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)]$$

The value for Tc can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{2047}\right) = V_{CHOLD} \qquad ;[1]\ \text{Vchold charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad ;[2]\ \text{Vchold charge response to Vapplied}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{2047}\right) \qquad ;\text{Combining [1] and [2]}$$

Solving for Tc:

$$T_C = -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047)$$
$$= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885)$$
$$= 1.37\mu s$$

Therefore:

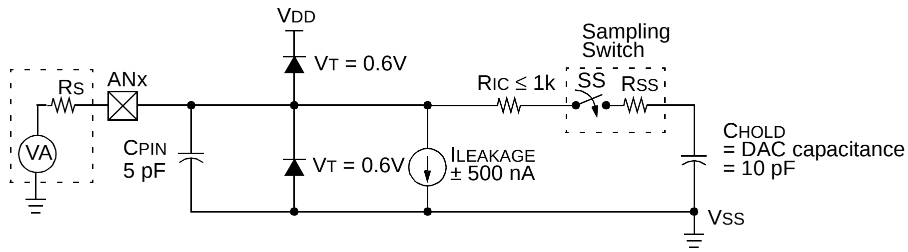
$$T_{ACQ} = 5\mu s + 1.37\mu s + [(50°C - 25°C)(0.05\mu s/°C)]$$
$$= 7.67\mu s$$

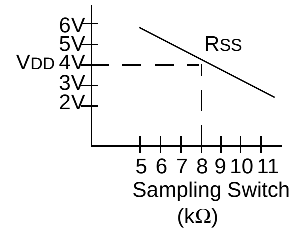
Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 12-4: ANALOG INPUT MODEL





Legend:

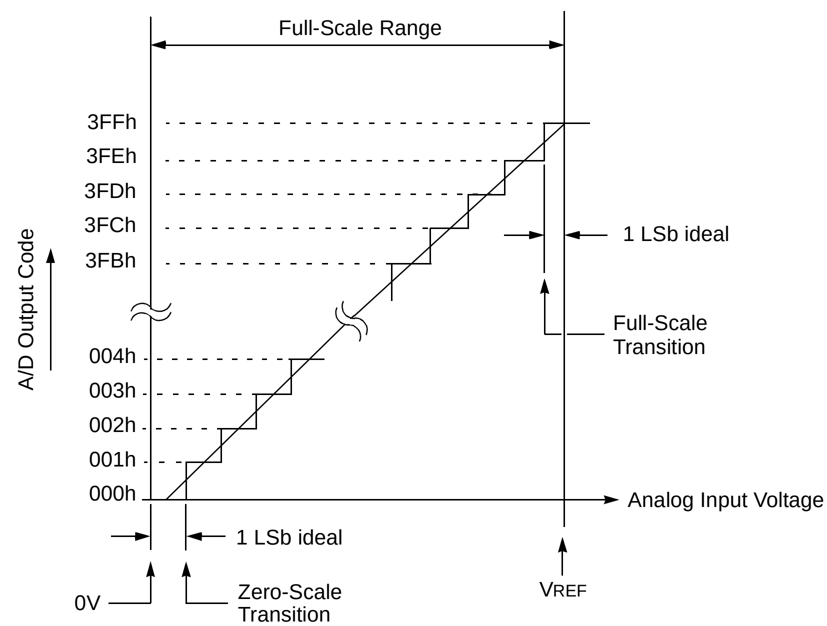
C_{PIN} =	Input Capacitance
V_T =	Threshold Voltage
$I_{LEAKAGE}$ =	Leakage current at the pin due to various junctions
R_{IC} =	Interconnect Resistance
SS =	Sampling Switch
C_{HOLD} =	Sample/Hold Capacitance (from DAC)

12.3 A/D Operation During Sleep

The A/D Converter module can operate during Sleep. This requires the A/D clock source to be set to the FRC option. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled (ADIE and PEIE bits set), the device awakens from Sleep. If the GIE bit (INTCON<7>) is set, the program counter is set to the interrupt vector (0004h). If GIE is clear, the next instruction is executed. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted and the A/D module is turned off. The ADON bit remains set.

FIGURE 12-5: A/D TRANSFER FUNCTION



12.4 Effects of Reset

A device Reset forces all registers to their Reset state. Thus, the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

12.5 Use of the CCP Trigger

An A/D conversion can be started by the "special event trigger" of the CCP module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D conversion and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRESH:ADRESL to the desired location).

The appropriate analog input channel must be selected and the minimum acquisition done before the "special event trigger" sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter. See **Section 8.0 "Capture/Compare/PWM (CCP) Module"** for more information.

TABLE 12-3: SUMMARY OF A/D REGISTERS

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
05h,105h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
06h,106h	PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	uuuu ----
07h,107h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
1Eh	ADRESH	Most Significant 8 bits of the left justified A/D result or 2 bits of the right justified result								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADFM	VCFG	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	0000 0000	0000 0000
85h,185h	TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	--11 1111	--11 1111
86h,186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	1111 ----	1111 ----
87h,187h	TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
91h	ANSEL0	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111
93h	ANSEL1	—	—	—	—	ANS11	ANS10	ANS9	ANS8	---- 1111	---- 1111
9Eh	ADRESL	Least Significant 2 bits of the left justified A/D result or 8 bits of the right justified result								xxxx xxxx	uuuu uuuu
9Fh	ADCON1	—	ADCS2	ADCS1	ADCS0	—	—	—	—	-000 ----	-000 ----

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for A/D module.

NOTES:

13.0 TWO-PHASE PWM

The two-phase PWM (Pulse Width Modulator) is a stand-alone peripheral that supports:

- Single or dual-phase PWM
- Single complementary output PWM with overlap/delay
- Sync input/output to cascade devices for additional phases

Setting either, or both, of the PH1EN or PH2EN bits of the PWMCON0 register will activate the PWM module (see Register 13-1). If PH1 is used then TRISC<1> must be cleared to configure the pin as an output. The same is true for TRISC<4> when using PH2. Both PH1EN and PH2EN must be set when using Complementary mode.

13.1 PWM Period

The PWM period is derived from the main clock (FOSC), the PWM prescaler and the period counter (see Figure 13-1). The prescale bits (PWMP<1:0>, see Register 13-2) determine the value of the clock divider which divides the system clock (FOSC) to the pwm_clk. This pwm_clk is used to drive the PWM counter. In Master mode, the PWM counter is reset when the count reaches the period count (PER<4:0>, see Register 13-2), which determines the frequency of the PWM. The relationship between the PWM frequency, prescale and period count is shown in Equation 13-1.

EQUATION 13-1: PWM FREQUENCY

$$PWM_{FREQ} = \frac{F_{OSC}}{(2^{PWMP} \bullet (PER + 1)}$$

The maximum PWM frequency is FOSC/2, since the period count must be greater than zero.

In Slave mode, the period counter is reset by the SYNC input, which is the master device period counter reset. For proper operation, the slave period count should be equal to or greater than that of the master.

13.2 PWM Phase

Each enabled phase output is driven active when the phase counter matches the corresponding PWM phase count (PH<4:0>, see Register 13-3 and Register 13-4). The phase output remains true until terminated by a feedback signal from either of the comparators or the auto-shutdown activates.

Phase granularity is a function of the period count value. For example, if PER<4:0> = 3, each output can be shifted in 90° steps (see Equation 13-2).

EQUATION 13-2: PHASE RESOLUTION

$$Phase_{DEG} = \frac{360}{(PER + 1)}$$

13.3 PWM Duty Cycle

Each PWM output is driven inactive, terminating the drive period, by asynchronous feedback through the internal comparators. The duty cycle resolution is in effect infinitely adjustable. Either or both comparators can be used to reset the PWM by setting the corresponding comparator enable bit (CxEN, see Register 13-3). Duty cycles of 100% can be obtained by suppressing the feedback which would otherwise terminate the pulse.

The comparator outputs can be "held off", or blanked, by enabling the corresponding BLANK bit (BLANKx, see Register 13-1) for each phase. The blank bit disables the comparator outputs for 1/2 of a system clock (FOSC), thus ensuring at least TOSC/2 active time for the PWM output. Blanking avoids early termination of the PWM output which may result due to switching transients at the beginning of the cycle.

13.4 Master/Slave Operation

Multiple chips can operate together to achieve additional phases by operating one as the master and the others as slaves. When the PWM is configured as a master, the RB7/SYNC pin is an output and generates a high output for one pwm_clk period at the end of each PWM period (see Figure 13-4).

When the PWM is configured as a slave, the RB7/SYNC pin is an input. The high input from a master in this configuration resets the PWM period counter which synchronizes the slave unit at the end of each PWM period. Proper operation of a slave device requires a common external FOSC clock source to drive the master and slave. The PWM prescale value of the slave device must also be identical to that of the master. As mentioned previously, the slave period count value must be greater than or equal to that of the master.

The PWM Counter will be reset and held at zero when both PH1EN and PH2EN (PWMCON0<1:0>) are false. If the PWM is configured as a slave, the PWM Counter will remain reset at zero until the first SYNC input is received.

13.5 Active PWM Output Level

The PWM output signal can be made active-high or active-low by setting or resetting the corresponding POL bit (see Register 13-3 and Register 13-4). When POL is '1' the active output state is VOL. When POL is '0' the active output state is VOH.

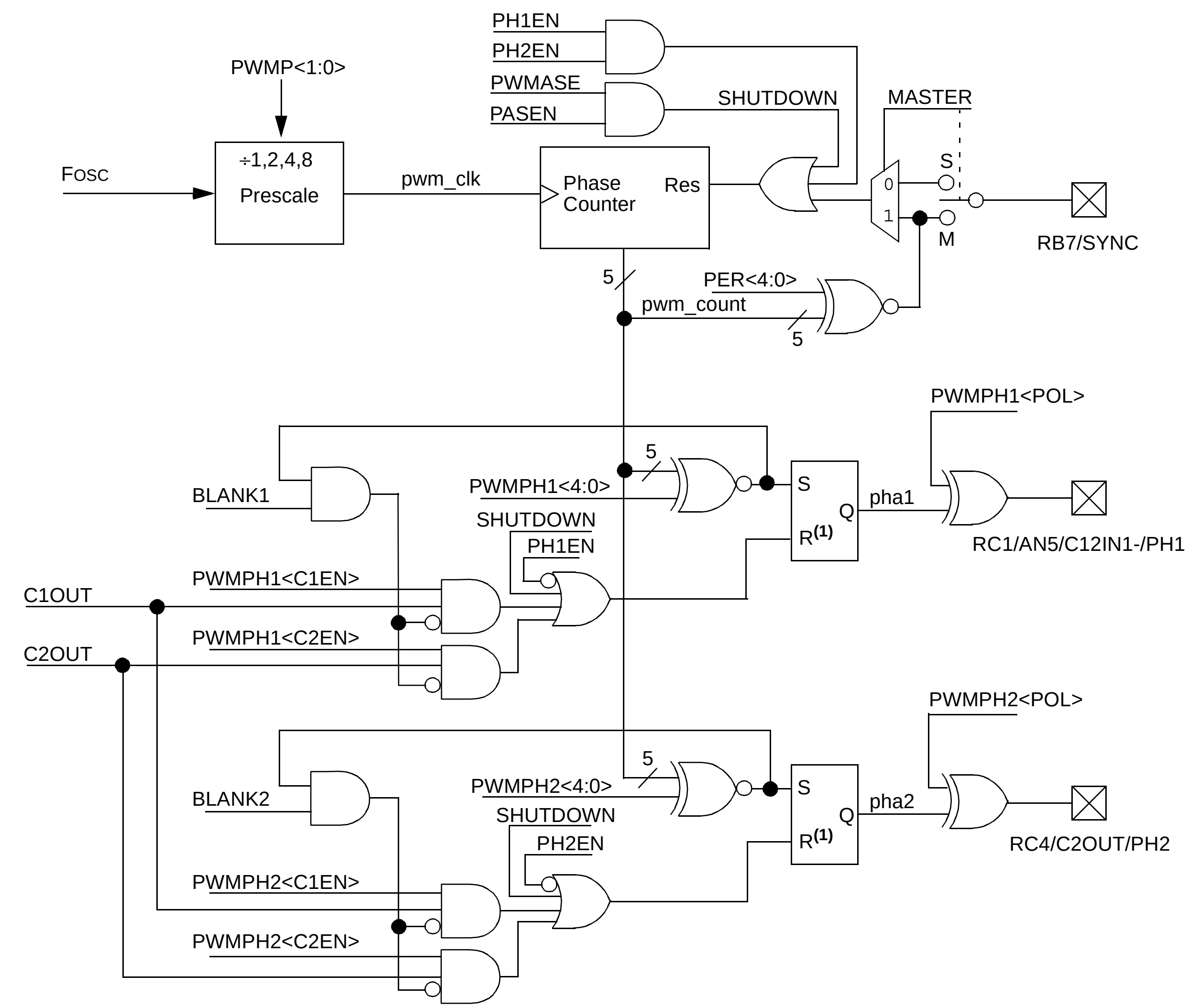
13.6 Auto-Shutdown and Auto-Restart

When the PWM is enabled, the PWM outputs may be configured for auto-shutdown by setting the PASEN bit (see Register 13-1). VIL on the RA2/AN2/T0CKI/INT/C1OUT pin will cause a shutdown event if auto-shutdown is enabled. An auto-shutdown event immediately places the PWM outputs in the inactive state (see **Section 13.5 "Active PWM Output Level"**) and the PWM phase and period counters are reset and held to zero.

The PWMASE bit (see Register 13-2) is set by hardware when a shutdown event occurs. If automatic restarts are not enabled (PRSEN = 0, see Register 13-1), PWM operation will not resume until the PWMASE bit is cleared by firmware after the shutdown condition clears. The PWMASE bit can not be cleared as long as the shutdown condition exists. If automatic restarts are not enabled, the auto-shutdown mode can be forced by writing a '1' to the PWMASE bit.

If automatic restarts are enabled (PRSEN = 1), the PWMASE bit is automatically cleared and PWM operation resumes when the auto-shutdown event clears (VIH on the RA2/AN2/T0CKI/INT/C1OUT pin).

FIGURE 13-1: TWO-PHASE PWM SIMPLIFIED BLOCK DIAGRAM



Note 1: Reset dominant.

REGISTER 13-1: PWMCON0: PWM CONTROL REGISTER 0 (ADDRESS: 111h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN
bit 7							bit 0

bit 7 **PRSEN:** PWM Restart Enable bit
1 = Upon auto-shutdown, the PWMASE shutdown bit clears automatically once the shutdown condition goes away. The PWM restarts automatically.
0 = Upon auto-shutdown, the PWMASE must be cleared in firmware to restart the PWM.

bit 6 **PASEN:** PWM Auto-Shutdown Enable bit
0 = PWM auto-shutdown is disabled
1 = V_{IL} on INT pin will cause auto-shutdown event

bit 5 **BLANK2:** PH2 Blanking bit(1)
1 = The PH2 pin is active for a minimum of 1/2 of an F_{OSC} clock period after it is set
0 = The PH2 pin is reset as soon as the comparator trigger is active

bit 4 **BLANK1:** PH1 Blanking bit(1)
1 = The PH1 pin is active for a minimum of 1/2 of an F_{OSC} clock period after it is set
0 = The PH1 pin is reset as soon as the comparator trigger is active

bit 3-2 **SYNC<1:0>:** SYNC Pin Function bits
0X = SYNC pin not used for PWM. PWM acts as its own master. RB7/SYNC pin is available for general purpose I/O.
10 = SYNC pin acts as system slave, receiving the PWM counter reset pulse
11 = SYNC pin acts as system master, driving the PWM counter reset pulse

bit 1 **PH2EN:** PH2 Pin Enabled bit
1 = The PH2 pin is driven by the PWM signal
0 = The PH2 pin is not used for PWM functions

bit 0 **PH1EN:** PH1 Pin Enabled bit
1 = The PH1 pin is driven by the PWM signal
0 = The PH1 pin is not used for PWM functions

Note 1: Blanking is disabled when operating in complementary mode. See COMOD<1:0> bits in the PWMCON1 register (Register 13-5) for more information.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 13-2: PWMCLK: PWM CLOCK CONTROL REGISTER (ADDRESS: 112h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0
bit 7							bit 0

bit 7 **PWMASE:** PWM Auto-Shutdown Event Status bit
0 = PWM outputs are operating
1 = A shutdown event has occured. PWM outputs are inactive.

bit 6-5 **PWMP<1:0>:** PWM Clock Prescaler bits
00 = pwm_clk = FOSC ÷ 1
01 = pwm_clk = FOSC ÷ 2
10 = pwm_clk = FOSC ÷ 4
11 = pwm_clk = FOSC ÷ 8

bit 4-0 **PER<4:0>:** PWM Period bits
00000 = Not used. (Period = 1/pwm_clk)
00001 = Period = 2/pwm_clk2
0●●●● = • • •
01111 = Period = 16/pwm_clk
10000 = Period = 17/pwm_clk
1●●●● = • • •
11110 = Period = 31/pwm_clk
11111 = Period = 32/pwm_clk

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 13-3: PWMPH1: PWM PHASE 1 CONTROL REGISTER (ADDRESS: 113h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0
bit 7							bit 0

bit 7 **POL:** PH1 Output Polarity bit
1 = PH1 Pin is active-low
0 = PH1 Pin is active-high

bit 6 **C2EN:** Comparator 2 Enable bit
When COMOD<1:0> = 00[(1)]
1 = PH1 is reset when C2OUT goes high
0 = PH1 ignores Comparator 2
When COMOD<1:0> = X1[(1)]
1 = Complementary drive terminates when C2OUT goes high
0 = Comparator 2 is ignored
When COMOD<1:0> = 10[(1)]
C2EN has no effect

bit 5 **C1EN:** Comparator 1 Enable bit
When COMOD<1:0> = 00[(1)]
1 = PH1 is reset when C1OUT goes high
0 = PH1 ignores Comparator 1
When COMOD<1:0> = X1[(1)]
1 = Complementary drive terminates when C1OUT goes high
0 = Comparator 1 is ignored
When COMOD<1:0> = 10[(1)]
C1EN has no effect

bit 4-0 **PH<4:0>:** PWM Phase bits
When COMOD<1:0> = 00[(1)]
00000 = PH1 starts 1 pwm_clk period after falling edge of SYNC pulse. All other PH1 delays are expressed relative to this time.
00001 = PH1 is delayed by 1 pwm_clk pulse
●●●●● = • • •
11111 = PH1 is delayed by 31 pwm_clk pulses
When COMOD<1:0> = X1 or 1X[(1)]
00000 = Complementary drive starts 1 pwm_clk period after falling edge of SYNC pulse. All other delays are expressed relative to this time.
00001 = Complementary drive start is delayed by 1 pwm_clk pulse
●●●●● = • • •
11111 = Complementary drive start is delayed by 31 pwm_clk pulses

Note 1: See PWMCON1 register (Register 13-5).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

REGISTER 13-4: PWMPH2: PWM PHASE 2 CONTROL REGISTER (ADDRESS: 114h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0
bit 7							bit 0

bit 7 **POL:** PH2 Output Polarity bit
1 = PH2 Pin is active low
0 = PH2 Pin is active high

bit 6 **C2EN:** Comparator 2 Enable bit
When COMOD<1:0> = 00(1)
1 = PH2 is reset when C2OUT goes high
0 = PH2 ignores Comparator 2
When COMOD<1:0> = 1X or X1(1)
C2EN has no effect

bit 5 **C1EN:** Comparator 1 Enable bit
When COMOD<1:0> = 00(1)
1 = PH2 is reset when C1OUT goes high
0 = PH2 ignores Comparator 1
When COMOD<1:0> = 1X or X1(1)
C1EN has no effect

bit 4-0 **PH<4:0>:** PWM Phase bits
When COMOD<1:0> = 00(1)
00000 = PH2 starts 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
00001 = PH2 is delayed by 1 pwm_clk pulse
●●●●● = • • •
11111 = PH2 is delayed by 31 pwm_clk pulses
When COMOD<1:0> = 1X(1)
00000 = Complementary drive terminates 1 pwm_clk period after falling edge of SYNC pulse. All other PH2 delays are expressed relative to this time.
00001 = Complementary drive termination is delayed by 1 pwm_clk pulse
●●●●● = • • •
11111 = Complementary drive termination is delayed by 31 pwm_clk pulses
When COMOD<1:0> = 01(1)
PH<4:0> has no effect.

Note 1: See PWMCON1 register (Register 13-5).

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

FIGURE 13-2: TWO-PHASE PWM AUTO-SHUTDOWN AND SYNC TIMING

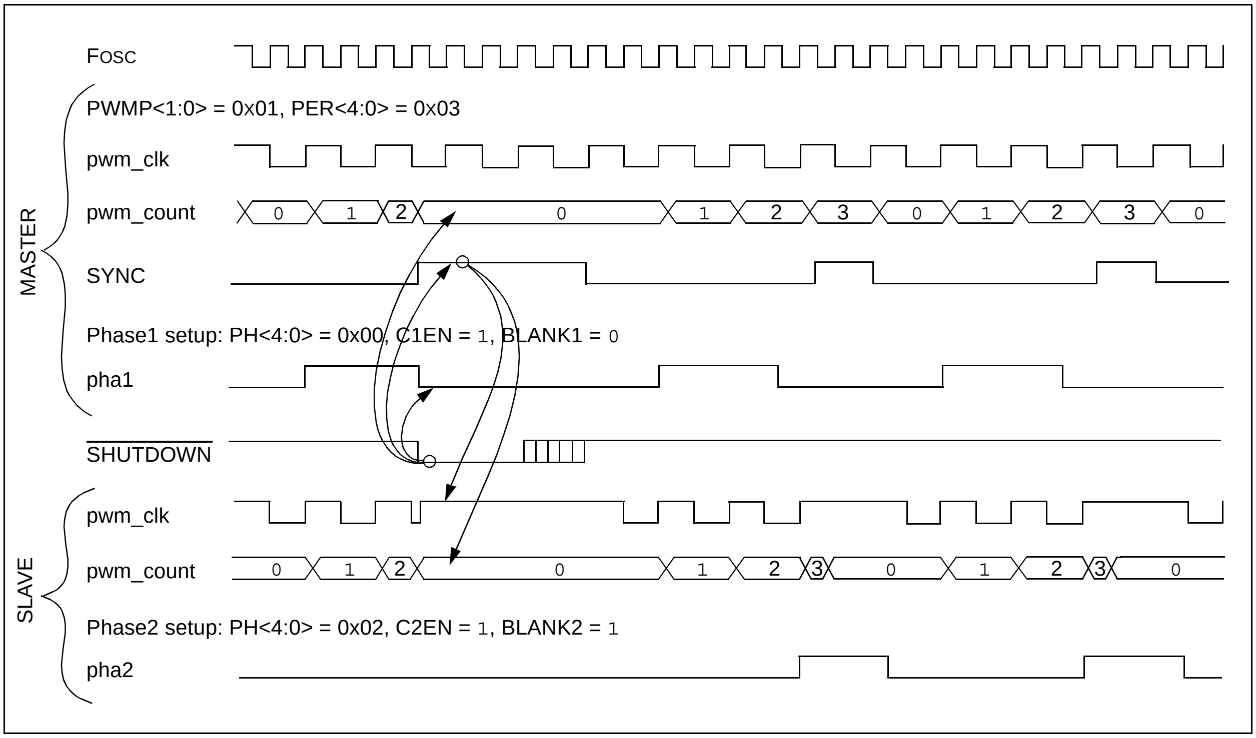
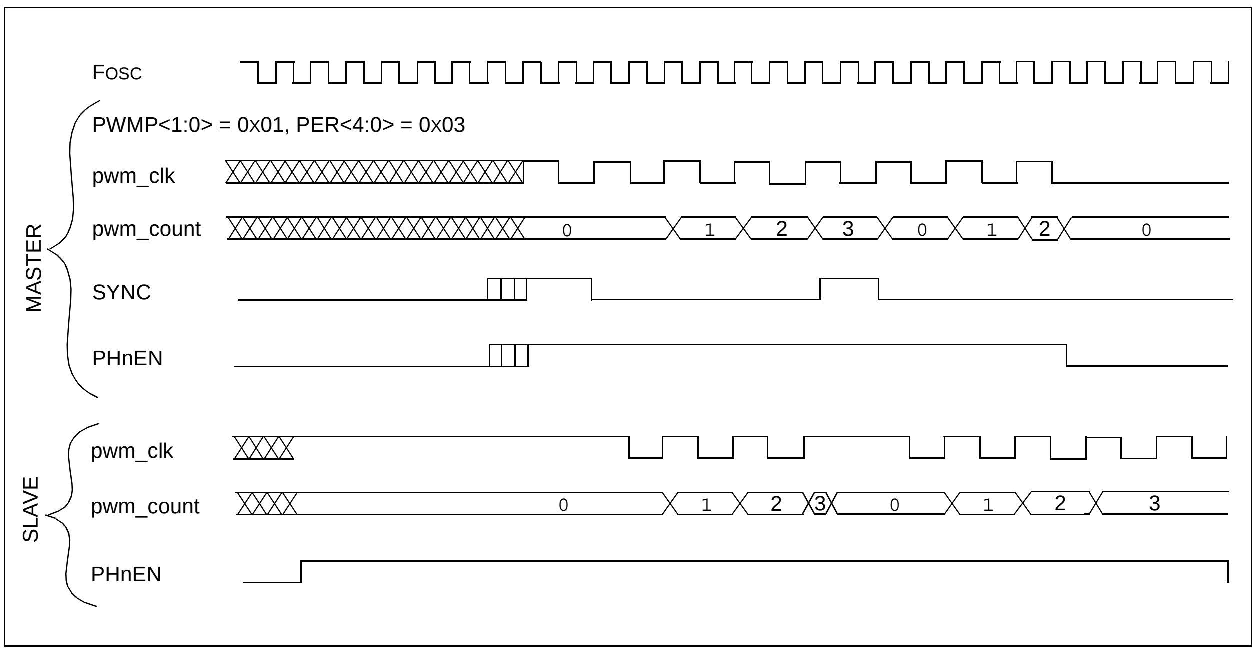


FIGURE 13-3: TWO-PHASE PWM START-UP TIMING



13.7 Example Single Phase Application

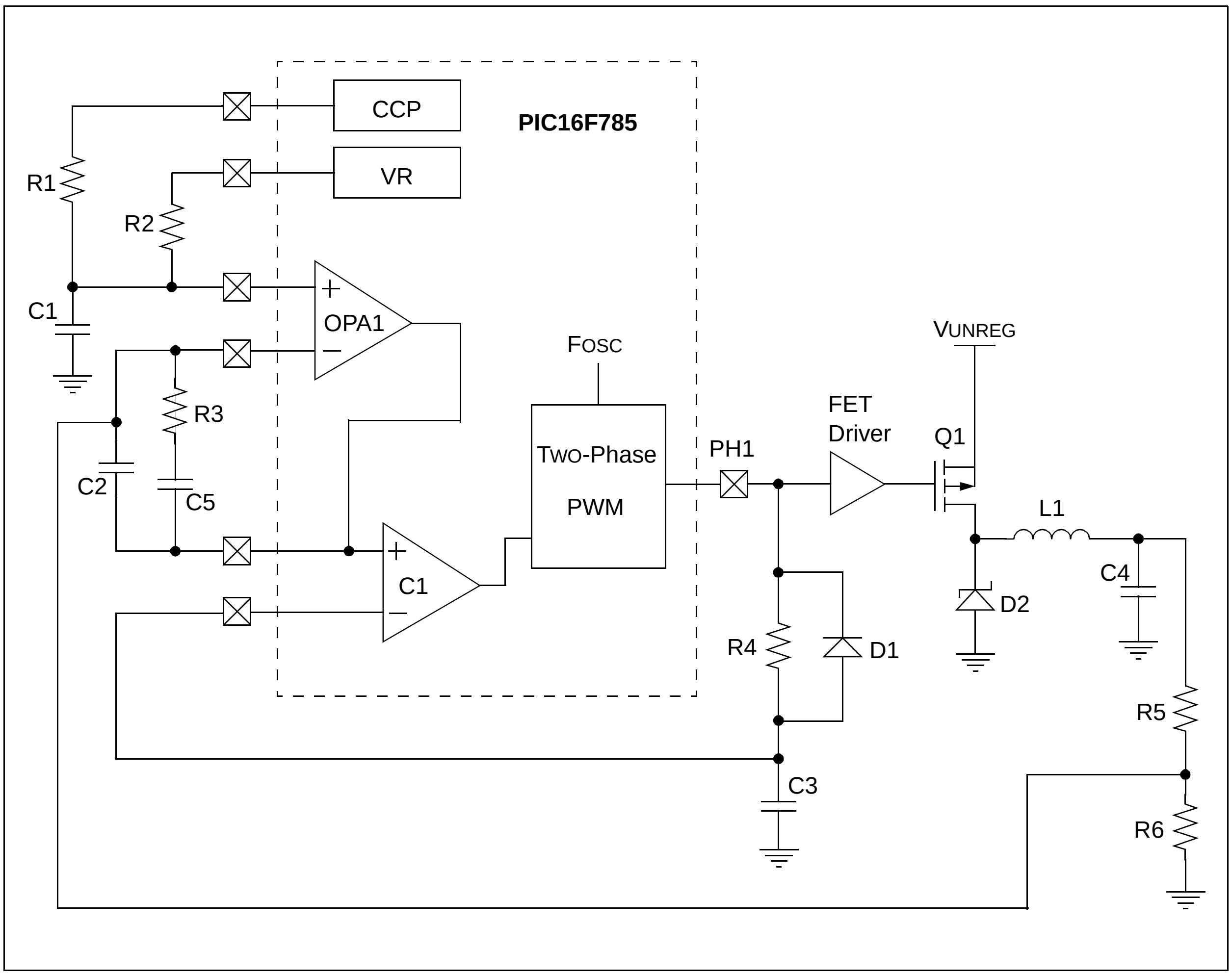
Figure 13-4 shows an example of a single phase buck voltage regulator application. The PWM output drives Q1 with pulses to alternately charge and discharge L1. C4 holds the charge from L1 during the inactive cycle of the drive period. R4 and C3 form a ramp generator.

At the beginning of the PWM period, the PWM output goes high causing the voltage on C3 to rise concurrently with the current in L1. When the voltage across C3 reaches the threshold level present at the positive input of Comparator 1, the comparator output changes and terminates the drive output from the PWM to Q1. When Q1 is not driven, the current path to L1 through Q1 is interrupted, but since the current in L1 cannot stop instantly, the current continues to flow through D2 as L1 discharges into C4. D1 quickly discharges C3 in preparation of the next ramp cycle.

Resistor divider R5 and R6 scale the output voltage, which is inverted and amplified by Op Amp 1, relative to the reference voltage present at the non-inverting pin of the op amp. R3, C5 and C2 form the inverting stabilization gain feedback of the amplifier. The VR reference supplies a stable reference to the non-inverting input of the op amp, which is tweaked by the voltage source created by a secondary time based PWM output of the CCP and R1 and C1.

Output regulation occurs by the following principle: If the regulator output voltage is too low, then the voltage to the non-inverting input of Comparator 1 will rise, resulting in a higher threshold voltage and, consequently, longer PWM drive pulses into Q1. If the output voltage is too high, then the voltage to the non-inverting input of Comparator 1 will fall, resulting in shorter PWM drive pulses into Q1.

FIGURE 13-4: EXAMPLE SINGLE PHASE APPLICATION



 Preliminary

13.8 PWM Configuration

When configuring the Two-Phase PWM, care must be taken to avoid active output levels from the PH1 and PH2 pins before the PWM is fully configured. The following sequence is suggested before the TRISC register or any of the Two-Phase PWM control registers are first configured:

- Output inactive (OFF) levels to the PORTC RC1/AN5/C12IN1-/PH1 and RC4/C2OUT/PH2 pins.
- Clear TRISC bits 1 and 4 to configure the PH1 and PH2 pins as outputs.
- Configure the PWMCLK, PWMPH1, PWMPH2, and PWMCON1 registers.
- Configure the PWMCON0 register.

EXAMPLE 13-1: PWM SETUP EXAMPLE

```
;Example to configure PH1 as a free running PWM output using the SYNC output as the duty cycle
;termination feedback.
;This requires an external connection between the SYNC output and the comparator input.
;SYNC out = RB7 on pin 10
;C1 inverting input = RC2/AN6 on pin 14

;Configure PH1, PH2 and SYNC pins as outputs
;First, ensure output latches are low
    BCF      PORTC,1        ;PH1 low
    BCF      PORTC,4        ;PH2 low
    BCF      PORTB,7        ;SYNC low
;Configure the I/Os as outputs
    BANKSEL  TRISB
    BCF      TRISC,1        ;PH1 output
    BCF      TRISC,4        ;PH2 output
    BCF      TRISB,7        ;SYNC output
;PH1 shares its function with AN5
;Configure AN5 as digital I/O
    BCF      ANSEL0,5       ;AN5 is digital, all others default as analog
;Configure the PWM but don't enable PH1 or PH2 yet
    BANKSEL  PWMCLK
;PWM control setup
    MOVLW    B'00001100'    ;auto shutdown off, no blanking, SYNC on, PH1 and PH2 off
    MOVWF    PWMCON0        ;see data sheet page 93
;PWM clock setup
    MOVLW    B'00111101'    ;pwm_clk = Fosc, 30 clocks in PWM period
    MOVWF    PWMCLK         ;see data sheet page 94
;PH1 setup
    MOVLW    B'00101111'    ;non-inverted, terminate on C1, Start on clock 15
    MOVWF    PWMPH1         ;see data sheet page 95
;PH2 setup
    MOVLW    B'00110101'    ;non-inverted, terminate on C1, Start on clock 21
    MOVWF    PWMPH2         ;see data sheet page 96
;Configure Comparator 1
    MOVLW    B'10011110'    ;C1 on, internal, inverted, normal speed, +:C1VREF, -:AN6
    MOVWF    CM1CON0        ;see data sheet page 68
;Configure comparator voltage reference
    BANKSEL  VRCON
    MOVLW    B'10101100'    ;C1VREN on, low range, CVREF= VDD/2
    MOVWF    VRCON          ;see data sheet page 71
;Everything is setup at this point so now it is time to enable PH1
    BANKSEL  PWMCON0
    BSF      PWMCON0,PH1EN  ;enable PH1
;Module is running autonomously at this point
```

13.9 Complementary Output Mode

The Two-Phase PWM module may be configured to operate in a Complementary Output mode where PH1 and PH2 are always 180 degrees out-of-phase (see Figure 13-5). Three complementary modes are available and are selected by the COMOD<1:0> bits in the PWMCON1 register (see Register 13-5). The difference between the modes is the method by which the PH1 and PH2 outputs switch from the active to the inactive state during the PWM period.

In Complementary mode, there are three methods by which the duty cycle can be controlled. These modes are selected with the COMOD<1:0> bits (see Register 13-5). In each of these modes, the duty cycle is started when the pwm_count = PWMPH1<4:0> and terminates on one of the following:

- Feedback through C1 or C2
- When the pwm_count equals PWMPH1<4:0>
- Combined feedback and pwm_count match

When COMOD<1:0> = `01`, the duty cycle is controlled only by feedback through comparator C1 or C2. In this mode, the active drive cycle starts when pwm_count equals PWMPH1<4:0> and terminates when comparator C1's output goes high (if enabled by PWMPH1<5> = `1`) or when comparator C2 output goes high (if enabled by PWMPH1<6> = `1`).

When COMOD<1:0> = `10`, the duty cycle is controlled only by the PWM Phase counter. In this mode, the active drive cycle starts when the pwm_count equals PWMPH1<4:0> and terminates when the pwm_count equals PWMPH2<4:0>. For example, free running 50% duty cycle can be accomplished by setting COMOD<1:0> = `10` and choosing appropriate values for PWMPH1<4:0> and PWMPH2<4:0>.

When COMOD<1:0> = `11`, the duty cycle is controlled by the phase counter or feedback through comparator C1 or C2. For example, in this mode, the maximum duty cycle is determined by the values of PWMPH1<4:0> (duty cycle start) and PWMPH2<4:0> (duty cycle end). The duty cycle can be terminated earlier than the maximum by feedback through comparator C1 or C2.

13.9.1 DEAD BAND CONTROL

The Complementary Output mode facilitates driving series connected MOSFET drivers by providing dead band drive timing between each phase output (see Figure 13-6). Dead band times are selectable by the CMDLY<4:0> bits of the PWMCON1 register. Delays from 0 to 155 nanoseconds (typical) with a resolution of 5 nanoseconds (typical) are available.

13.9.2 OVERLAP CONTROL

Overlap timing can be accomplished by configuring the Complementary mode for the desired output polarity and overlap time (as dead time) then swapping the output connections and inverting the outputs. For example, to configure a complementary drive for 55 ns of overlap and an active-high drive output on PH1 and an active-low drive output on PH2, set the PWM control registers as follows:

- Connect PH1 driver to PH2 output
- Connect PH2 driver to PH1 output
- Initialize PORTC<1> to `1` (PH2 driver off)
- Initialize PORTC<4> to `0` (PH1 driver off)
- Set TRISC<1,4> to `0` for output
- Set PWMPH1<POL> to `1` (Inverted PH1)
- Set PWMPH2<POL> to `1` (Non-Inverted PH2)
- Set PWMCON1 for 55 ns delay and desired termination (comparator, count or both)
- Set PWMCON0 desired SYNC and auto-shutdown configuration and to enable PH1 and PH2

13.9.3 SHUTDOWN IN COMPLEMENTARY MODE

During shutdown the PH1 and PH2 complementary outputs are forced to their inactive states (see Figure 13-5). When shutdown ceases the PWM outputs revert to their start-up states for the first cycle which is PH1 inactive (output undriven) and PH2 active (output driven).

REGISTER 13-5: PWMCON1: PWM CONTROL REGISTER 1 (ADDRESS: 110h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0
bit 7							bit 0

bit 7 **Unimplemented:** Read as ‘0’

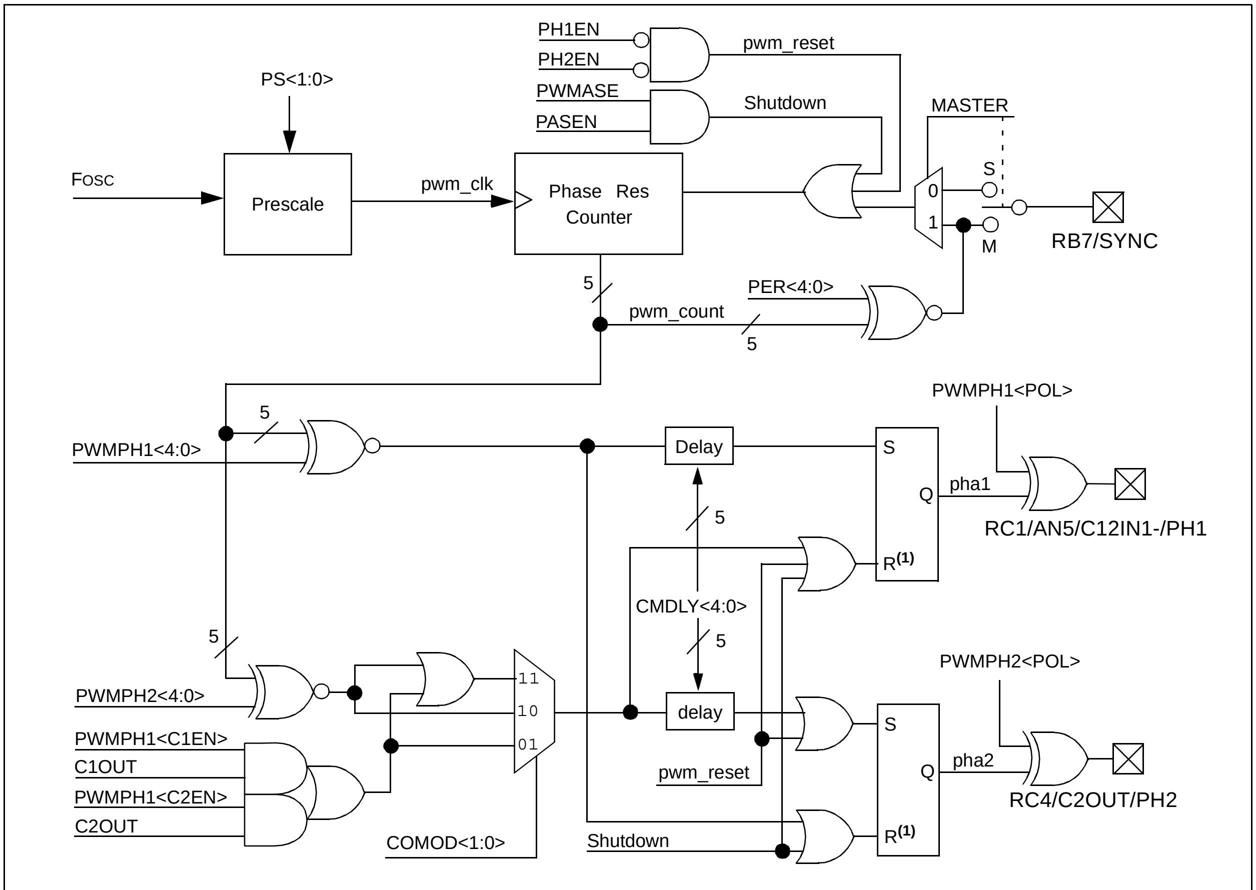
bit 6-5 **COMOD<1:0>:** Complementary Mode Select bits(1)
00 = Normal two-phase operation. Complementary mode is disabled.
01 = Complementary operation. Duty cycle is terminated by C1OUT or C2OUT.
10 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count.
11 = Complementary operation. Duty cycle is terminated by PWMPH2<4:0> = pwm_count or C1OUT or C2OUT.

bit 4-0 **CMDLY<4:0>:** Complementary Drive Dead Time bits (typical)
00000 = Delay = 0
00001 = Delay = 5 ns
00010 = Delay = 10 ns
●●●●● = • • •
11111 = Delay = 155 ns

Note 1: PWMCON0<1:0> must be set to ‘11’ for Complementary mode operation.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

FIGURE 13-5: COMPLEMENTARY OUTPUT PWM BLOCK DIAGRAM



Note 1: Reset dominant.

FIGURE 13-6: COMPLEMENTARY OUTPUT PWM TIMING

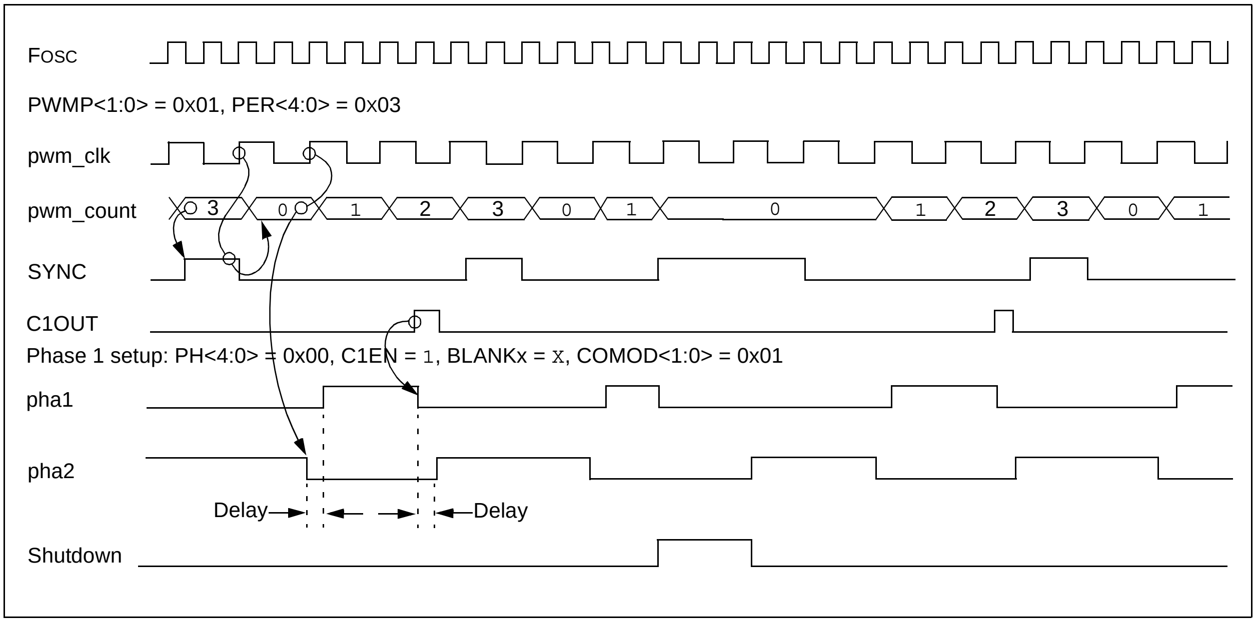


TABLE 13-1: REGISTERS/BITS ASSOCIATED WITH PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
98h	REFCON	—	—	BGST	VRBB	VREN	VROE	CVROE	—	--00 000-	--00 000-
99h	VRCON	C1VREN	C2VREN	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000
119h	CM1CON0	C1ON	C1OUT	C1OE	C1POL	C1SP	C1R	C1CH1	C1CH0	0000 0000	0000 0000
11Ah	CM2CON0	C2ON	C2OUT	C2OE	C2POL	C2SP	C2R	C2CH1	C2CH0	0000 0000	0000 0000
110h	PWMCON1	—	COMOD1	COMOD0	CMDLY4	CMDLY3	CMDLY2	CMDLY1	CMDLY0	-000 0000	-000 0000
111h	PWMCON0	PRSEN	PASEN	BLANK2	BLANK1	SYNC1	SYNC0	PH2EN	PH1EN	0000 0000	0000 0000
112h	PWMCLK	PWMASE	PWMP1	PWMP0	PER4	PER3	PER2	PER1	PER0	0000 0000	0000 0000
113h	PWMPH1	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	0000 0000
114h	PWMPH2	POL	C2EN	C1EN	PH4	PH3	PH2	PH1	PH0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data PWM module.

14.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. The PIC16F785/HV785 has 256 bytes of data EEPROM with an address range from 0h to FFh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature, as well as from chip-to-chip. Please refer to AC Specifications in **Section 19.0 "Electrical Specifications"** for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

Additional information on the data EEPROM is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

REGISTER 14-1: EEDAT: EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0
bit 7							bit 0

bit 7-0 **EEDATn**: Byte Value to Write to or Read From Data EEPROM bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 14-2: EEADR: EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0
bit 7							bit 0

bit 7-0 **EEADR**: Specifies one of 256 locations for EEPROM Read/Write Operation bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

14.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a $\overline{\text{MCLR}}$ Reset, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The EEDAT and EEADR registers are cleared by a Reset. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag EEIF bit (PIR1<7>) is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note:	The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 14-3: EECON1: EEPROM CONTROL REGISTER (ADDRESS: 9Ch)

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7							bit 0

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ Reset, any WDT Reset during normal operation or BOR reset)
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
0 = Does not initiate an EEPROM read

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'S' = Bit can only be set	'0' = Bit is cleared	x = Bit is unknown

14.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>), as shown in Example 14-1. The data is available, in the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 14-1: DATA EEPROM READ

```
BSF    STATUS,RP0    ;Bank 1
BCF    STATUS,RP1    ;
MOVLW  CONFIG_ADDR   ;
MOVWF  EEADR         ;Address to read
BSF    EECON1,RD     ;EE Read
MOVF   EEDAT,W       ;Move data to W
```

14.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 14-2.

EXAMPLE 14-2: DATA EEPROM WRITE

```
BSF     STATUS,RP0    ;Bank 1
BCF     STATUS,RP1    ;
BSF     EECON1,WREN   ;Enable write
BCF     INTCON,GIE    ;Disable INTs
BTFSC   INTCON,GIE    ;See AN-576
GOTO    $-2           ;
MOVLW   55h           ;Unlock write
MOVWF   EECON2        ;
MOVLW   AAh           ;
MOVWF   EECON2        ;
BSF     EECON1,WR     ;Start the write
BSF     INTCON,GIE    ;Enable INTs
```

Required Sequence

The write will not initiate if the sequence in Example 14-2 is not followed exactly (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. It is strongly recommended that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in the hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR1<7>) register must be cleared by software.

14.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 14-3) to the desired value to be written.

EXAMPLE 14-3: WRITE VERIFY

```
BSF    STATUS,RP0   ;Bank 1
BCF    STATUS,RP1   ;
MOVF   EEDAT,W      ;EEDAT not changed
                     from previous write
BSF    EECON1,RD    ;YES, Read the
                    ; value written
XORWF  EEDAT,W      ;
BTFSS  STATUS,Z     ;Is data the same
GOTO   WRITE_ERR    ;No, handle error
                    ;Yes, continue
```

14.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

14.5 Protect Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit helps prevent an accidental write during a brown-out, power glitch and software malfunction.

14.6 Data EEPROM Operation During Code-Protect

Data memory can be code-protected by programming the CPD bit in the Configuration Word (Register 15-1) to '0'.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended that the user code protect the program memory when code protecting the data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to '0' will also help prevent data memory code protection from becoming breached.

TABLE 14-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	0000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2	EEPROM Control register 2 (not a physical register)								---- ----	---- ----

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by data EEPROM module.

15.0 SPECIAL FEATURES OF THE CPU

The PIC16F785/HV785 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset:
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through an external Reset, Watchdog Timer Wake-up or interrupt.

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 15-1).

15.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 15-1. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

REGISTER 15-1: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h)

—	—	FCMEN	IESO	BOREN1	BOREN0	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 13													bit 0

bit 13-12 **Unimplemented:** Read as '1'

bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit(5)
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled

bit 10 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled
0 = Internal External Switchover mode is disabled

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits(1)
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit (PCON<4>)
00 = BOR disabled

bit 7 **$\overline{\text{CPD}}$:** Data Code Protection bit(2), (3)
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled

bit 6 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 5 **MCLRE:** RA3/$\overline{\text{MCLR}}$ pin function select bit(4)
1 = RA3/$\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$
0 = RA3/$\overline{\text{MCLR}}$ pin function is digital input, $\overline{\text{MCLR}}$ internally tied to V_{DD}

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit(5)
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit (WDTCON<0>)

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on RA4/AN3/T1G/OSC2/CLKOUT pin, RC on RA5/T1CKI/OSC1/CLKIN
110 = RCIO oscillator: I/O function on RA4/AN3/T1G/OSC2/CLKOUT pin, RC on RA5/T1CKI/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on RA4/AN3/T1G/OSC2/CLKOUT pin, I/O function on RA5/T1CKI/OSC1/CLKIN
100 = INTOSCIO oscillator: I/O function on RA4/AN3/T1G/OSC2/CLKOUT pin, I/O function on RA5/T1CKI/OSC1/CLKIN
011 = EC: I/O function on RA4/AN3/T1G/OSC2/CLKOUT pin, CLKIN on RA5/T1CKI/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on RA4/AN3/T1G/OSC2/CLKOUT and RA5/T1CKI/OSC1/CLKIN(5)
001 = XT oscillator: Crystal/resonator on RA4/AN3/T1G/OSC2/CLKOUT and RA5/T1CKI/OSC1/CLKIN(5)
000 = LP oscillator: Low-power crystal on RA4/AN3/T1G/OSC2/CLKOUT and RA5/T1CKI/OSC1/CLKIN(5)

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: Program memory bulk erase must be performed to turn off code protection.
3: The entire data EEPROM will be erased when the code protection is turned off.
4: When $\overline{\text{MCLR}}$ is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.
5: If the HS, XT, or LP oscillator fails In Fail-safe mode the Watchdog time-out can occur only once after which it will be disabled until the oscillator is restored.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

15.2 Reset

The PIC16F785/HV785 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a “Reset state” on:

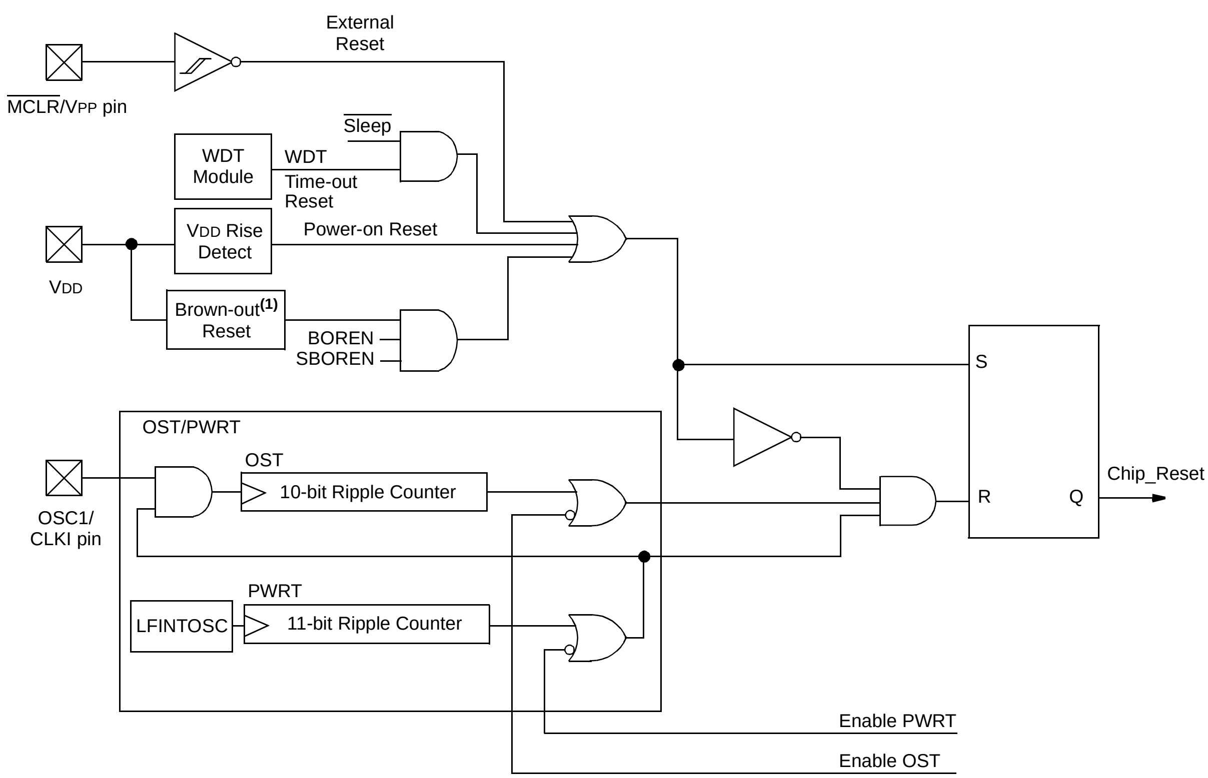
- Power-on Reset
- $\overline{\text{MCLR}}$ Reset
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

They are not affected by a WDT wake-up since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 15-2. These bits are used in software to determine the nature of the Reset. See Table 15-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 15-1.

The $\overline{\text{MCLR}}$ Reset path has a noise filter to detect and ignore small pulses. See **Section 19.0 “Electrical Specifications”** for pulse width specifications.

FIGURE 15-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: Refer to the Configuration Word register (Register 15-1).

15.2.1 POWER-ON RESET

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. A minimum rise rate for VDD is required. See **Section 19.0 "Electrical Specifications"** for details. If the BOR is enabled, the minimum rise rate specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see **Section 15.2.4 "Brown-Out Reset (BOR)"**)

The POR circuit, on this device, has a POR re-arm circuit. This circuit is designed to ensure a re-arm of the POR circuit if VDD drops below a preset re-arming voltage (VPARM) for at least the minimum required time. Once VDD is below the re-arming point for the minimum required time, the POR Reset will reactivate and remain in Reset until VDD returns to a value greater than VPOR. At this point, a 1 µs (typical) delay will be initiated to allow VDD to continue to ramp to a voltage safely above VPOR.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "*Power-up Trouble Shooting*" (DS00607).

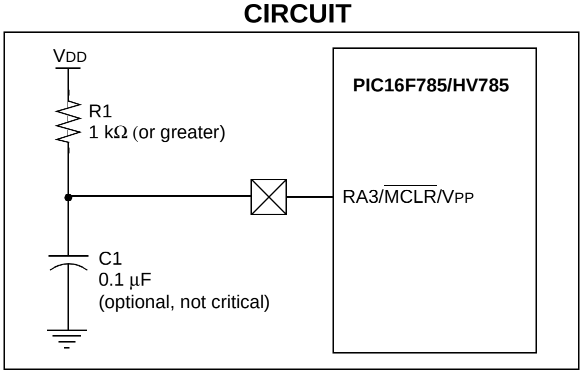
15.2.2 MASTER CLEAR (MCLR)

PIC16F785/HV785 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from earlier devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 15-1, is suggested.

FIGURE 15-2: RECOMMENDED MCLR CIRCUIT



An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word. When cleared, MCLR is internally tied to VDD and an internal Weak Pull-up is enabled for the MCLR pin. The VPP function of the RA3/MCLR/VPP pin is not affected by selecting the internal MCLR option.

15.2.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.4 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE can disable (if '1') or enable (if '0') the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Time Delay will vary from chip-to-chip and vary due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 19.0 "Electrical Specifications"**).

15.2.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When BOREN<1:0> = 01, the SBOREN bit (PCON<4>) enables/disables the BOR allowing it to be controlled in software. By selecting BOREN<1:0>, the BOR is automatically disabled in Sleep to conserve power, and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 15-1 for the Configuration Word definition.

If VDD falls below VBOR for greater than parameter (TBOR), see **Section 19.0 "Electrical Specifications"**, the Brown-out situation will reset the device. This will occur regardless of the VDD slew rate. A Reset is not assured if VDD falls below VBOR for less than parameter (TBOR).

On any Reset (Power-on, Brown-out Reset, Watchdog, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 15-3). The Power-up Timer will now be invoked, if enabled, and will keep the chip in Reset an additional 64 ms.

Note:	The Power-up Timer is enabled by the PWRTE bit in the Configuration Word.

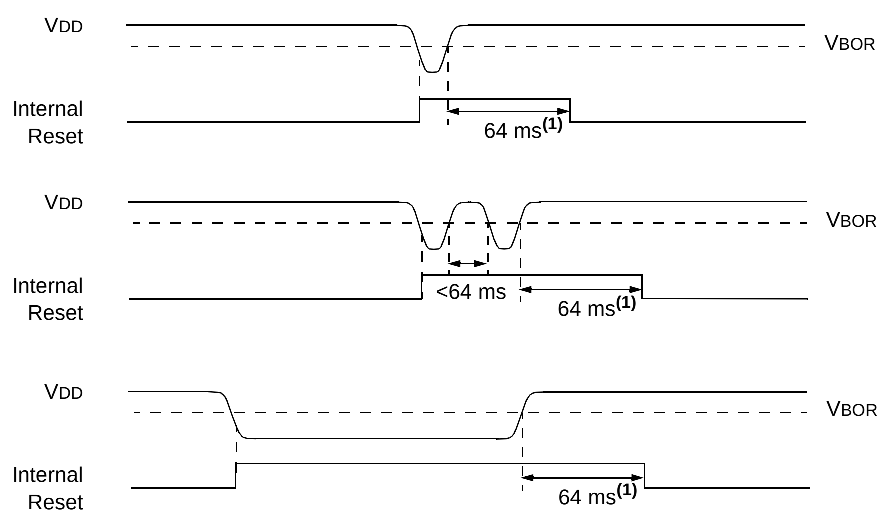
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

15.2.5 BOR CALIBRATION

The PIC16F785/HV785 stores the BOR calibration values in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) and thus, does not require reprogramming.

Note:	Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

FIGURE 15-3: BROWN-OUT SITUATIONS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit is programmed to '0'.

15.2.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time out is invoked after POR has expired, then OST is activated after the PWRT time out has expired. The total time out will vary based on oscillator configuration and $\overline{\text{PWRTE}}$ bit status. For example, in EC mode with $\overline{\text{PWRTE}}$ bit equal to '1' (PWRT disabled), there will be no time out at all. Figure 15-4, Figure 15-6 and Figure 15-6 depict time-out sequences. The device can execute code from the INTOSC, while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 3.6.2 "Two-Speed Start-up Sequence"** and **Section 3.7 "Fail-Safe Clock Monitor"**).

Since the time outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time outs will expire. Then bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 15-6). This is useful for testing purposes or to synchronize more than one PIC16F785/HV785 device operating in parallel.

Table 15-5 shows the Reset conditions for some special registers, while Table 15-4 shows the Reset conditions for all the registers.

15.2.7 POWER CONTROL (PCON) REGISTER

The Power Control register (address 8Eh) has two Status bits to indicate what type of Reset that last occurred.

Bit 0 is $\overline{\text{BOR}}$ (Brown-out Reset). $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ = 0, indicating that a Brown-out has occurred. The $\overline{\text{BOR}}$ Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word).

Bit 1 is $\overline{\text{POR}}$ (Power-on Reset). It is '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if $\overline{\text{POR}}$ is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 15.2.4 "Brown-Out Reset (BOR)"**.

TABLE 15-1: TIME OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	$\overline{\text{PWRTE}}$ = 0	$\overline{\text{PWRTE}}$ = 1	
XT, HS, LP	TPWRT + 1024•TOSC	1024•TOSC	TPWRT + 1024•TOSC	1024•TOSC	1024•TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 15-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
u	u	1	0	$\overline{\text{MCLR}}$ Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 15-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets(1)
03h, 103h 83h, 183h	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
8Eh	PCON	—	—	—	SBOREN	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---1 --qq	---u --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

FIGURE 15-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 1

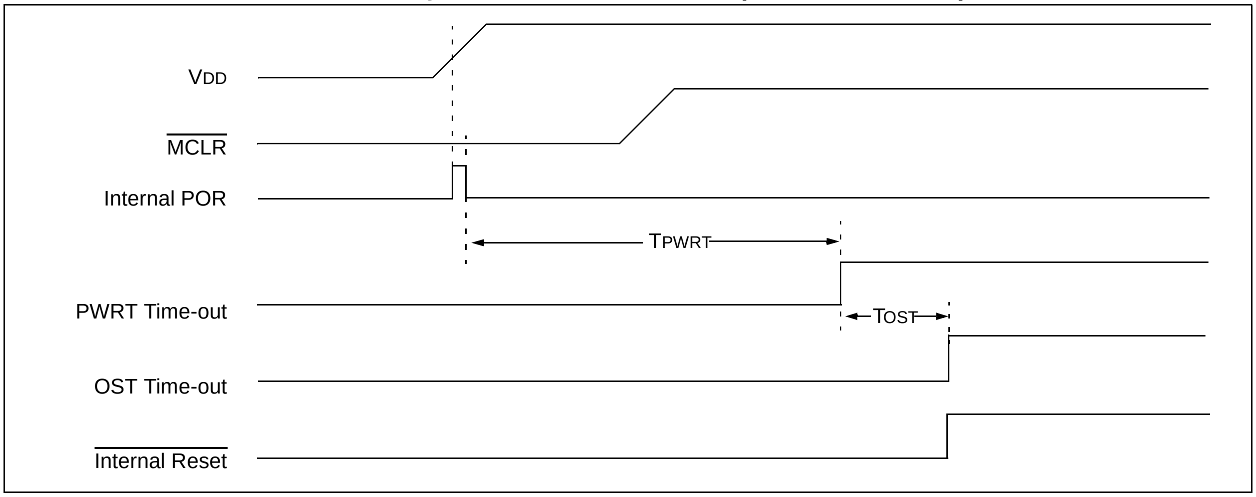


FIGURE 15-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{MCLR}$): CASE 2

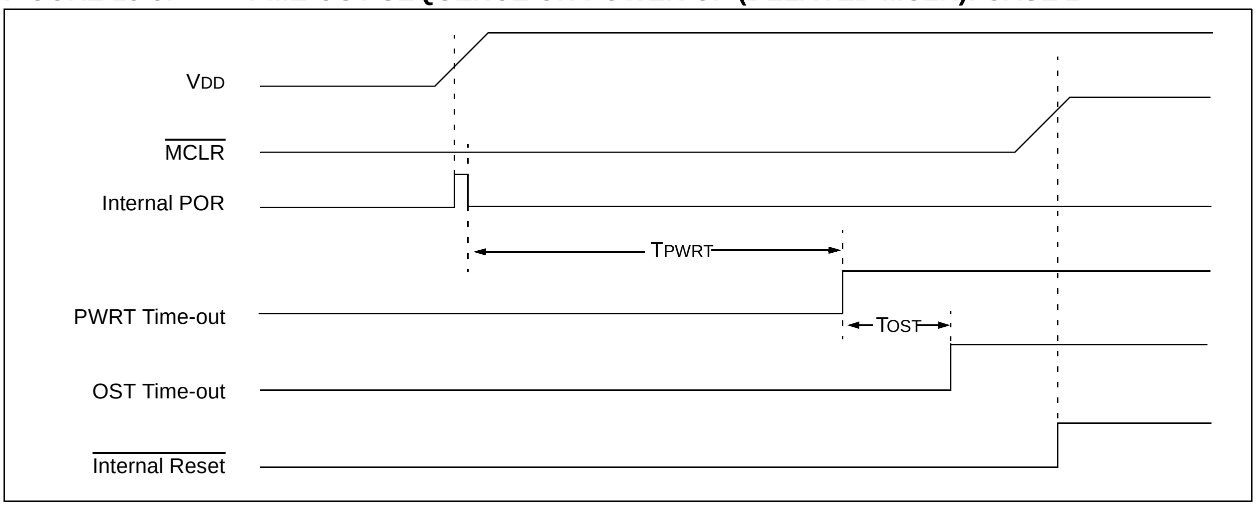


FIGURE 15-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ WITH V_{DD})

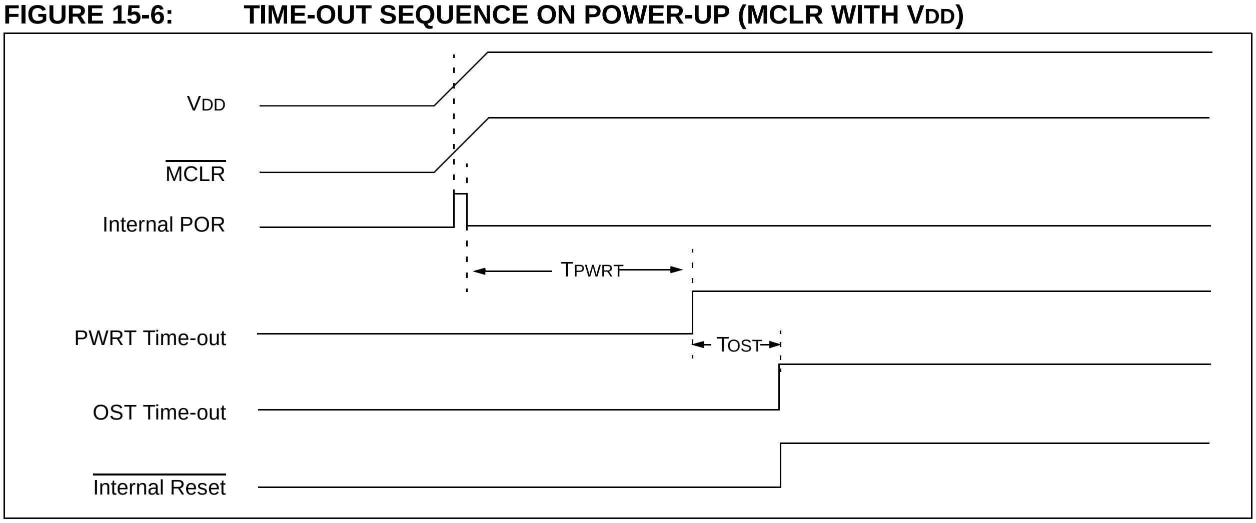


TABLE 15-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA	05h	--x0 x000(6)	--u0 u000(7)	--uu uuuu
PORTB	06h	xx00 ----(6)	uu00 ----(7)	uuuu ----
PORTC	07h	00xx 0000(6)	00uu uuuu(7)	uuuu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	uuuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	--00 0000	--00 0000	--uu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	0000 0000	0000 0000	uuuu uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISA	85h	--11 1111	--11 1111	--uu uuuu
TRISB	86h	1111 ----	1111 ----	uuuu ----
TRISC	87h	1111 1111	1111 1111	uuuu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	---1 --0x	---u --uq(1,5)	---u --uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
ANSEL0	91h	1111 1111	1111 1111	uuuu uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
ANSEL1	93h	---- 1111	---- 1111	---- uuuu
WPUA	95h	--11 1111	--11 1111	--uu uuuu
IOCA	96h	--00 0000	--00 0000	--uu uuuu
REFCON	98h	--00 000-	--00 000-	--uu uuu-

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 15-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: Analog channels read 0 but data latches are unknown.

7: Analog channels read 0 but data latches are unchanged.

TABLE 15-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	$\overline{MCLR}$ Reset WDT Reset Brown-out Reset[1]	Wake-up from Sleep through interrupt Wake-up from Sleep through WDT Time-out
VRCON	99h	000- 0000	000- 0000	uuu- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu uuuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	---- ----	---- ----	---- ----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	9Fh	-000 ----	-000 ----	-uuu ----
PWMCON1	110h	-000 0000	-000 0000	-uuu uuuu
PWMCON0	111h	0000 0000	0000 0000	uuuu uuuu
PWMCLK	112h	0000 0000	0000 0000	uuuu uuuu
PWMPH1	113h	0000 0000	0000 0000	uuuu uuuu
PWMPH2	114h	0000 0000	0000 0000	uuuu uuuu
CM1CON0	119h	0000 0000	0000 0000	uuuu uuuu
CM2CON0	11Ah	0000 0000	0000 0000	uuuu uuuu
CM2CON1	11Bh	00-- --10	00-- --10	uu-- --uu
OPA1CON	11Ch	0--- ----	0--- ----	u--- ----
OPA2CON	11Dh	0--- ----	0--- ----	u--- ----

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as ‘0’, q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
4: See Table 15-5 for Reset value for specific condition.
5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.
6: Analog channels read 0 but data latches are unknown.
7: Analog channels read 0 but data latches are unchanged.

TABLE 15-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---1 --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	---u --uu
$\overline{\text{MCLR}}$ Reset during Sleep	000h	0001 0uuu	---u --uu
WDT Reset	000h	0000 uuuu	---u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---u --uu
Brown-out Reset	000h	0001 1uuu	---1 --u0
Interrupt Wake-up from Sleep	PC + 1(1)	uuu1 0uuu	---u --uu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

15.3 Interrupts

The PIC16F785/HV785 has 11 sources of interrupt:

- External Interrupt RA2/INT
- TMR0 Overflow Interrupt
- PORTA Change Interrupt
- 2 Comparator Interrupts
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A Global Interrupt Enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE1 register. GIE is cleared on Reset.

The Return from Interrupt instruction, `RETFIE`, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- PORTA Change Interrupt
- TMR0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in special register PIE1.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- 2 Comparator Interrupts
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is PUSHed onto the stack
- The PC is loaded with 0004h

For external interrupt events, such as the INT pin or PORTA change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 15-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1:	Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
2:	When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, A/D, Data EEPROM or CCP modules, refer to the respective peripheral section.

15.3.1 RA2/AN2/T0CKI/INT/C1OUT INTERRUPT

External interrupt on RA2/AN2/T0CKI/INT/C1OUT pin is edge-triggered; either rising, if INTEDG bit (OPTION_REG<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the RA2/AN2/T0CKI/INT/C1OUT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The RA2/AN2/T0CKI/INT/C1OUT interrupt can wake-up the processor from Sleep if the INTE bit was set prior to going into Sleep. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up (0004h). See **Section 15.6 "Power-Down Mode (Sleep)"** for details on Sleep and Figure 15-10 for timing of wake-up from Sleep through RA2/AN2/T0CKI/INT/C1OUT interrupt.

Note:	The ANSEL0 (91h), and ANSEL1 (93h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

15.3.2 TMR0 INTERRUPT

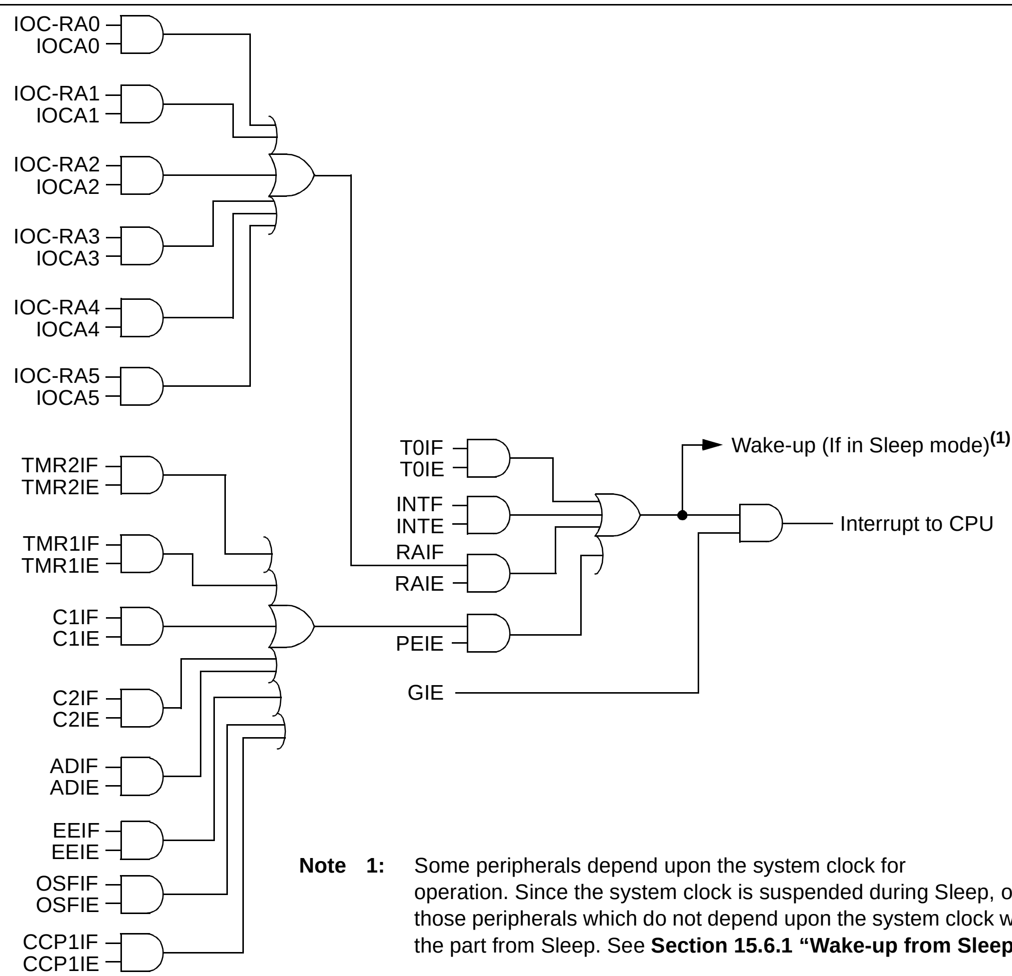
An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. See **Section 5.0 "Timer0 Module"** for operation of the Timer0 module.

15.3.3 PORTA INTERRUPT

An input change on PORTA change sets the RAIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the RAIE (INTCON<3>) bit. Plus, individual pins can be configured through the IOCA register.

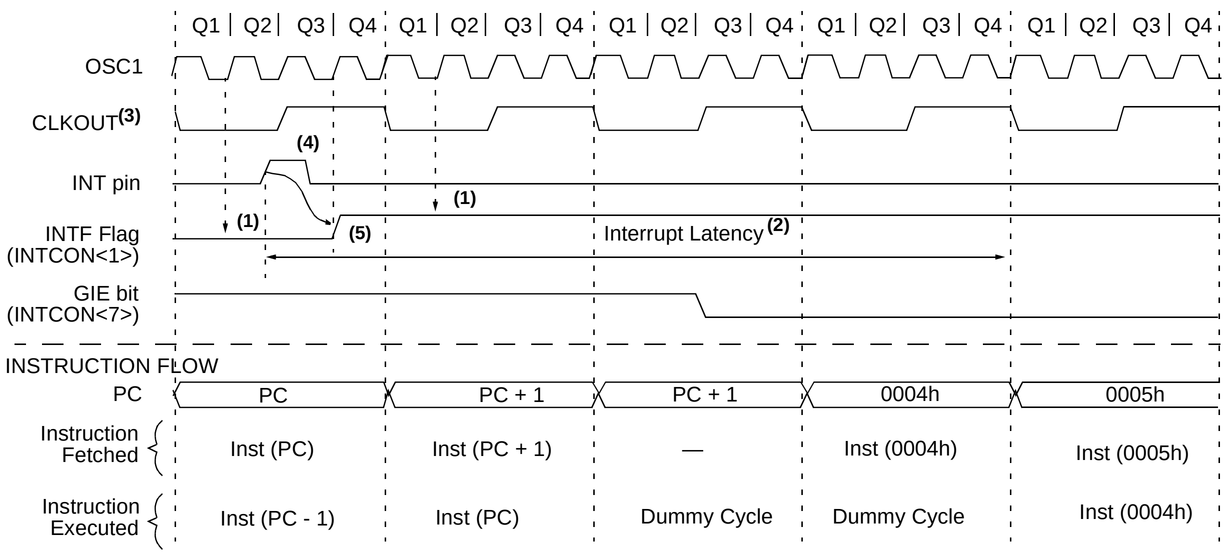
Note:	If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the RAIF interrupt flag may not get set.

FIGURE 15-7: INTERRUPT LOGIC



Note 1: Some peripherals depend upon the system clock for operation. Since the system clock is suspended during Sleep, only those peripherals which do not depend upon the system clock will wake the part from Sleep. See **Section 15.6.1 "Wake-up from Sleep"**.

FIGURE 15-8: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-4 TCY. Synchronous latency = 3 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT is available only in INTOSC and RC Oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 19.0 "Electrical Specifications"**.

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

TABLE 15-6: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000 0000	0000 0000
0Ch	PIR1	EEIF	ADIF	CCP1IF	C2IF	C1IF	OSFIF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	EEIE	ADIE	CCP1IE	C2IE	C1IE	OSFIE	TMR2IE	TMR1IE	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the Interrupt module.

15.4 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the last 16 bytes of all banks are common in the PIC16F785/HV785 (see Figure 2-2), temporary holding registers W_TEMP and STATUS_TEMP should be placed in here. These 16 locations do not require banking, therefore, making it easier to save and restore context. The same code shown in Example 15-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC16F785/HV785 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 15-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP            ;Copy W to TEMP register
SWAPF   STATUS,W          ;Swap status to be saved into W (swap does not affect status)
CLRF    STATUS            ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF   STATUS_TEMP       ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                    ;Insert user code here
:
SWAPF   STATUS_TEMP,W     ;Swap STATUS_TEMP register into W
                          ;(sets bank to original state)
MOVWF   STATUS            ;Move W into Status register
SWAPF   W_TEMP,F          ;Swap W_TEMP
SWAPF   W_TEMP,W          ;Swap W_TEMP into W
```


15.5 Watchdog Timer (WDT)

For PIC16F785/HV785, the WDT has been modified from previous PIC16FXXX devices. The new WDT is code and functionally compatible with previous PIC16FXXX WDT modules and adds a 16-bit prescaler to the WDT. This allows the user to scale the value for the WDT and TMR0 at the same time. In addition, the WDT time out value can be extended to 268 seconds. WDT is cleared under certain conditions described in Table 15-7.

15.5.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit does not reflect that the LFINTOSC is enabled (OSCON<1>).

The value of WDTCON is '`---0 1000`' on all Resets. This gives a nominal time base of 16 ms, which is compatible with the time base generated with previous PIC16FXXX microcontroller versions.

Note:	When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the INTRC and the multiplexers used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the INTRC by 128 to 65536, giving the time base used for the WDT a nominal range of 1 ms to 268s.

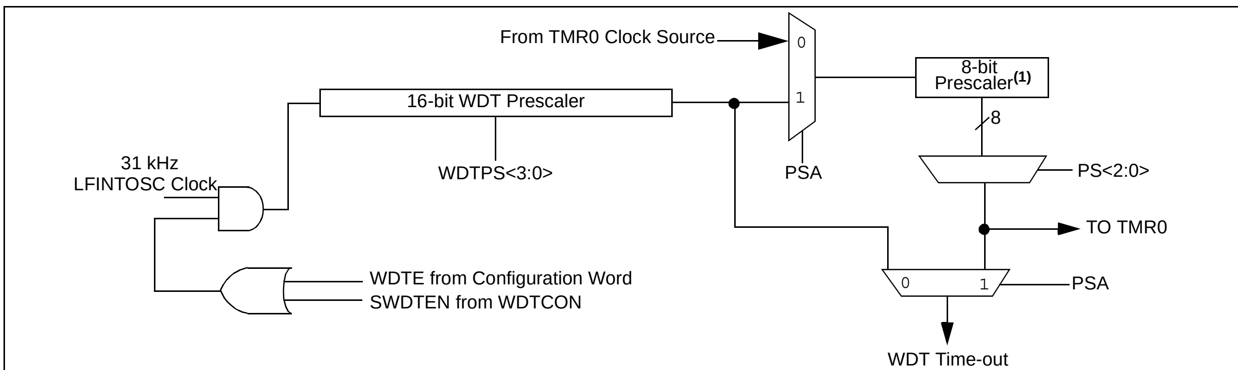
15.5.2 WDT CONTROL

The WDTE bit is located in the Configuration Word. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit (WDTCON<0>) has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits (OPTION_REG) have the same function as in previous versions of the PIC16FXXX family of microcontrollers. See **Section 5.0 "Timer0 Module"** for more information.

FIGURE 15-9: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: This is the shared Timer0/WDT prescaler. See **Section 5.4 "Prescaler"** for more information.

TABLE 15-7: WDT STATUS

Conditions	WDT
WDTE = `0`	Cleared
`CLRWDT` command	
OSC FAIL detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

REGISTER 15-2: WDTCON: WATCHDOG TIMER CONTROL REGISTER (ADDRESS: 18h)

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN(1)
bit 7							bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32
0001 = 1:64
0010 = 1:128
0011 = 1:256
0100 = 1:512 (Reset value)
0101 = 1:1024
0110 = 1:2048
0111 = 1:4096
1000 = 1:8192
1001 = 1:16384
1010 = 1:32768
1011 = 1:65536
1100 = reserved
1101 = reserved
1110 = reserved
1111 = reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer bit(1)

1 = WDT is turned on
0 = WDT is turned off (Reset value)

Note 1: If WDTE configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 15-8: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR,BOR	Value on all other resets
03h, 103h 83h, 183h	STATUS	IRP	RP1	RPO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000
81h/ 181h	OPTION_REG	$\overline{\text{RAPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
2007h(1)	CONFIG	$\overline{\text{CPD}}$	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	uuuu uuuu	uuuu uuuu

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 15-1 for operation of all Configuration Word bits.

15.6 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running
- $\overline{PD}$ bit in the STATUS register is cleared
- $\overline{TO}$ bit is set
- Oscillator driver is turned off
- I/O ports maintain the status they had before SLEEP was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or VSS, with no external circuitry drawing current from the I/O pin and all unused peripheral modules should be disabled. Digital I/O pins that are high-impedance inputs should be pulled high, or low, externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTA should be considered.

The $\overline{MCLR}$ pin must be at a logic high level.

Note:	It should be noted that a Reset generated by a WDT time-out does not drive $\overline{MCLR}$ pin low.

15.6.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on $\overline{MCLR}$ pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from RA2/AN2/T0CKI/INT/C1OUT pin, PORTA change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device Reset. The $\overline{PD}$ bit, which is set on power-up, is cleared when Sleep is invoked. $\overline{TO}$ bit is cleared if WDT Wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

- TMR1 interrupt; Timer1 must be operating as an asynchronous counter.
- CCP Capture mode interrupt
- A/D conversion (when A/D clock source is RC)
- EEPROM write operation completion
- Comparator output changes state
- Interrupt-on-change
- External Interrupt from INT pin

Other peripherals cannot generate interrupts since, during Sleep, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit (and PEIE bit where applicable) must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution of the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction, following SLEEP, is not desired, the user should place a NOP after the SLEEP instruction.

Note:	If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set (including PEIE, where applicable), the device will immediately wake-up from Sleep. The SLEEP instruction is completely executed.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

15.6.2 WAKE-UP USING INTERRUPTS

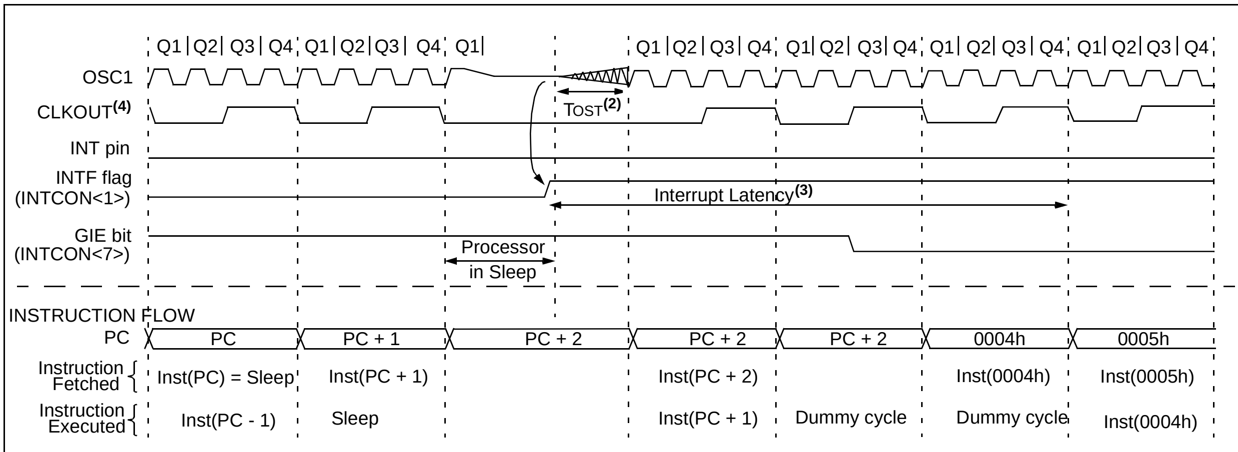
When global interrupts are disabled (i.e., GIE bit of the INTCON register is clear) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the $\overline{TO}$ bit will not be set and the $\overline{PD}$ bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a SLEEP instruction, the device will immediately wake-up from Sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the $\overline{TO}$ bit will be set, and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as a NOP.

When global interrupts are disabled, a CLRWDT instruction should be executed before a SLEEP instruction to ensure that the WDT is cleared.

FIGURE 15-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT(1)



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024TOSC (drawing not to scale). This delay does not apply to EC, RC and INTOSC Oscillator modes or Two-Speed Start-up (see **Section 3.6 "Two-Speed Clock Start-up Mode"**).

3: GIE = `1` assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = `0`, execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

15.7 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	If the code protection is turned off, the entire data EEPROM and Flash program memory will be erased by performing a bulk erase command. See the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information.

15.8 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

15.9 In-Circuit Serial Programming™ (ICSP™)

The PIC16F785/HV785 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five lines:

- Clock
- Data
- Power
- Ground
- Programming voltage

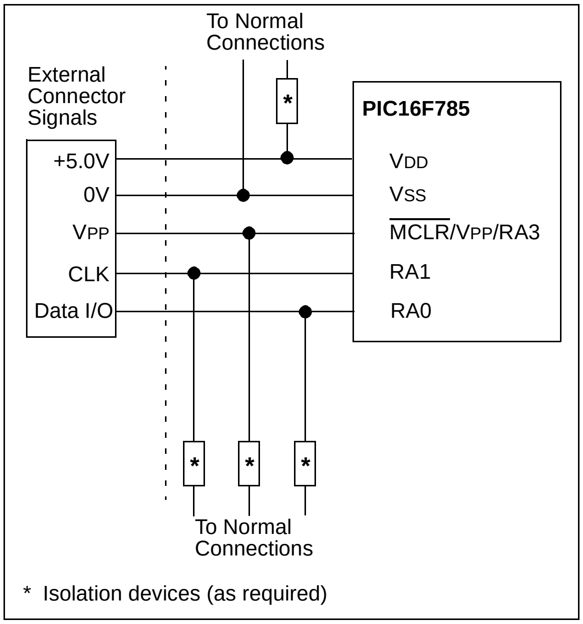
This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The device is placed into a Program/Verify mode by holding the RA0 and RA1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237) for more information. RA0 becomes the programming data and RA1 becomes the programming clock. Both RA0 and RA1 are Schmitt Trigger inputs in this mode.

After Reset, to place the device into Program/Verify mode, the Program Counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the "*PIC16F785/HV785 Memory Programming Specification*" (DS41237).

A typical In-Circuit Serial Programming connection is shown in Figure 15-11.

FIGURE 15-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



15.10 In-Circuit Debugger

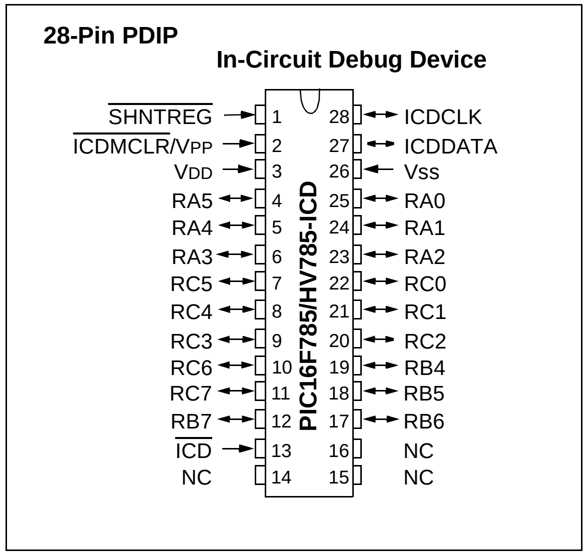
- In-circuit debugging requires clock, data and MCLR pins. A special 28-pin PIC16F785-ICD device is used with MPLAB® ICD 2 to provide separate clock, data and MCLR pins so that no pins are lost for these functions, leaving all 18 of the PIC16F785/HV785 I/O pins available to the user during debug operation.
- This special ICD device is mounted on the top of a header and its signals are routed to the MPLAB ICD 2 connector. On the bottom of the header is a 20-pin socket that plugs into the user's target via the 20-pin stand-off connector.
- When the ICD pin on the PIC16F785-ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 15-9 shows which features are consumed by the background debugger.

TABLE 15-9: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Data RAM	65h-70h, F0h
Program Memory	Address 0h must be `NOP` 700h-7FFh

For more information, see "*MPLAB® ICD 2 In-Circuit Debugger User's Guide*" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 15-12: 28-PIN ICD PINOUT



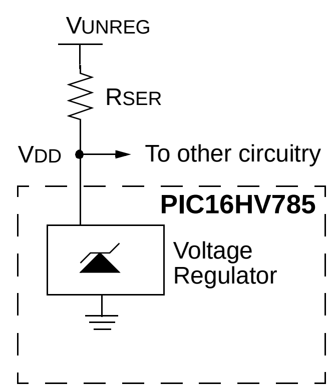
16.0 VOLTAGE REGULATOR

The PIC16HV785 includes a permanent internal 5 volt (nominal) shunt regulator in parallel with the V_{DD} pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the V_{DD} pin will share the regulated supply voltage and contribute to the total V_{DD} supply current (I_{LOAD}).

16.1 Regulator Operation

The regulator operates by maintaining a constant voltage at the V_{DD} pin by adjusting the regulator shunt current in response to variations of the V_{DD} supply load and the unregulated supply voltage. The regulator behaves like a fully compensated Zener diode. (See Figure 16-1).

FIGURE 16-1: REGULATOR



An external current limiting resistor, R_{SER}, located between the unregulated supply, V_{UNREG}, and the V_{DD} pin, drops the difference in voltage between V_{UNREG} and V_{DD}. R_{SER} must be between R_{MAX} and R_{MIN} as defined by Equation 16-1.

EQUATION 16-1: R_{SER} LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - V_{DD}) \cdot 1000}{1.05 \cdot (4\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MIN} - V_{DD}) \cdot 1000}{0.95 \cdot (50\ mA)}$$

Where:

- R_{MAX} = maximum value of R_{SER} (ohms)
- R_{MIN} = minimum value of R_{SER} (ohms)
- VU_{MIN} = minimum value of V_{UNREG}
- VU_{MAX} = maximum value of V_{UNREG}
- V_{DD} = regulated voltage (5V nominal)
- I_{LOAD} = maximum expected load current in mA including I/O pin currents and external circuits connected to V_{DD}.
- 1.05 = compensation for +5% tolerance of R_{SER}
- 0.95 = compensation for -5% tolerance of R_{SER}

16.2 Regulator Precautions

The total V_{DD} load current variation must be less than 46 mA so that it falls within the voltage regulator shunt current dynamic range. If the load current rises above the expected maximum, the regulator will be starved for current and go out of regulation causing V_{DD} to drop.

Since the regulator uses the band gap voltage as the regulated voltage reference, the VR voltage reference is permanently enabled in the PIC16HV785 device.

17.0 INSTRUCTION SET SUMMARY

The PIC16F785/HV785 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The format for each of the categories is presented in Figure 17-1, while the various opcode fields are summarized in Table 17-1.

Table 17-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with future products, do not use the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

17.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is always performed, even if the instruction is a Write command.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the RAIF flag.

TABLE 17-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 17-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13 — 8	7	6 — 0
OPCODE	d	f (FILE #)

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13 — 10	9 — 7	6 — 0
OPCODE	b (BIT #)	f (FILE #)

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13 — 8	7 — 0
OPCODE	k (literal)

k = 8-bit immediate value

CALL and GOTO instructions only

13 — 11	10 — 0
OPCODE	k (literal)

k = 11-bit immediate value

TABLE 17-2: PIC16F785/HV785 INSTRUCTION SET

Mnemonic,	Operands	Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	**1,2**
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	**1,2**
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	**2**
CLRW	–	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	**1,2**
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	**1,2**
DECFSZ	f, d	Decrement f, Skip if 0	1**(2)**	00	1011	dfff	ffff		**1,2,3**
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	**1,2**
INCFSZ	f, d	Increment f, Skip if 0	1**(2)**	00	1111	dfff	ffff		**1,2,3**
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	**1,2**
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	**1,2**
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	–	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	**1,2**
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	**1,2**
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	**1,2**
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		**1,2**
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	**1,2**
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		**1,2**
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		**1,2**
BTFSC	f, b	Bit Test f, Skip if Clear	1 **(2)**	01	10bb	bfff	ffff		**3**
BTFSS	f, b	Bit Test f, Skip if Set	1 **(2)**	01	11bb	bfff	ffff		**3**
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	–	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '`1`' for a pin configured as input and is driven low by an external device, the data will be written back with a '`0`'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = `1`), the prescaler will be cleared if assigned to the Timer0 module.

3: If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

Note:	Additional information on the mid-range instruction set is available in the "*PICmicro® Mid-Range MCU Family Reference Manual*" (DS33023).

 Preliminary

17.2 Instruction Descriptions

ADDLW **Add Literal and W**

Syntax:	[*label*] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal ‘k’ and the result is placed in the W register.

ADDWF **Add W and f**

Syntax:	[*label*] ADDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

ANDLW **AND Literal with W**

Syntax:	[*label*] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND’ed with the eight-bit literal ‘k’. The result is placed in the W register.

ANDWF **AND W with f**

Syntax:	[*label*] ANDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

BCF **Bit Clear f**

Syntax:	[*label*] BCF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit ‘b’ in register ‘f’ is cleared.

BSF **Bit Set f**

Syntax:	[*label*] BSF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit ‘b’ in register ‘f’ is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	skip if (f<b>) = `0`
Status Affected:	None
Description:	If bit 'b' in register 'f' is '`1`', the next instruction is executed. If bit 'b', in register 'f', is '`0`', the next instruction is discarded, and a `NOP` is executed instead, making this a two-cycle instruction.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	$0 \le f \le 127$ $0 \le b < 7$
Operation:	skip if (f<b>) = `1`
Status Affected:	None
Description:	If bit 'b' in register 'f' is '`0`', the next instruction is executed. If bit 'b' is '`1`', then the next instruction is discarded and a `NOP` is executed instead, making this a two-cycle instruction.

CALL	Call Subroutine
Syntax:	[*label*] CALL k
Operands:	$0 \le k \le 2047$
Operation:	(PC)+ 1→ TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>
Status Affected:	None
Description:	Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

CLRF	Clear f
Syntax:	[*label*] CLRF f
Operands:	$0 \le f \le 127$
Operation:	00h → (f) 1 → Z
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

CLRW	Clear W
Syntax:	[*label*] CLRW
Operands:	None
Operation:	00h → (W) 1 → Z
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

CLRWDT	Clear Watchdog Timer
Syntax:	[*label*] CLRWDT
Operands:	None
Operation:	00h → WDT 0 → WDT prescaler, 1 → $\overline{TO}$ 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	`CLRWDT` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

COMF	Complement f
Syntax:	[*label*] COMF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	$(\overline{f}) \rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are complemented. If ‘d’ is ‘0’, the result is stored in W. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	$0 \le k \le 2047$
Operation:	k → PC<10:0> PCLATH<4:3> → PC<12:11>
Status Affected:	None
Description:	`GOTO` is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. `GOTO` is a two-cycle instruction.

DECF	Decrement f
Syntax:	[*label*] DECF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination)
Status Affected:	Z
Description:	Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘1’, the next instruction is executed. If the result is ‘0’, then a `NOP` is executed instead, making it a two-cycle instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. If the result is ‘1’, the next instruction is executed. If the result is ‘0’, a `NOP` is executed instead, making it a two-cycle instruction.

IORLW — Inclusive OR Literal with W

Syntax:	[*label*] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF — Inclusive OR W with f

Syntax:	[*label*] IORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

MOVF — Move f

Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Encoding:	`00` | `1000` | `dfff` | `ffff`
Description:	The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If 'd' = 0, destination is W register. If 'd' = 1, the destination is file register 'f' itself. 'd' = 1 is useful to test a file register since status flag Z is affected.

MOVLW — Move Literal to W

Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Encoding:	`11` | `00xx` | `kkkk` | `kkkk`
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as 0's.

MOVWF — Move W to f

Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	(W) → (f)
Status Affected:	None
Encoding:	`00` | `0000` | `1fff` | `ffff`
Description:	Move data from W register to register 'f'.

NOP — No Operation

Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Encoding:	`00` | `0000` | `0xx0` | `0000`
Description:	No operation.

RETFIE — Return from Interrupt

Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Encoding:	`00` `0000` `0000` `1001`
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.

RETLW — Return with Literal in W

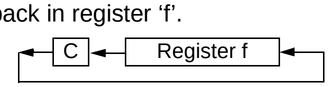
Syntax:	[*label*] RETLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	`11` `01xx` `kkkk` `kkkk`
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RETURN — Return from Subroutine

Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

RLF — Rotate Left f through Carry

Syntax:	[*label*] RLF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Encoding:	`00` `1101` `dfff` `ffff`
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is '`0`', the result is placed in the W register. If 'd' is '`1`', the result is stored back in register 'f'.



RRF — Rotate Right f through Carry

Syntax:	[*label*] RRF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Encoding:	`00` `1100` `dfff` `ffff`
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is '`0`', the result is placed in the W register. If 'd' is '`1`' the result is placed back in register 'f'.

SLEEP — Go into Standby mode

Syntax:	[*label*] SLEEP
Operands:	None
Operation:	00h → WDT, 0 → WDT prescaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Encoding:	`00` `0000` `0110` `0011`
Description:	The power-down Status bit, $\overline{PD}$ is cleared. Time out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBLW	Subtract W from Literal			
Syntax:	[*label*] SUBLW k			
Operands:	$0 \le k \le 255$			
Operation:	k - (W) → (W)			
Status Affected:	C, DC, Z			
Encoding:	11	110x	kkkk	kkkk
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register. C = 1; result is positive or zero C = 0; result is negative			

TRIS	Load TRIS Register			
Syntax:	[*label*] TRIS f			
Operands:	$5 \le f \le 6$			
Operation:	(W) → TRIS register f;			
Status Affected:	None			
Encoding:	00	0000	0110	0fff
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.			
Words:	1			
Cycles:	1			
<u>Example:</u>				
	To maintain upward compatibility with future PICmicro® products, do not use this instruction.			

SUBWF	Subtract W from f			
Syntax:	[*label*] SUBWF f,d			
Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Operation:	(f) - (W) → (dest)			
Status Affected:	C, DC, Z			
Encoding:	00	0010	dfff	ffff
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. C = 1; result is positive or zero C = 0; result is negative			

SWAPF	Swap Nibbles in f			
Syntax:	[*label*] SWAPF f,d			
Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)			
Status Affected:	None			
Encoding:	00	1110	dfff	ffff
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'.			

XORLW	Exclusive OR Literal with W			
Syntax:	[*label*] XORLW k			
Operands:	$0 \le k \le 255$			
Operation:	(W) .XOR. k → (W)			
Status Affected:	Z			
Encoding:	11	1010	kkkk	kkkk
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.			

XORWF	Exclusive OR W with f			
Syntax:	[*label*] XORWF f,d			
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$			
Operation:	(W) .XOR. (f) → (dest)			
Status Affected:	Z			
Encoding:	`00`	`0110`	`dfff`	`ffff`
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '`0`', the result is stored in the W register. If 'd' is '`1`' the result is stored back in register 'f'.			

NOTES:

18.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

18.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit micro-controller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

18.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

18.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 family of microcontrollers and dsPIC30F family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

18.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

18.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

18.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PICmicro MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, as well as internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

18.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

18.8 MPLAB ICE 4000 High-Performance In-Circuit Emulator

The MPLAB ICE 4000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro MCUs and dsPIC DSCs. Software control of the MPLAB ICE 4000 In-Circuit Emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high-speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, and up to 2 Mb of emulation memory.

The MPLAB ICE 4000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

18.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PICmicro MCUs and can be used to develop for these and other PICmicro MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

18.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PICmicro devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

18.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PICmicro devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

18.12 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PICmicro MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *“Product Selector Guide”* (DS00148) for the complete list of demonstration, development and evaluation kits.

19.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

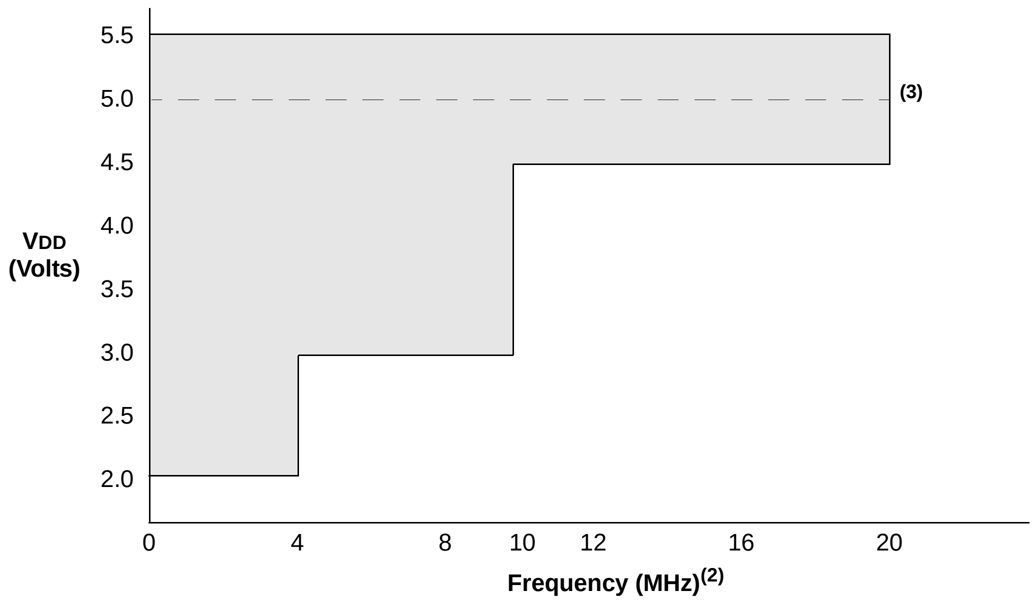
Ambient temperature under bias....................-40 to +125°C
Storage temperature .... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} .... -0.3 to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss ....-0.3 to +13.5V
Voltage on RB6 open-drain pin with respect to Vss ....-0.3 to +8.5V
Voltage on all other pins with respect to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Total power dissipation**(1)** (PDIP and SOIC)....................800 mW
Total power dissipation**(1)** (SSOP)....................600 mW
Maximum current out of V_{SS} pin ....300 mA
Maximum current into V_{DD} pin ....250 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})....................±20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD})....................±20 mA
Maximum output current sunk by any I/O pin....................25 mA
Maximum output current sourced by any I/O pin ....25 mA
Maximum current sunk by PORTA, PORTB, and PORTC (combined) ....200 mA
Maximum current sourced PORTA, PORTB, and PORTC (combined)....................200 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$.

† **NOTICE**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

FIGURE 19-1: PIC16F785/HV785 WITH ANALOG DISABLED VOLTAGE-FREQUENCY GRAPH, -40°C $\leq$ TA $\leq$ +125°C(2)



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: Frequency denotes system clock frequency. When using the HFINTOSC the system clock is after the postscaler.

3: The internal shunt regulator of the PIC16HV785 keeps VDD at or below 5.0V (nominal).

19.1 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for industrial -40°C ≤ T_A ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	V_{DD}	**Supply Voltage(2)**					F_{OSC} ≤ 4 MHz:
D001			2.0	—	5.5	V	PIC16F785 with A/D off
D001A			2.2	—	5.5	V	PIC16F785 with A/D on, 0°C to +125°C
D001B			2.5	—	5.5	V	PIC16F785 with A/D on, -40°C to +125°C
D001C			3.0	—	5.5	V	4 MHz ≤ F_{OSC} ≤ 10 MHz
D001D			4.5	—	5.5	V	10 MHz ≤ F_{OSC} ≤ 20 MHz
D002	V_{DR}	**RAM Data Retention Voltage(1)**	1.5*	—	—	V	Device in Sleep mode
D003	V_{POR}	V_{DD} voltage above which the internal **POR releases**	—	1.8	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D003A	V_{PARM}	V_{DD} voltage below which the internal **POR rearms**	—	1.0	—	V	See **Section 15.2.1 "Power-On Reset"** for details.
D004	S_{VDD}	V_{DD} **Rise Rate** to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See **Section 15.2.1 "Power-On Reset"** for details.
D005	V_{BOR}	**Brown-out Reset**	—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in Sleep mode without losing RAM data.

2: Maximum supply voltage is V_{SHUNT} for PIC16HV785 device (see Table 19-14).

19.2 DC Characteristics: PIC16F785/HV785-I (Industrial)(1), (2)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions
D010	**Supply Current (IDD)**	—	9	TBD	μA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	17	TBD	μA	3.0	
		—	33	TBD	μA	5.0	
D011		—	110	TBD	μA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	190	TBD	μA	3.0	
		—	330	TBD	μA	5.0	
D012		—	220	TBD	μA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	300	TBD	μA	3.0	
		—	540	TBD	μA	5.0	
D013		—	70	TBD	μA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	140	TBD	μA	3.0	
		—	260	TBD	μA	5.0	
D014		—	180	TBD	μA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	320	TBD	μA	3.0	
		—	580	TBD	μA	5.0	
D015		—	9	TBD	μA	2.0	FOSC = 31 kHz INTRC mode
		—	18	TBD	μA	3.0	
		—	35	TBD	mA	5.0	
D016		—	340	TBD	μA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	TBD	μA	3.0	
		—	0.8	TBD	mA	5.0	
D017		—	180	TBD	μA	2.0	FOSC = 4 MHz EXTRC mode
		—	320	TBD	μA	3.0	
		—	580	TBD	μA	5.0	
D018		—	2.8	TBD	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	3.3	TBD	mA	5.0	

Legend: TBD = To Be Determined.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD. When A/D is off, it will not consume any current other than leakage current. the power-down current spec includes any such leakage from the A/D module.

19.2 DC Characteristics: PIC16F785/HV785-I (Industrial)(1), (2) (Continued)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	
D020	**Power-down Base Current (IPD)(4)**	—	25	TBD	nA	2.0	WDT, BOR, Comparators, VREF, T1OSC, Op Amps and VR disabled
		—	45	TBD	nA	3.0	
		—	85	TBD	nA	5.0	
D021		—	0.3	TBD	μA	2.0	WDT Current(3)
		—	1.2	TBD	μA	3.0	
		—	2.2	TBD	μA	5.0	
D022		—	50	TBD	μA	3.0	BOR Current(3)
		—	100	TBD	μA	5.0	
D023		—	150	TBD	μA	2.0	Comparator Current(3) CxSP = 1
		—	170	TBD	μA	3.0	
		—	200	TBD	μA	5.0	
D023A		—	3.3	TBD	μA	2.0	Comparator Current(3) CxSP = 0
		—	6.1	TBD	μA	3.0	
		—	35	TBD	μA	5.0	
D024		—	58	TBD	μA	2.0	CVREF Current(3) Low Range
		—	85	TBD	μA	3.0	
		—	104	TBD	μA	5.0	
D024A		—	35	TBD	μA	2.0	CVREF Current(3) High Range (VRR = 0)
		—	45	TBD	μA	3.0	
		—	80	TBD	μA	5.0	
D025		—	1.8	TBD	μA	2.0	T1 OSC Current(3)
		—	2.0	TBD	μA	3.0	
		—	3.2	TBD	μA	5.0	
D026		—	1.2	TBD	nA	3.0	A/D Current(3) (not converting)
		—	2.2	TBD	nA	5.0	
D027		—	10	TBD	μA	2.0	VR Current(3)
		—	11	TBD	μA	3.0	
		—	12	TBD	μA	5.0	
D028		—	150	TBD	μA	3.0	Op Amp Current(3)
		—	250	TBD	μA	5.0	

Legend: TBD = To Be Determined.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD. When A/D is off, it will not consume any current other than leakage current. the power-down current spec includes any such leakage from the A/D module.

19.3 DC Characteristics: PIC16F785/HV785-E (Extended)(1), (2)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	
D010E	**Supply Current (IDD)**	—	9	TBD	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	17	TBD	µA	3.0	
		—	33	TBD	µA	5.0	
D011E		—	110	TBD	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	190	TBD	µA	3.0	
		—	330	TBD	µA	5.0	
D012E		—	220	TBD	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	300	TBD	µA	3.0	
		—	540	TBD	µA	5.0	
D013E		—	70	TBD	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	140	TBD	µA	3.0	
		—	260	TBD	µA	5.0	
D014E		—	180	TBD	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	320	TBD	µA	3.0	
		—	580	TBD	µA	5.0	
D015E		—	9	TBD	µA	2.0	FOSC = 31 kHz INTRC mode
		—	18	TBD	µA	3.0	
		—	35	TBD	mA	5.0	
D016E		—	340	TBD	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	TBD	µA	3.0	
		—	0.8	TBD	mA	5.0	
D017E		—	180	TBD	µA	2.0	FOSC = 4 MHz EXTRC mode
		—	320	TBD	µA	3.0	
		—	580	TBD	µA	5.0	
D018E		—	2.8	TBD	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	3.3	TBD	mA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD. When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

19.3 DC Characteristics: PIC16F785/HV785-E (Extended)(1), (2) (Continued)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions: VDD	Conditions
D020E	Power-down Base Current (IPD)(4)	—	25	TBD	nA	2.0	WDT, BOR, Comparators, VREF, T1OSC, Op Amps and VR disabled
		—	45	TBD	nA	3.0	
		—	85	TBD	nA	5.0	
D021E		—	0.3	TBD	μA	2.0	WDT Current(3)
		—	1.2	TBD	μA	3.0	
		—	2.2	TBD	μA	5.0	
D022E		—	50	TBD	μA	3.0	BOR Current(3)
		—	100	TBD	μA	5.0	
D023E		—	50	TBD	μA	2.0	Comparator Current(3) CxSP = 1
		—	170	TBD	μA	3.0	
		—	200	TBD	μA	5.0	
D023E		—	3.3	TBD	μA	2.0	Comparator Current(3) CxSP = 0
		—	6.1	TBD	μA	3.0	
		—	35	TBD	μA	5.0	
D024E		—	58	TBD	μA	2.0	CVREF Current(3) Low Range
		—	85	TBD	μA	3.0	
		—	104	TBD	μA	5.0	
D024E		—	35	TBD	μA	2.0	CVREF Current(3) High Range
		—	45	TBD	μA	3.0	
		—	80	TBD	μA	5.0	
D025E		—	1.8	TBD	μA	2.0	T1 Osc Current(3)
		—	2.0	TBD	μA	3.0	
		—	3.2	TBD	μA	5.0	
D026E		—	1.2	TBD	nA	3.0	A/D Current(3) (not converting)
		—	2.2	TBD	nA	5.0	
D027E		—	10	TBD	μA	3.0	VR Current(3)
		—	11	TBD	μA	3.0	
		—	12	TBD	μA	5.0	
D028E		—	150	TBD	μA	3.0	Op Amp Current(3)
		—	250	TBD	μA	5.0	

Legend: TBD = To Be Determined

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

3: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

4: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD. When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

19.4 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature-40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			VSS	—	0.15 VDD	V	Otherwise
D031		with Schmitt Trigger buffer	VSS	—	0.2 VDD	V	Entire range
D032		$\overline{\text{MCLR}}$, OSC1 (RC mode)(1)	VSS	—	0.2 VDD	V	
D033		OSC1 (XT and LP modes)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)	VSS	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			(0.25 VDD + 0.8)	—	VDD	V	Otherwise
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	Entire range
D042		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	**(Note 1)**
D070	IPUR	**PORTA Weak Pull-up Current**	50*	250	400*	μA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	±0.1	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		Analog inputs	—	±0.1	±1	μA	VSS ≤ VPIN ≤ VDD
D060B		VREF	—	±0.1	±1	μA	VSS ≤ VPIN ≤ VDD
D061		$\overline{\text{MCLR}}$(3)	—	±0.1	±5	μA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	±0.1	±5	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
D083		OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.) IOL = 1.2 mA, VDD = 4.5V (Ext.)
	VOH	**Output High Voltage**					
D090		I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V
D092		OSC2/CLKOUT (RC mode)	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V (Ind.) IOH = -1.0 mA, VDD = 4.5V (Ext.)
D193*	VOD	**Open-Drain High Voltage**	—	—	8.5	V	RB6 pin

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.
† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
2: Negative current is defined as current sourced by the pin.
3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
4: See **Section 14.4.1 "Using the Data EEPROM"** on page 105.

19.4 DC Characteristics: PIC16F785/HV785-I (Industrial), PIC16F785/HV785-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature-40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
		Data EEPROM Memory					
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON1 to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh(4)	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	EP	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.
† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
2: Negative current is defined as current sourced by the pin.
3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
4: See **Section 14.4.1 "Using the Data EEPROM"** on page 105.

19.5 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

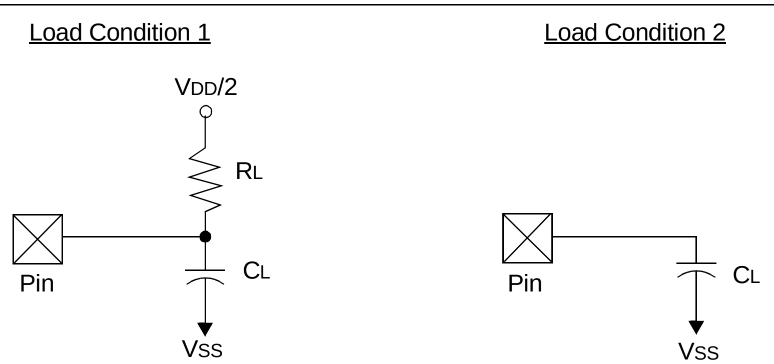
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 19-2: LOAD CONDITIONS



Legend: R_L = 464Ω

C_L = 50 pF for all pins

15 pF for OSC2 output

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FIGURE 19-3: EXTERNAL CLOCK TIMING

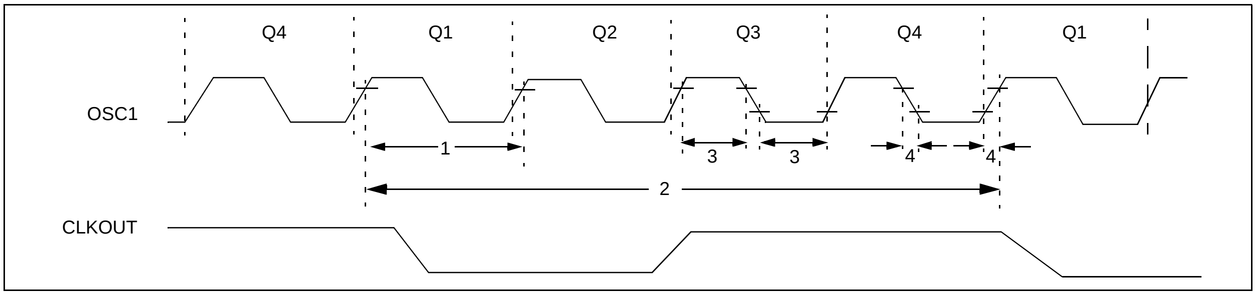

TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency(1)	—	32.768	—	kHz	LP mode (complementary input only)
			DC	—	4	MHz	XT mode
			DC	—	20	MHz	HS mode
			DC	—	20	MHz	EC mode
		Oscillator Frequency(1)	—	32.768	—	kHz	LP Osc mode
			—	4	—	MHz	INTOSC mode
			DC	—	4	MHz	RC Osc mode
			0.1	—	4	MHz	XT Osc mode
			1	—	20	MHz	HS Osc mode
1	TOSC	External CLKIN Period(1)	—	0.3052	—	µs	LP mode (complementary input only)
			50	—	∞	ns	HS Osc mode
			50	—	∞	ns	EC Osc mode
			250	—	∞	ns	XT Osc mode
		Oscillator Period(1)	—	0.3052	—	µs	LP Osc mode
			—	250	—	ns	INTOSC mode
			250	—	—	ns	RC Osc mode
			250	—	10,000	ns	XT Osc mode
			50	—	1,000	ns	HS Osc mode
2	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC
3	TosL, TosH	External CLKIN (OSC1) High External CLKIN Low	2*	—	—	µs	LP oscillator, TOSC L/H duty cycle
			20*	—	—	ns	HS oscillator, TOSC L/H duty cycle
			100 *	—	—	ns	XT oscillator, TOSC L/H duty cycle
4	TosR, TosF	External CLKIN Rise External CLKIN Fall	—	—	50*	ns	LP oscillator
			—	—	25*	ns	XT oscillator
			—	—	15*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

FIGURE 19-4: CLKOUT AND I/O TIMING

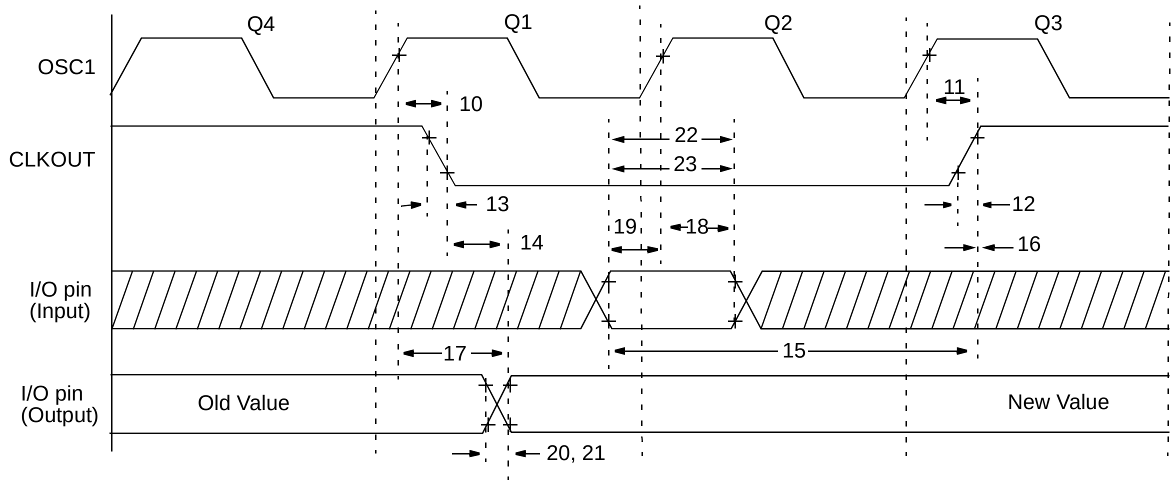

TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TOSH2CKL	OSC1↑ to CLKOUT↓	—	75	200	ns	**(Note 1)**
11	TOSH2CKH	OSC1↑ to CLKOUT↑	—	75	200	ns	**(Note 1)**
12	TCKR	CLKOUT rise time	—	35	100	ns	**(Note 1)**
13	TCKF	CLKOUT fall time	—	35	100	ns	**(Note 1)**
14	TCKL2IOV	CLKOUT↓ to Port out valid	—	—	20	ns	**(Note 1)**
15	TIOV2CKH	Port input valid before CLKOUT↑	TOSC + 200 ns	—	—	ns	**(Note 1)**
16	TCKH2IOI	Port input hold after CLKOUT↑	0	—	—	ns	**(Note 1)**
17	TOSH2IOV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	TOSH2IOI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	TIOV2OSH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TIOR	Port output rise time	—	10	40	ns	
21	TIOF	Port output fall time	—	10	40	ns	
22	TINP	INT pin high or low time	25	—	—	ns	
23	TRBP	PORTA interrupt-on-change high or low time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

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TABLE 19-3: PRECISION INTERNAL OSCILLATOR PARAMETERS

Param No.	Sym	Characteristic	Freq. Tolerance	Min	Typ†	Max	Units	Conditions
F10	FOSC	Internal Calibrated INTOSC Frequency(1)	±1%	7.92	8.00	8.08	MHz	VDD = 3.5V, 25°C
			±2%	7.84	8.00	8.16	MHz	2.5V ≤ VDD ≤ 5.5V 0°C ≤ TA ≤ +85°C
			±5%	7.60	8.00	8.40	MHz	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (Ind.) -40°C ≤ TA ≤ +125°C (Ext.)
F14	TIOSCST	Oscillator wake-up from Sleep start-up time*	—	—	10.3	TBD	µs	VDD = 2.0V, -40°C to +85°C
			—	—	9.0	TBD	µs	VDD = 3.0V, -40°C to +85°C
			—	—	6.5	TBD	µs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

FIGURE 19-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

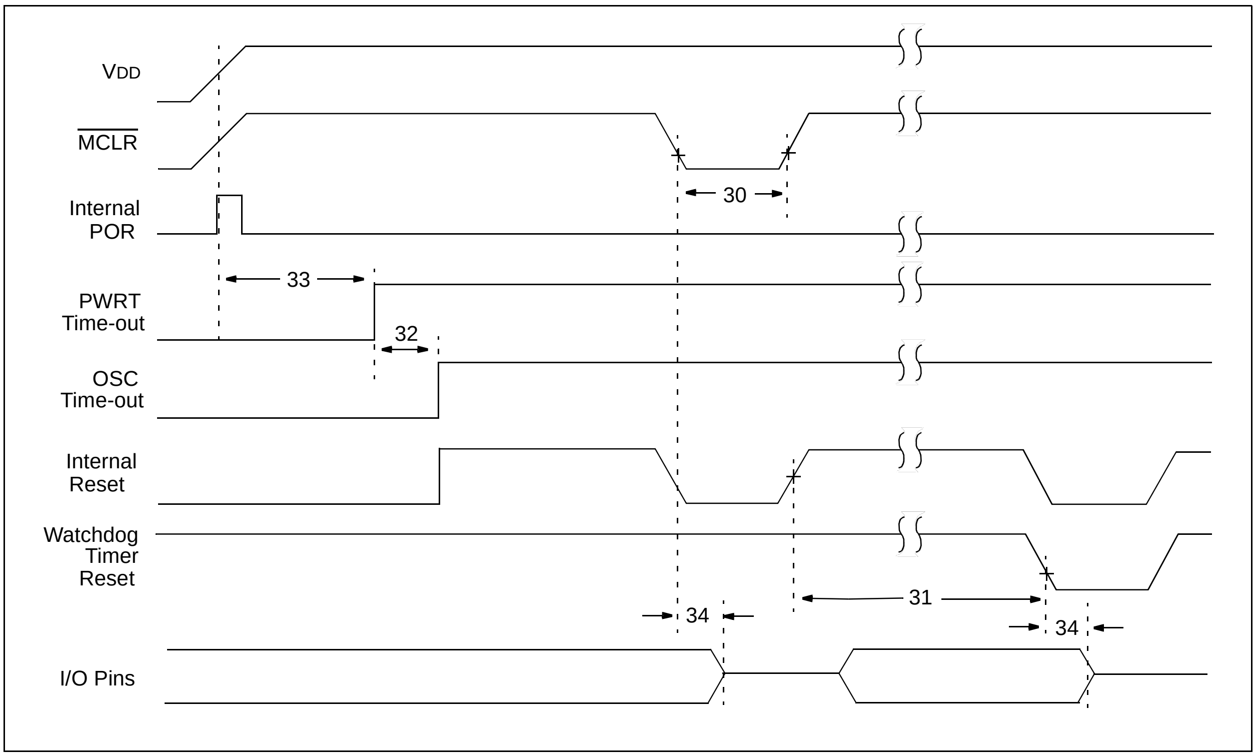
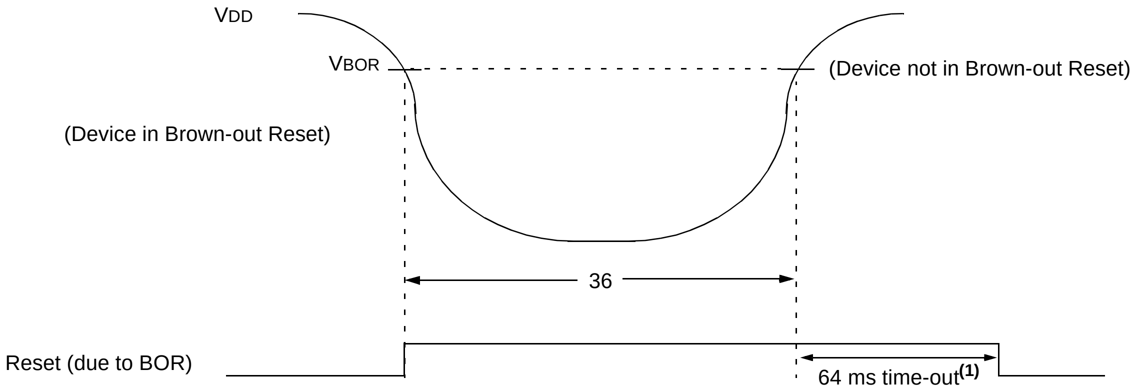


FIGURE 19-6: BROWN-OUT RESET TIMING AND CHARACTERISTICS



Note 1: 64 ms delay only if $\overline{\text{PWRTE}}$ bit in Configuration Word is programmed to '0'.

TABLE 19-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	T_{MCL}	$\overline{\text{MCLR}}$ Pulse Width (low)	2 11	— 18	— 24	µs ms	VDD = 5.0V, -40°C to +85°C Extended temperature
31	T_{WDT}	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5.0V, -40°C to +85°C Extended temperature
32	T_{OST}	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	T_{PWRT}	Power-up Timer Period	28* TBD	64 TBD	132* TBD	ms ms	VDD = 5.0V, -40°C to +85°C Extended Temperature
34	T_{IOZ}	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	µs	
35	V_{BOR}	Brown-out Reset Voltage	2.025	—	2.175	V	
36	T_{BOR}	Brown-out Reset Pulse Width	100*	—	—	µs	$V_{DD} \le V_{BOR}$ (D005)

Legend: TBD = To Be Determined.
* These parameters are characterized but not tested.
† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-7: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

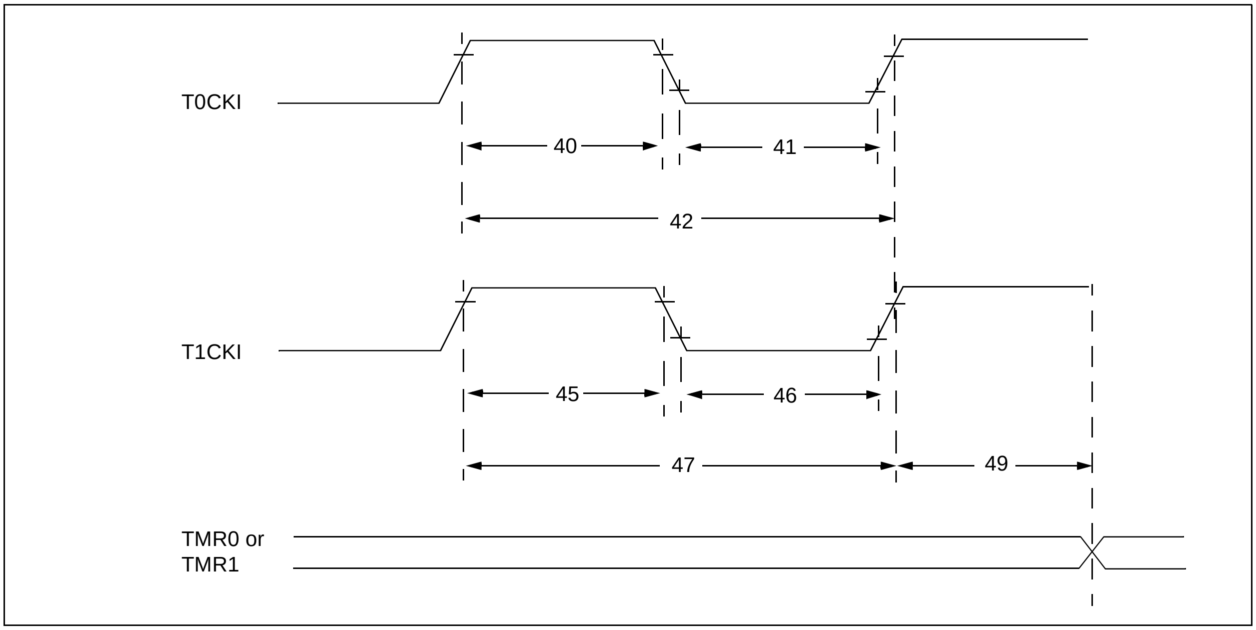


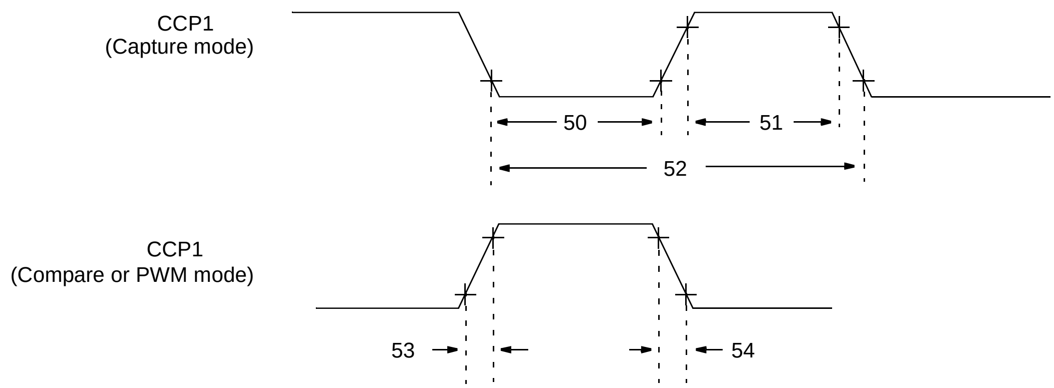
TABLE 19-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	—	200*	kHz	
49	TCKEZTMR1	Delay from external clock edge to timer increment		2 TOSC*	—	7 TOSC*	—	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-8: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 19-2 for load conditions.

TABLE 19-6: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
50*	TCCL	CCP1 input low time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
51*	TCCH	CCP1 input high time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
52*	TCCP	CCP1 input period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1,4 or 16)
53*	TCCR	CCP1 output rise time		—	25	50	ns	
54*	TCCF	CCP1 output fall time		—	25	45	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 19-7: COMPARATOR SPECIFICATIONS

Comparator Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
C01	V_{OS}	Input Offset Voltage	—	±5	TBD	mV	
C02	V_{CM}	Input Common Mode Voltage	0	—	V_{DD} – 1.5	V	
C03	I_{LC}	Input Leakage Current	—	—	200*	nA	
C04	C_{MRR}	Common Mode Rejection Ratio	+70*	—	—	dB	
C05	T_{RT}	Response Time(1)	— —	— —	20* 40*	ns ns	Internal Output to pin

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (V_{DD} – 1.5)/2, while the other input transitions from V_{SS} to V_{DD} – 1.5V.

TABLE 19-8: COMPARATOR VOLTAGE REFERENCE (CV_{REF}) SPECIFICATIONS

Comparator Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
CV01	CV_{RES}	Resolution	— —	V_{DD}/24* V_{DD}/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV02		Absolute Accuracy	— —	— —	±1/4* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03		Unit Resistor Value (R)	—	2K*	—	Ω	
CV04		Settling Time(1)	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

TABLE 19-9: VOLTAGE REFERENCE (VR) SPECIFICATIONS

VR Voltage Reference Specifications			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C Operating Voltage 3.0V ≤ V_{DD} ≤ 5.5V				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VR01	V_{ROUT}	VR voltage output	1.188 1.176 1.164	1.200 1.200 1.200	1.212 1.224 1.236	V V V	T_A = 25°C 0°C ≤ T_A ≤ +85°C -40°C ≤ T_A ≤ +125°C
VR02*	TCV_{OUT}	Voltage drift temperature coefficient	—	150	TBD	ppm/°C	
VR03*	ΔV_{ROUT}/ ΔV_{DD}	Voltage drift with respect to V_{DD} regulation	—	200	—	μV/V	
VR04	T_{STABLE}	Settling Time	—	10	100*	μs	
VR05*	I_{VROUT}	VR output current	—	—	TBD	μA	Unbuffered 1.2V out

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

TABLE 19-10: VOLTAGE REFERENCE OUTPUT (V_{REF}) BUFFER SPECIFICATIONS

Voltage Reference Output Buffer Specifications			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +125°C Operating voltage 3.0V ≤ V_{DD} ≤ 5.5V				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
VB01*	CL	External capacitor load	—	—	200	pF	
VB02*	$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	—	1	TBD	mV/mA	V_{REF} = 1.2V, I_{REF} = ±1 ma
			—	1	TBD		V_{REF} = 0.5V, I_{REF} = ±1 ma
			—	1	TBD		V_{REF} = 3.6V, I_{REF} = ±1 ma

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

TABLE 19-11: OPERATIONAL AMPLIFIER (OPA) MODULE DC SPECIFICATIONS

OPA DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** V_{CM} = 0V, V_{OUT} = V_{DD}/2, V_{DD} = 5.0V, V_{SS} = 0V, C_L = 50pF, R_L = 100k Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
OPA01	V_{OS}	**Input Offset Voltage**	—	±5	—	mV	
		Input current and impedance					
OPA02*	I_B	Input bias current	—	±2*	—	nA	
OPA03*	I_{OS}	Input offset bias current	—	±1*	—	pA	
		Common Mode					
OPA04*	V_{CM}	Common mode input range	V_{SS}	—	V_{DD} – 1.4	V	V_{DD} = 5.0V
OPA05*	CMR	Common mode rejection	TBD	70	—	dB	V_{CM} = V_{DD}/2, Freq. = DC
		Open Loop Gain					
OPA06A*	A_{OL}	DC Open loop gain	—	90	—	dB	No load
OPA06B*	A_{OL}	DC Open loop gain	—	60	—	dB	Standard load
		Output					
OPA07*	Vout	Output voltage swing	V_{SS}+100	—	V_{DD} – 100	mV	To V_{DD}/2 (20 kΩ connected to V_{DD}, 20 kΩ + 20 pF to Vss)
OPA08*	Isc	Output short circuit current	—	25	TBD	mA	
		Power Supply					
OPA10	PSR	Power supply rejection	80	—	—	dB	

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

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TABLE 19-12: OPERATIONAL AMPLIFIER (OPA) MODULE AC SPECIFICATIONS

OPA AC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) V_{CM} = 0V, V_{OUT} = $V_{DD}/2$, V_{DD} = 5.0V, V_{SS} = 0V, C_L = 50 pF, R_L = 100k Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
OPA11*	GBWP	Gain bandwidth product	—	3	—	MHz	
OPA12*	T_{ON}	Turn on time	—	10	TBD	µs	
OPA13*	Θ_M	Phase margin	—	60	—	deg	
OPA14*	SR	Slew rate	2	—	—	V/µs	

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

TABLE 19-13: TWO-PHASE PWM DEAD TIME DELAY SPECIFICATIONS

Dead Time Delay Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
PW01*	T_{DLY}	Dead Time Delay	TBD	150	TBD	ns	F_{OSC} = 4 MHz, maximum delay, Complementary mode

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

TABLE 19-14: SHUNT REGULATOR SPECIFICATIONS (PIC16HV785 only)

SHUNT REGULATOR CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +125°C				
Param No.	**Symbol**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
SR01	V_{SHUNT}	Shunt Voltage	4.25	5	5.25	V	
SR02	I_{SHUNT}	Shunt Current	4	—	50	mA	
SR03*	T_{SETTLE}	Settling Time	—	—	150	ns	To 1% of final value
SR04*	C_{LOAD}	Load Capacitance	0.01	—	10	µF	Bypass capacitor on V_{DD} pin
SR05*	ΔI_{SNT}	Regulator operating current	—	—	180	µA	Includes band gap reference current

Legend: TBD = To Be Determined
* These parameters are characterized but not tested.

TABLE 19-15: PIC16F785/HV785 A/D CONVERTER CHARACTERISTICS:

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A03	EIL	Integral Error	—	—	±1	LSb	VREF = 5.0V (external)
A04	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.0V (external)
A06	EOFF	Offset Error	—	—	±1	LSb	VREF = 5.0V (external)
A07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.0V (external)
A20 A20A	VREF	Reference Voltage	2.2(4) 1.0	—	— VDD + 0.3	V	 Absolute minimum to ensure 10-bit accuracy
A25	VAIN	Analog Input Voltage	VSS	—	VREF(5)	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current*(3)	— —	— —	150 1	μA mA	During VAIN acquisition. Based on differential of VHOLD to VAIN. Transient during A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes Integral, Differential, Offset and Gain Errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: VREF current is from external VREF or VDD pin, whichever is selected as reference input.

4: Only limited when VDD is at or below 2.5V. If VDD is above 2.5V, VREF is allowed to go as low as 1.0V.

5: Analog input voltages are allowed up to VDD, however the conversion accuracy is limited to VSS to VREF.

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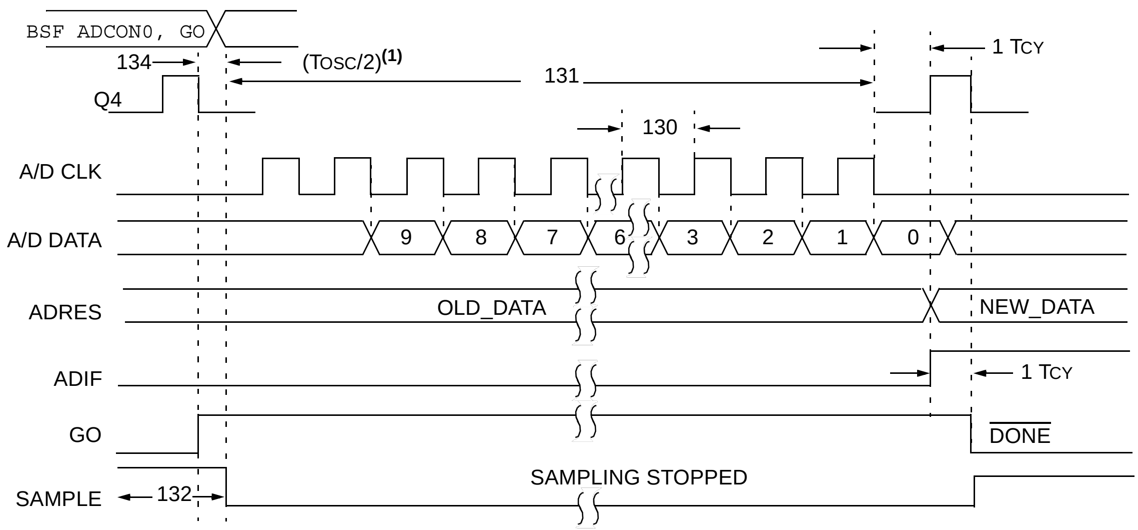
FIGURE 19-9: PIC16F785/HV785 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 19-16: PIC16F785/HV785 A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6	—	—	μs	TOSC-based, VREF ≥ 3.0V
			3.0*	—	—	μs	TOSC-based, VREF full range
130	TAD	A/D Internal RC Oscillator Period					ADCS<1:0> = `11` (RC mode)
			3.0*	6.0	9.0*	μs	At VDD = 2.5V
			2.0*	4.0	6.0*	μs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO bit to new data in A/D result register
132	TACQ	Acquisition Time	**(Note 2)**	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

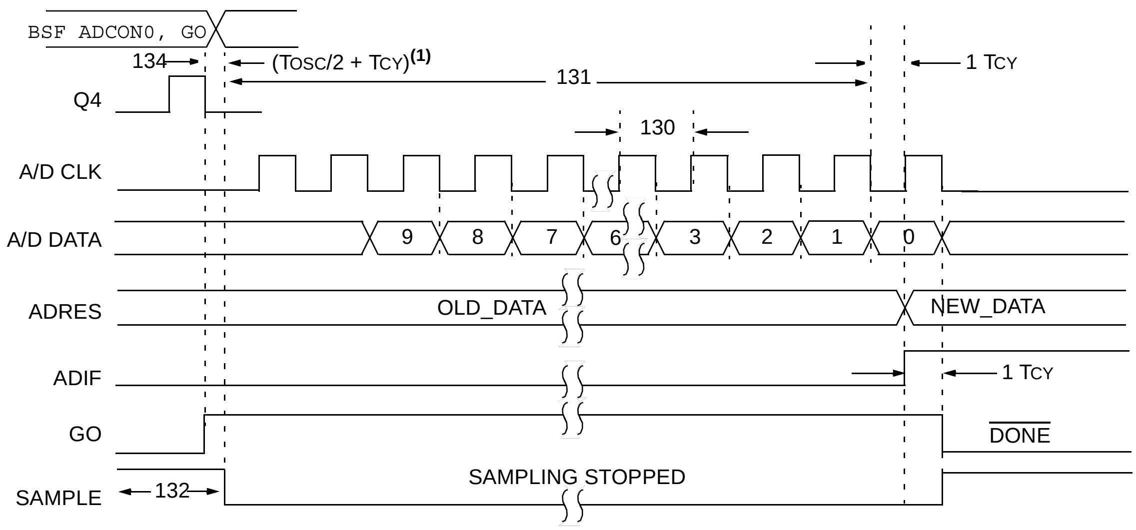
* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See **Section 12.2 “A/D Acquisition Requirements”** for minimum conditions.

FIGURE 19-10: PIC16F785/HV785 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

TABLE 19-17: PIC16F785/HV785 A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Internal RC Oscillator Period					ADCS<1:0> = `11` (RC mode)
			3.0*	6.0	9.0*	μs	At VDD = 2.5V
			2.0*	4.0	6.0*	μs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	
132	TACQ	Acquisition Time	**(Note 2)**	11.5	—	μs	
			5*	—	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following TCY cycle.

2: See Table 12-1 for minimum conditions.

20.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs are not available at this time.

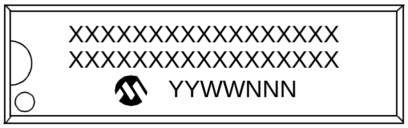
NOTES:

21.0 PACKAGING INFORMATION

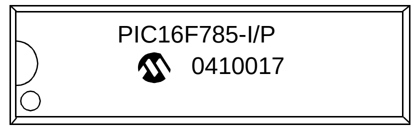
21.1 Package Marking Information

The following sections give the technical details of the packages.

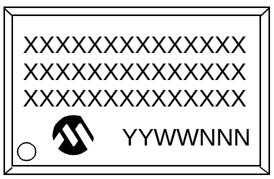
20-Lead PDIP



Example

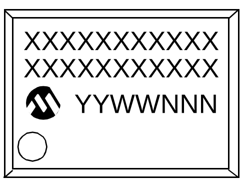


20-Lead SOIC (.300”)

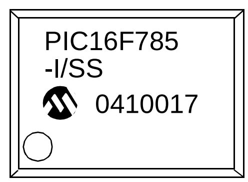


Example

20-Lead SSOP



Example



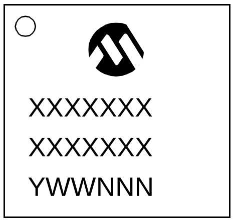
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

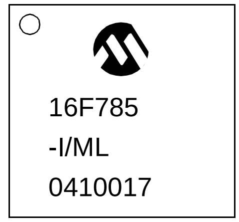
* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Marking Information (Cont'd)

20-Lead QFN

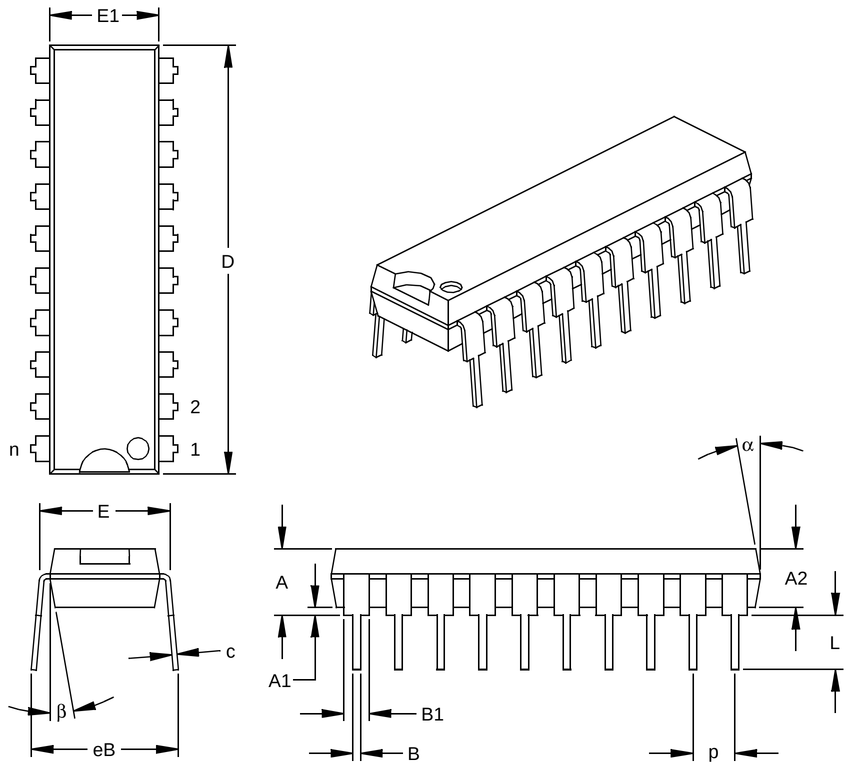


Example



 Preliminary

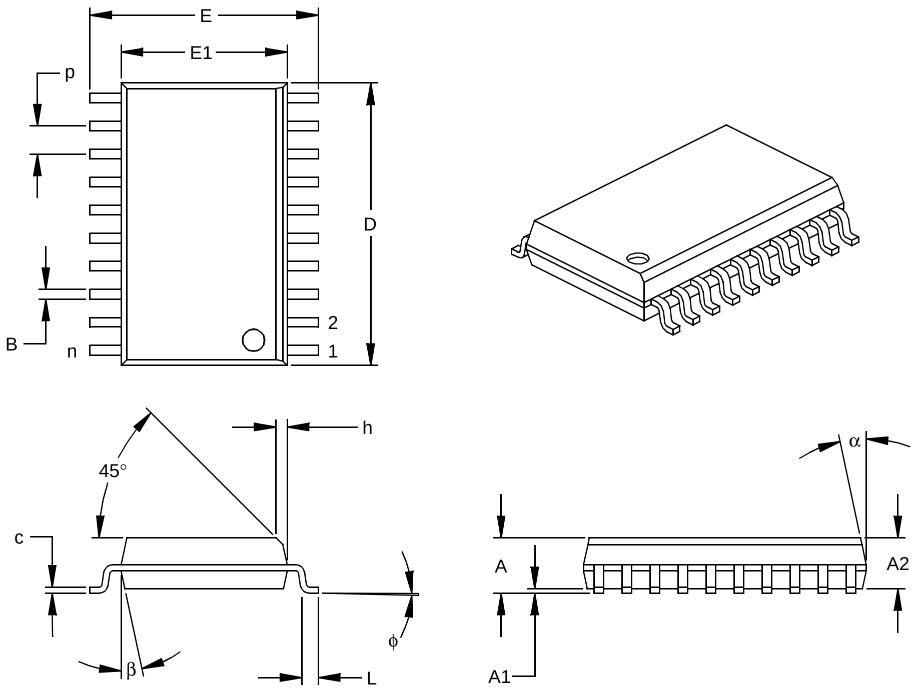
20-Lead Plastic Dual In-line (P) – 300 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.295	.310	.325	7.49	7.87	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	1.025	1.033	1.040	26.04	26.24	26.42
Tip to Seating Plane	L	.120	.130	.140	3.05	3.30	3.56
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.055	.060	.065	1.40	1.52	1.65
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-019

20-Lead Plastic Small Outline (SO) – Wide, 300 mil Body (SOIC)

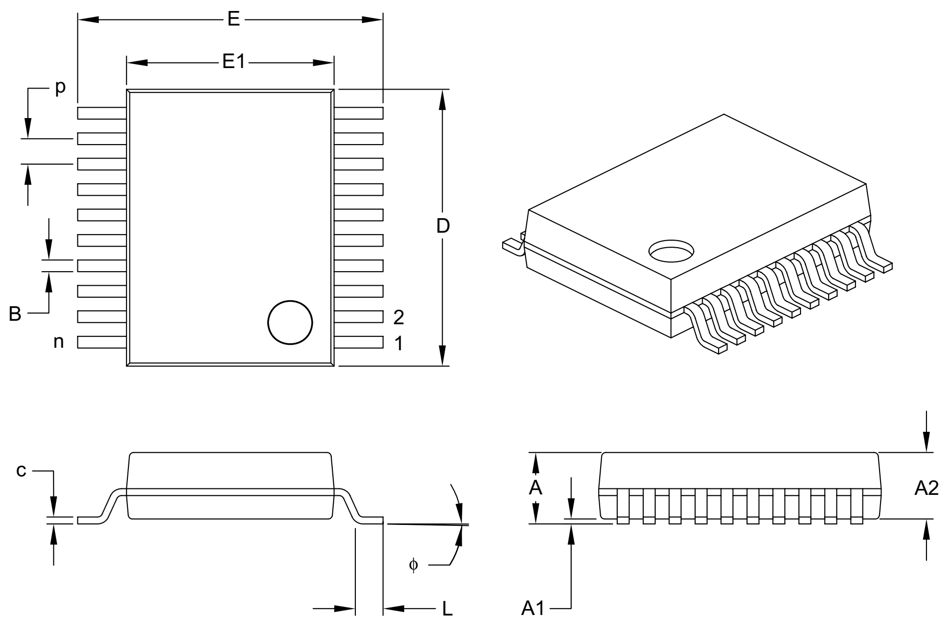


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff **§**	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.496	.504	.512	12.60	12.80	13.00
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-094

 Preliminary

20-Lead Plastic Shrink Small Outline (SS) – 209 mil Body, 5.30 mm (SSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			.065	
Overall Height	A	–	–	.079	–	–	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	–	–	0.05	–	–
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.295	6.90	7.20	7.50
Foot Length	L	0.22	0.30	0.37	0.55	0.75	0.95
Lead Thickness	c	.004	–	.010	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°	0°	4°	8°
Lead Width	B	.009	–	.015	0.22	–	0.38

* Controlling Parameter

Notes:

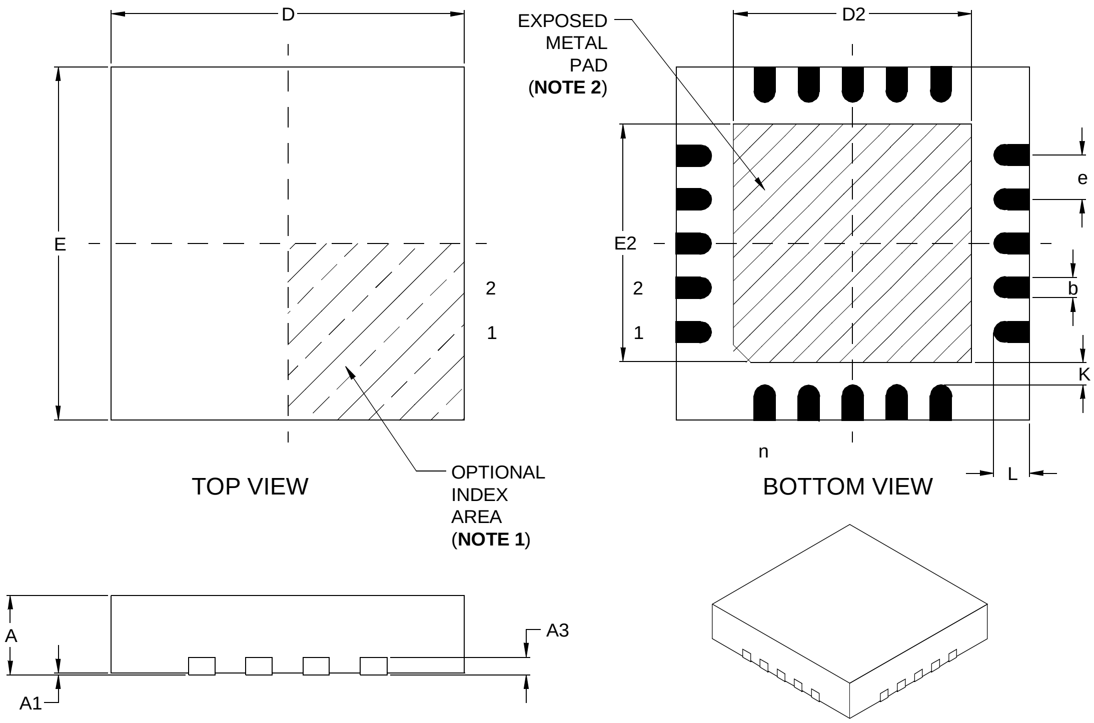
Dimensions D and E1 do no include mold flash or protrusions. Mold flash or protrusions shall not exceed 010" (0.254mm) per side.

JEDEC Equivalent: MO-150

Drawing No. C04-072

Revised 8-27-04

20-Lead Plastic Quad Flat No Lead Package (ML) 4x4x0.9 mm Body (QFN) – Saw Singulated



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	e		.020 BSC			0.50 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Contact Thickness	A3		.008 REF			0.20 REF	
Overall Width	E		.157 BSC			4.00 BSC	
Exposed Pad Width	E2	.102	.106	.110	2.60	2.70	2.80
Overall Length	D		.157 BSC			4.00 BSC	
Exposed Pad Length	D2	.102	.106	.110	2.60	2.70	2.80
Contact Width	b	.007	.010	.012	0.18	0.25	0.30
Contact Length §	L	.012	.016	.020	0.30	0.40	0.50
Contact-to-Exposed Pad §	K	.008	–	–	0.20	–	–

***** Controlling Parameter
§ Significant Characteristic

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exposed pad varies according to die attach paddle size.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M
REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M
JEDEC equivalent: Not Registered
Drawing No. C04-126

Revised 09-12-05

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Updates throughout document.

Revision C

Revised part number to include “HV785”; Added PWM Setup Example; Added Voltage Regulator secton.

Revision D

Revised VROUT min./max. limits in Table 19-9.

APPENDIX B: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from the PIC16F684 PICmicro device to the PIC16F785/HV785.

B.1 PIC16F684 to PIC16F785/HV785

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F684	PIC16F785
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	2048	2048
SRAM (bytes)	128	128
A/D Resolution	10-bit	10-bit
Data EEPROM (bytes)	256	256
Timers (8/16-bit)	2/1	2/1
Oscillator modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5 $\overline{\text{MCLR}}$	RA0/1/2/3/4/5 $\overline{\text{MCLR}}$
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator		2
CCP	ECCP	Y
Op Amps	N	2
PWM	N	Two-Phase
Ultra Low-Power Wake-up	Y	N
Extended WDT	Y	Y
Software Control Option of WDT/BOR	Y	Y
INTOSC Frequencies	32 kHz - 8 MHz	32 kHz - 8 MHz
Clock Switching	Y	Y

NOTES:

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X

NOTES:

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Application (optional):

Would you like a reply?____Y ____N

Device: PIC16F785/HV785   Literature Number: DS41249D

Questions:

1. What are the best features of this document?

____

____

2. How does this document meet your hardware and software development needs?

____

____

3. Do you find the organization of this document easy to follow? If not, why?

____

____

4. What additions to the document do you think would enhance the structure and subject?

____

____

5. What deletions from the document could be made without affecting the overall usefulness?

____

____

6. Is there any incorrect or misleading information (what and where)?

____

____

7. How would you improve this document?

____

____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device: PIC18F248/258(1), PIC18F448/458(1), PIC18F248/258T(2), PIC18F448/458T(2);
VDD range 4.2V to 5.5V
PIC18LF248/258(1), PIC18LF448/458(1), PIC18LF248/258T(2), PIC18LF448/458T(2);
VDD range 2.0V to 5.5V

Temperature Range:

I	=	-40°C to +85°C	(Industrial)
E	=	-40°C to +125°C	(Extended)

Package:

PT	=	TQFP (Thin Quad Flatpack)
L	=	PLCC
SO	=	SOIC
SP	=	Skinny Plastic DIP
P	=	PDIP

Pattern: QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a) PIC18LF258 - I/L 301 = Industrial temp., PLCC package, Extended VDD limits, QTP pattern #301.

b) PIC18LF458 - I/PT = Industrial temp., TQFP package, Extended VDD limits.

c) PIC18F258 - E/L = Extended temp., PLCC package, normal VDD limits.

Note 1: F = Standard Voltage Range
LF = Wide Voltage Range

2: T = in tape and reel PLCC, and TQFP packages only.

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