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## **NTE65101** **Integrated Circuit** **256 x 4–Bit Static Random Access Memory (SRAM)**

### **Description:**

The NTE65101 is a CMOS 1024–bit device organized in 256 words by 4 bits in a 22–Lead DIP type package. This device offers ultra low power and fully static operation with a single 5V supply. Separate data inputs and data outputs permit maximum flexibility in bus–oriented systems. Data retention at a power supply as low as 2V over temperature readily allows design into applications using battery backup for nonvolatility. The NTE65101 is fully static and does not require clocking in standby mode.

### **Features:**

- Organized as 256 Bytes of 4–Bits
- Static Operation
- Low Standby Power
- Three–State Output
- Single 5V Power Supply
- Data Retention to 2V
- TTL Compatible
- Maximum Access Time: 450ns

### **Absolute Maximum Ratings:** (Voltages referenced to $V_{SS}$ Pin8)

Supply Voltage, $V_{CC}$ .....	–0.5 to +7V
Input Voltage, $V_{in}$ .....	–0.3 to $V_{CC} + 0.3V$
Operating Temperature Range, $T_A$ .....	–40° to +85°C
Storage Temperature Range, $T_{stg}$ .....	–65° to +150°C

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

**DC Electrical Characteristics:** ( $V_{CC} = 5V \pm 5\%$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current	$I_{in}$	Note 3	–	5.0	–	nA
Input High Voltage	$V_{IH}$		2.2	–	$V_{CC}$	V
Input Low Voltage	$V_{IL}$		–0.3	–	0.65	V
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4	–	–	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$	–	–	0.4	V
Output Leakage Current	$I_{LO}$	$\overline{CE}1 = 2.2\text{V}$ , $V_{OL} = 0\text{V}$ to $V_{CC}$ , Note 3	–	–	$\pm 1.0$	$\mu\text{A}$
Operating Current	$I_{CC1}$	$V_{in} = V_{CC}$ , except $\overline{CE}1 \leq 0.65\text{V}$ , Outputs open	–	9.0	22	mA
	$I_{CC2}$	$V_{in} = 2.2\text{V}$ , except $\overline{CE}1 \leq 0.65\text{V}$ , Outputs open	–	13	27	mA
Standby Current	$I_{CCL}$	$CE2 \leq 0.2\text{V}$ , Note 3, Note 4	–	–	10	$\mu\text{A}$

Note 2. Typical values are  $T_A = +25^\circ\text{C}$  and nominal voltage.

Note 3. Current through all inputs and outputs included in  $I_{CCL}$  measurement.

Note 4. Low current state is for  $CE2 = 0$  only.

**Capacitance:**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	$C_{in}$	$V_{in} = 0\text{V}$	–	4.0	8.0	pF
Output Capacitance	$C_{out}$	$V_{out} = 0\text{V}$	–	8.0	12.0	pF

Note 2. Typical values are  $T_A = +25^\circ\text{C}$  and nominal voltage.

**Low  $V_{CC}$  Retention Characteristics:** ( $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$		2.0	–	–	V
Data Retention Current	$I_{CCDR1}$	$CE2 \leq 0.2\text{V}$ , $V_{DR} = 2\text{V}$	–	0.14	10	$\mu\text{A}$
Chip Deselect to Data Retention Time	$t_{CDR}$		0	–	–	ns
Operation Recovery Time	$t_R$	Note 5	$t_{RC}$	–	–	ns

Note 2. Typical values are  $T_A = +25^\circ\text{C}$  and nominal voltage.

Note 5.  $t_{RC}$  = Read Cycle Time.

**AC Operating Conditions and Characteristics:** (Full operating voltage and temperature unless otherwise specified)**AC Test Conditions:**

Condition	Value
Input Pulse Levels	+0.65V to 2.2V
Input Rise and Fall Times	20ns
Output Load –	1 TTL Gate and $C_L = 100\text{pF}$
Timing Measurement Reference Level	1.5V

**AC Operating Conditions and Characteristics (Cont'd):** (Full operating voltage and temperature unless otherwise specified)

**Read Cycle:**

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	$t_{RC}$	450	–	ns
Access Time	$t_A$	–	450	ns

**Read Cycle (Cont'd):**

Parameter	Symbol	Min	Max	Unit
Address Setup Time	$t_{AS}$	20	–	ns
Address Hold Time	$t_{AH}$	0	–	ns
Chip Enable ( $\overline{CE}1$ ) to Output	$t_{CO1}$	–	400	ns
Chip Enable (CE2) to Output	$t_{CO2}$	–	500	ns
Output Disable to Output	$t_{OD}$	–	250	ns
Data Output to High Z State	$t_{DF}$	0	130	ns
Previous Read Data Valid with Respect to Address Change	$t_{OH1}$	0	–	ns
Previous Read Data Valid with Respect to Chip Enable	$t_{OH2}$	0	–	ns

**Write Cycle:**

Parameter	Symbol	Min	Max	Unit
Write Cycle	$t_{WC}$	450	–	ns
Write Delay	$t_{AW}$	130	–	ns
Chip Enable ( $\overline{CE}1$ ) to Write	$t_{CW1}$	350	–	ns
Chip Enable (CE2) to Write	$t_{CW2}$	350	–	ns
Data Setup	$t_{DW}$	250	–	ns
Data Hold	$t_{DH}$	50	–	ns
Write Pulse	$t_{WP}$	250	–	ns
Write Recovery	$t_{WR}$	50	–	ns
Output Disable Setup	$t_{DS}$	130	–	ns

**Truth Table:**

$\overline{CE}1$	CE2	OD	R/W	D <sub>in</sub>	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disable
L	H	H	L	X	High Z	Write
L	H	L	L	X	D <sub>in</sub>	Write
L	H	L	H	X	D <sub>out</sub>	Read

### Pin Connection Diagram

