512K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time : 55 ns
- Low power consumption:
  Operatingcurrent : 30/20mA (TYP.)
  Standby current : 4 µA (TYP.) C-version
- Single 2.7V ~ 5.5V power supply
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product

- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- All products ROHS Compliant
- Package 32-pin 450 mil SOP
  32-pin 8mm x 20mm TSOP-I
  32-pin 600 mil P-DIP
  32-pin 8mm x 13.4mm sTSOP
  *36-ball 6mm x 8mm TFBGA
  *

Coming Soon!

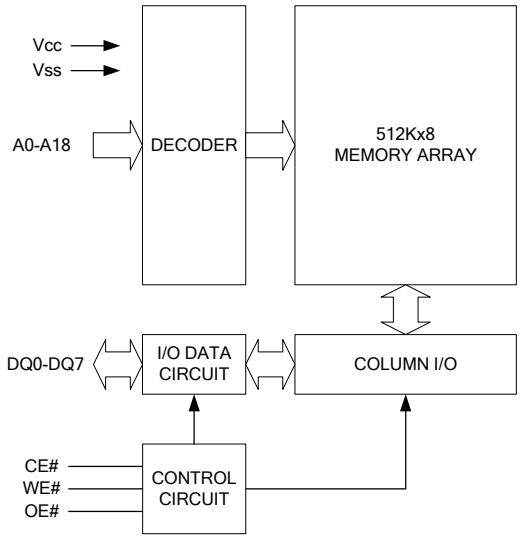
GENERAL DESCRIPTION

The AS6C4008 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C4008 is well designed for very low power system applications, and particularly well suited for battery back-up non-volatile memory application.

The AS6C4008 operates from a single power supply of 2.7V ~ 5.5V
.

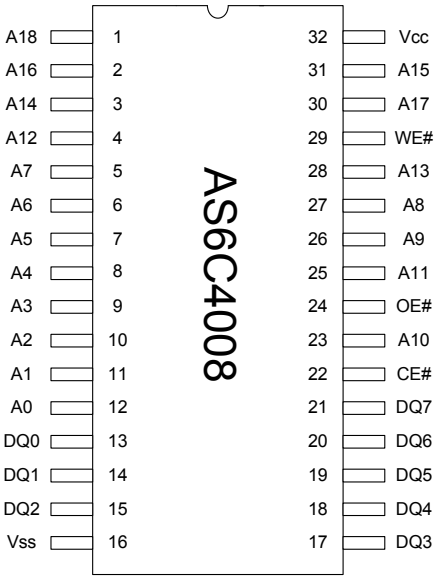
FUNCTIONAL BLOCK DIAGRAM



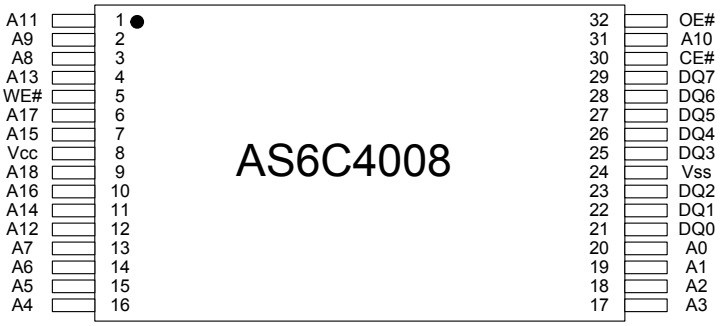
PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

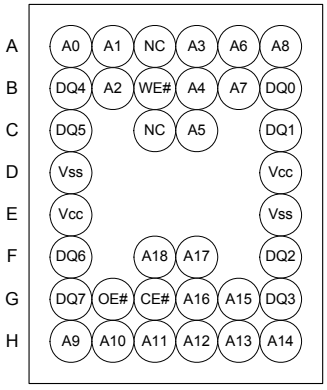
PIN CONFIGURATION



SOP/P-DIP



TSOP-I/sTSOP



TFBGA

512K X 8 BIT LOW POWER CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 6.5	V
Operating Temperature	T_A	0 to 70(C grade)	°C
		-40 to 85(I grade)	
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC},I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC},I_{CC1}
Write	L	X	L	D_{IN}	I_{CC},I_{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

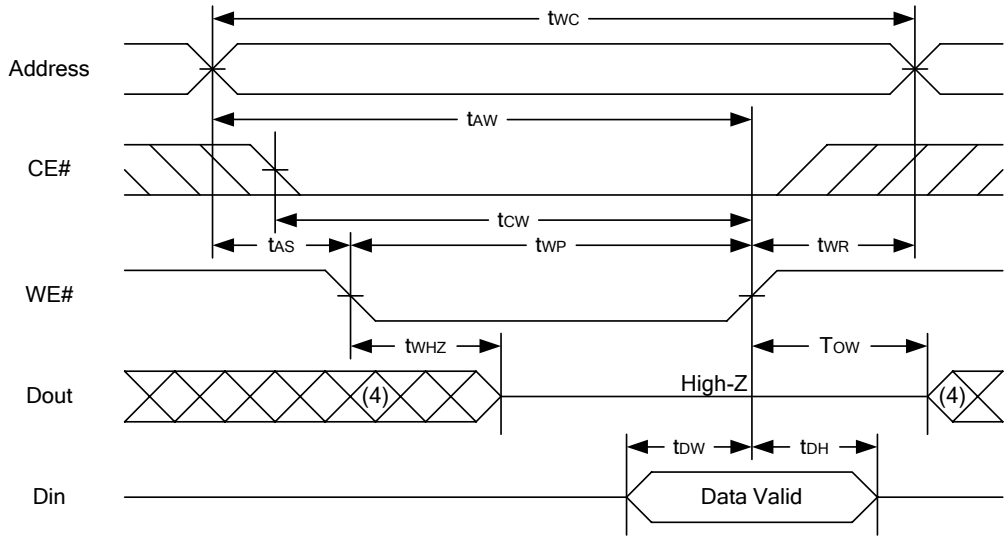
DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.*3	MAX.	UNIT
Supply Voltage	V_{CC}			2.7	3.0	5.5	V
Input High Voltage	V_{IH}*1			0.7* V_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}*1			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{CC} \geqq V_{IN} \geqq V_{SS}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{CC} \geqq V_{OUT} \geqq V_{SS}$, Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH} = -1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA		-	-	0.4	V
Average Operating Power supply Current	I_{CC}	Cycle time = Min. CE# = 0.2V, $I_{I/O}$ = 0mA other pins at 0.2V or V_{CC} - 0.2V	- 55	-	30	60	mA
	I_{CC1}	Cycle time = 1µs CE# = 0.2V, $I_{I/O}$ = 0mA other pins at 0.2V or V_{CC} - 0.2V		-	4	10	mA
Standby Power Supply Current	I_{SB1}	CE# $\geqq V_{CC}$ - 0.2V	*C	-	4	50*4	µA
			*I	-	4	50*4	µA

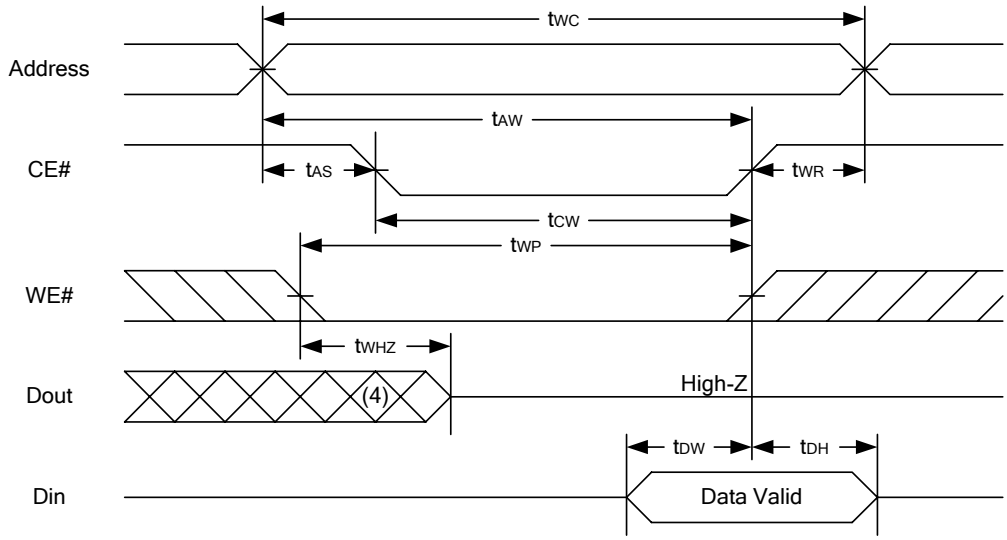
Notes: 1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
2. Over/Undershoot specifications are characterized, not 100% tested.
3. Typical values are included for reference only and are not guaranteed or tested. Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C
4. 25µA for special request

*C=Commercial temperature/I = Industrial temperature

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :
1.WE#, CE# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#.
3.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

Notes:
1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
   Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25?

CAPACITANCE (T_A = 25℃, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V_{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.			AS6C4008-55				UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}			55	-			ns
Address Access Time	t_{AA}			-	55			ns
Chip Enable Access Time	t_{ACE}			-	55			ns
Output Enable Access Time	t_{OE}			-	30			ns
Chip Enable to Output in Low-Z	t_{CLZ}*			10	-			ns
Output Enable to Output in Low-Z	t_{OLZ}*			5	-			ns
Chip Disable to Output in High-Z	t_{CHZ}*			-	20			ns
Output Disable to Output in High-Z	t_{OHZ}*			-	20			ns
Output Hold from Address Change	t_{OH}			10	-			ns

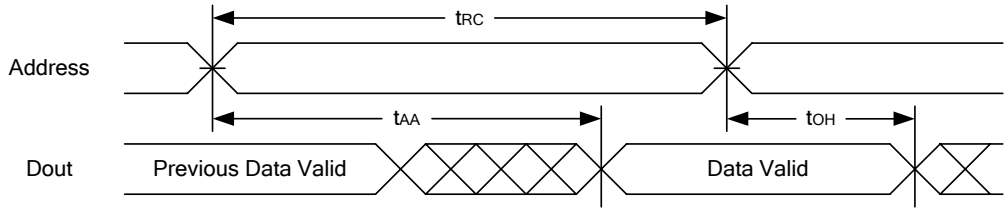
(2) WRITE CYCLE

PARAMETER	SYM.			AS6C4008-55				UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}			55	-			ns
Address Valid to End of Write	t_{AW}			50	-			ns
Chip Enable to End of Write	t_{CW}			50	-			ns
Address Set-up Time	t_{AS}			0	-			ns
Write Pulse Width	t_{WP}			45	-			ns
Write Recovery Time	t_{WR}			0	-			ns
Data to Write Time Overlap	t_{DW}			25	-			ns
Data Hold from End of Write Time	t_{DH}			0	-			ns
Output Active from End of Write	t_{OW}*			5	-			ns
Write to Output in High-Z	t_{WHZ}*			-	20			ns

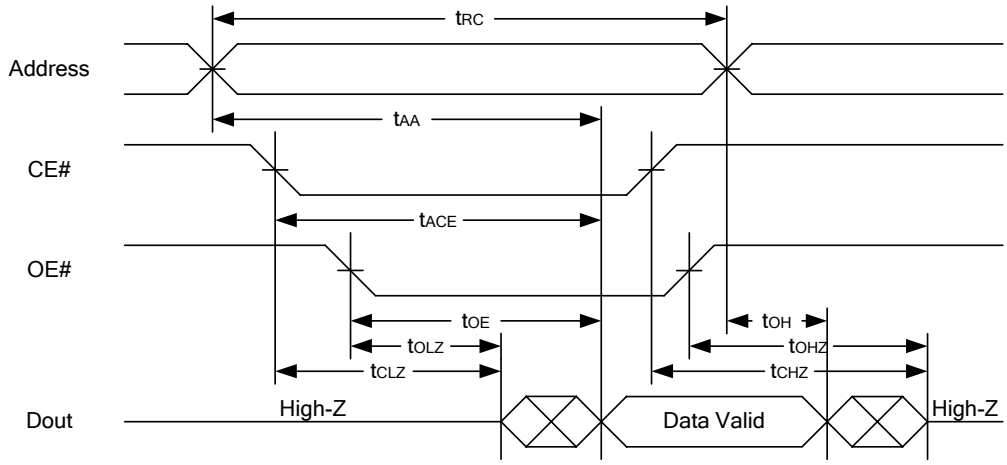
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)

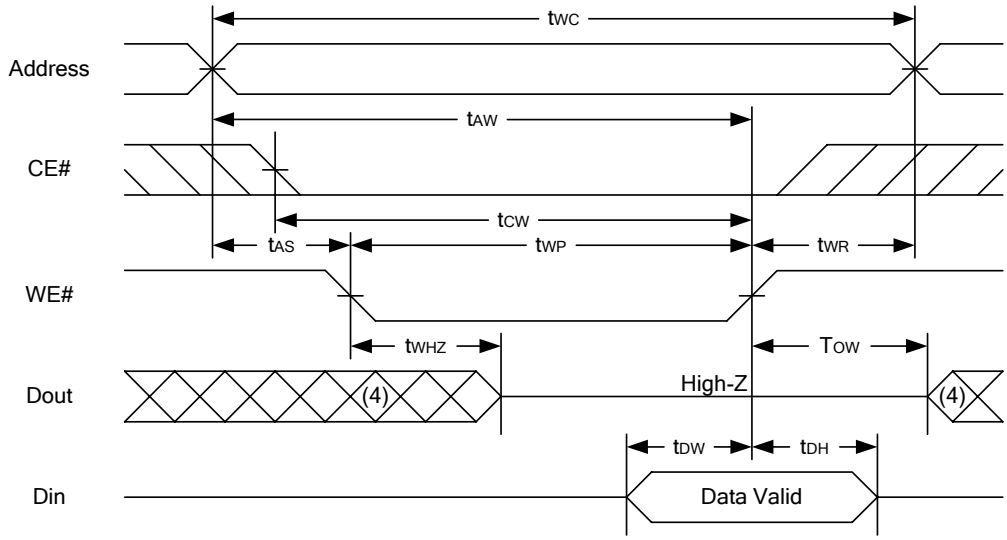


READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

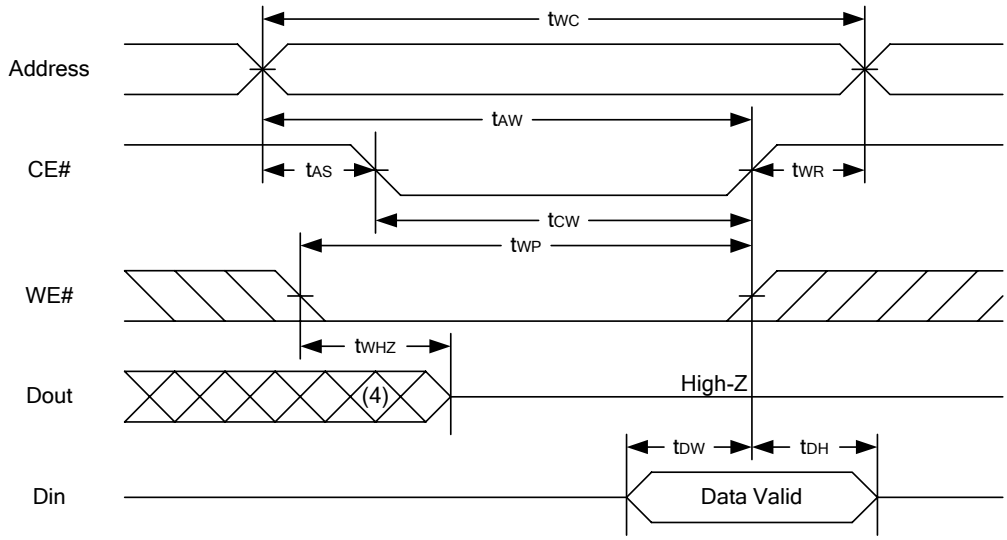


Notes :
1.WE# is high for read cycle.
2.Device is continuously selected OE# = low, CE# = low.
3.Address must be valid prior to or coincident with CE# = low.; otherwise t_{AA} is the limiting parameter.
4.t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



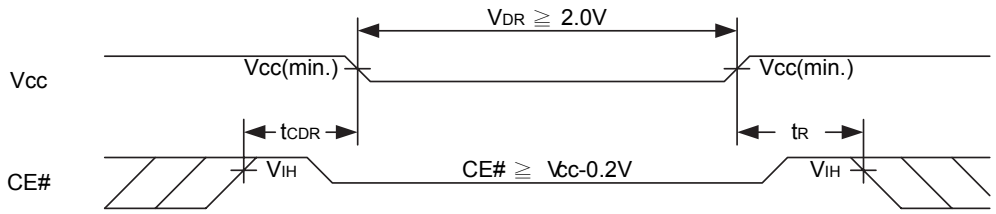
Notes :
1.WE#, CE# must be high during all address transitions.
2.A write occurs during the overlap of a low CE#, low WE#.
3.During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4.During this period, I/O pins are in the output state, and input signals must not be applied.
5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
V_{CC} for Data Retention	V_{DR}	CE# ≧ V_{CC} - 0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	V_{CC} = 2.0V	**C	-	2	30	µ
		CE# ≧ V_{CC} - 0.2V	**I	-	2	30	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

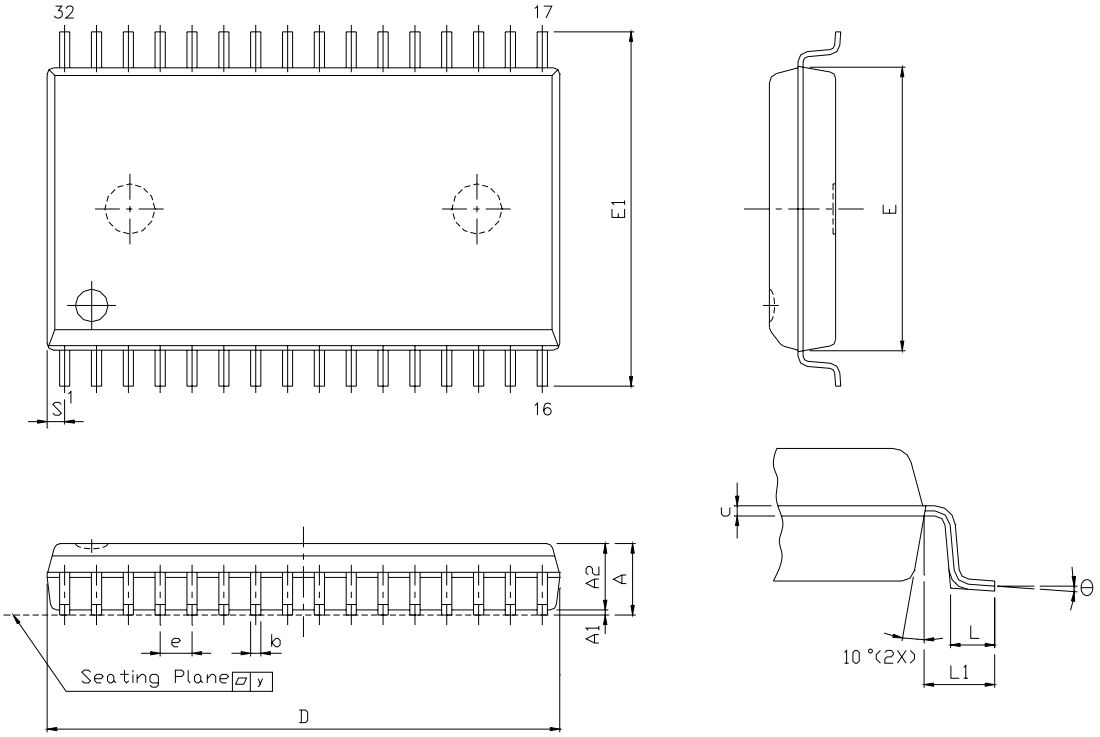
t_{RC*} = Read Cycle Time **C=Commercial temperature/I=Industrial temperature

DATA RETENTION WAVEFORM



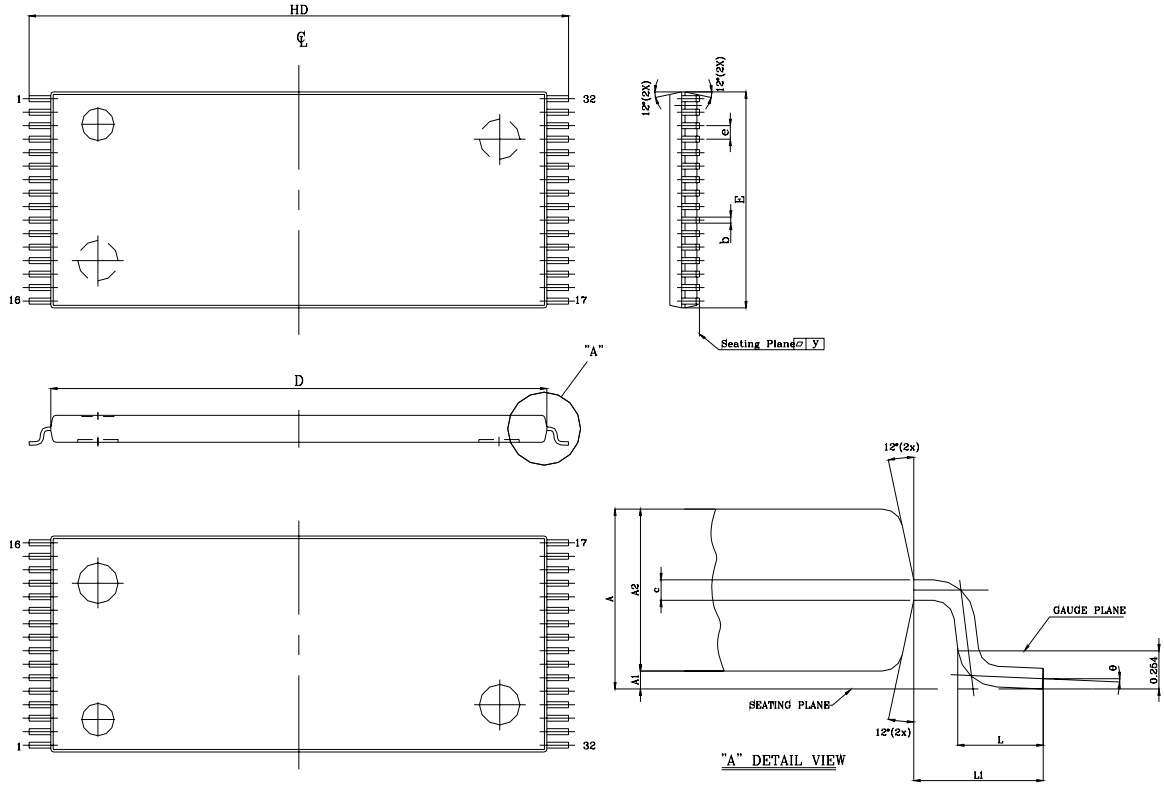
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension



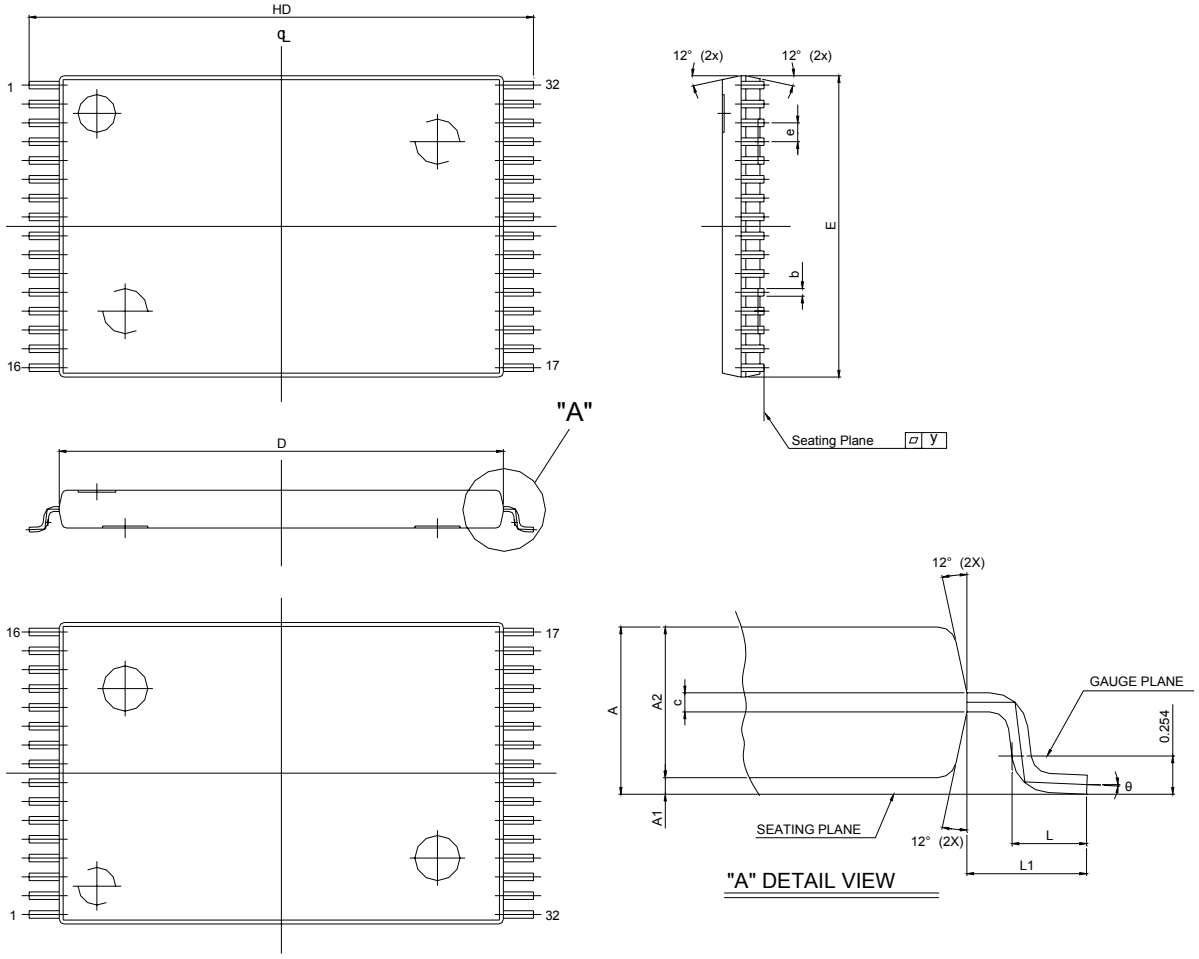
UNIT / SYM.	INCH.(BASE)	MM(REF)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445 ±0.005	11.303 ±0.127
E1	0.555 ±0.012	14.097 ±0.305
e	0.050(TYP)	1.270(TYP)
L	0.0347 ±0.008	0.881 ±0.203
L1	0.055 ±0.008	1.397 ±0.203
S	0.026(MAX)	0.660 (MAX)
y	0.004(MAX)	0.101(MAX)
Θ	0^o -10^o	0^o -10^o

32 pin 8mm x 20mm TSOP-I Package Outline Dimension



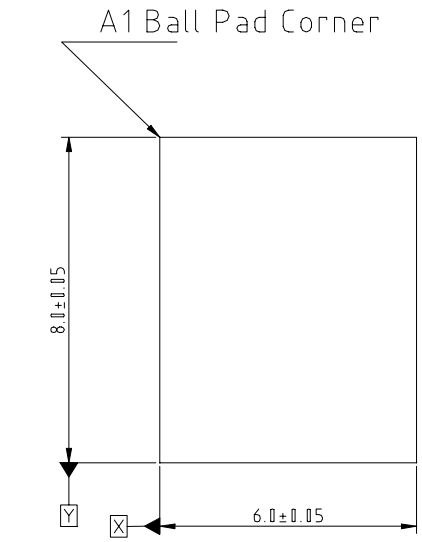
UNIT / SYM.	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0°～5°	0°～5°

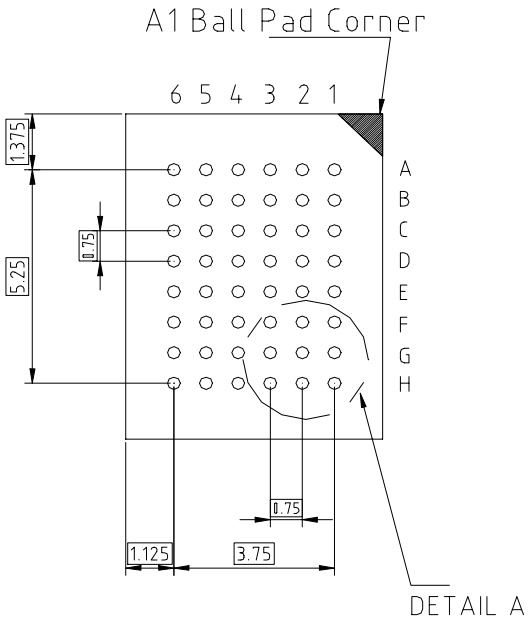
32 pin 8mm x 13.4mm sTSOP Package Outline Dimension

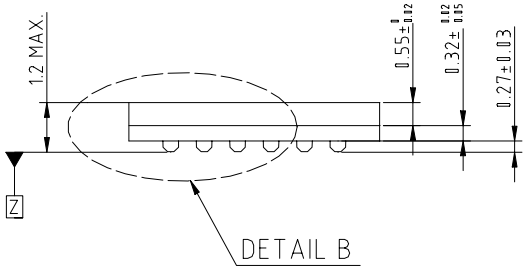


UNIT / SYM.	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ±0.002	0.130 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.01	0.20±0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ±0.004	11.80 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.528±0.008	13.40 ±0.20.
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.8 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0^o～5^o	0^o～5^o

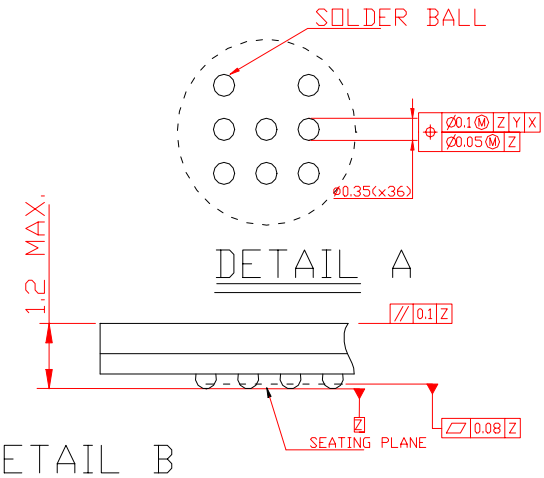
36 ball 6mm × 8mm TFBGA Package Outline Dimension





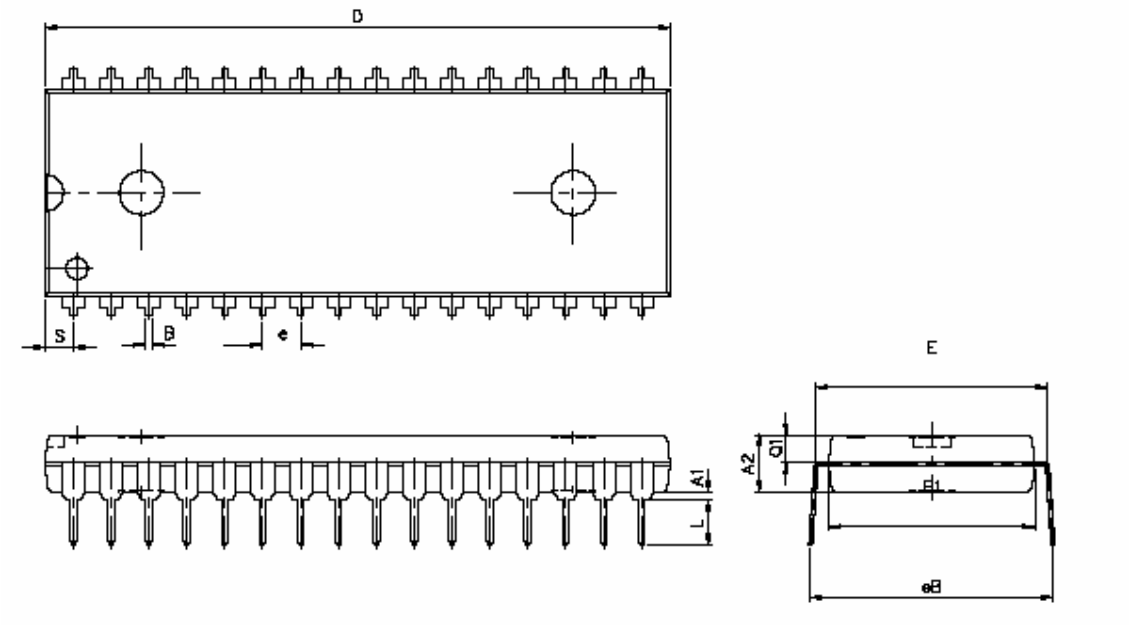


SIDE VIEW



DETAIL B

32 pin 600 mil P-DIP Package Outline Dimension



UNIT / SYM.	INCH(BASE)	MM(REF)
A1	0.001 (MIN)	0.254 (MIN)
A2	0.150 ± 0.005	3.810 ± 0.127
B	0.018 ± 0.005	0.457 ± 0.127
D	1.650 ± 0.005	41.910 ± 0.127
E	0.600 ± 0.010	15.240 ± 0.254
E1	0.544 ± 0.004	13.818 ± 0.102
e	0.100 (TYP)	2.540 (TYP)
eB	0.640 ± 0.020	16.256 ± 0.508.
L	0.130 ± 0.010	3.302 ± 0.254
S	0.075 ± 0.010	1.905 ± 0.254
Q1	0.070 ± 0.005	1.778 ± 0.127

Note : D/E1/S dimension do not include mold flash.

ORDERING INFORMATION

Ordering Codes

Alliance	Organization	VCC range	Package	Operating Temp	Speed ns
AS6C4008-55PCN	512k x 8	2.7-5.5V	32pin 600mil PDIP	Commercial ~ 0° C to 70° C	55
AS6C4008-55SIN	512k x 8	2.7-5.5V	32pin 450mil SOP	Industrial ~ -40°C to 85° C	55
AS6C4008-55TIN	512k x 8	2.7-5.5V	32pin TSOP-I (8 x 20 mm)	Industrial ~ -40°C to 85° C	55
AS6C4008-55STIN	512k x 8	2.7-5.5V	32pin sTSOP (8 x 13.4 mm)	Industrial ~ -40°C to 85° C	55
AS6C4008-55BIN	512k x 8	2.7-5.5V	36pin TFBGA (6mm x 8mm) *	Industrial ~ -40°C to 85° C	55
			*Coming Soon!		

Part numbering system

AS6C	4008	- 55	X	X	N
low power SRAM prefix	Device Number 40 = 4M 08 = by 8	Access Time	Package Options: P = 32 pin 600 mil P-DIP S = 32 pin 450 mil SOP T = 32 pin TSOP-I (8mm x 20 mm) ST = 32 pin sTSOP (8mm x 13.4 mm) B = 36 pin TFBGA (6mm x 8mm)*	Temperature Range: C = Commercial (0°C to +70° C) I = Industrial (-40° to +85° C)	N = Lead Free RoHS Compliant Part

* Coming Soon!

Alliance Memory, Inc.
1116 South Amphlett, #2,
San Mateo, CA 94402
Tel: 650-525-3737
Fax: 650-525-0449
www.alliancememory.com

Part Number: AS6C4008
Document Version: v. 1.1