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NTE6507
Integrated Circuit
NMOS, 8 Bit Microprocessor (MPU)
w/On–Chip Clock OSC

Description:

The NTE6507 integrated circuit is an 8 bit microprocessor in a 28–Lead DIP type package which provides a selection of addressable memory range, interrupt input options, and on–chip clock oscillators and drivers. This device is bus compatible with the MC6800 product offering and is aimed at high performance, low cost applications where single phase inputs or crystals provide the time base.

Features:

- Single 5V ±5% Power Supply
- N Channel, Silicon Gate, Depletion Load Technology
- 8 Bit Parallel Processing
- Decimal and Binary Arithmetic
- Thirteen Addressing Modes
- True Indexing Capability
- Programmable Stack Pointer
- Variable Length Stack
- Bi–Directional Data Bus
- Instruction Decoding and Control
- 8k Addressable Bytes of Memory
- “Ready” Input
- Direct Memory Access Capability
- Bus Compatible with MC6800
- On–Board Clock
- 1MHz Operating Frequency

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} . . . . . –0.3 to +7.0V
Input Voltage, V_{in} . . . . . –0.3 to +7.0V
Operating Temperature Range, T_A . . . . . 0 to +70°C
Storage Temperature Range, T_{stg} . . . . . –55° to +150°C

Note 1. This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

DC Characteristics: (V_{CC} = 5V ±5%, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input High Voltage Logic and $\varnothing_{o(in)}$	V_{IH}		+2.0	V_{CC}	V
Logic			V_{CC}–0.5	V_{CC}+0.25	V
Input Low Voltage Logic and $\varnothing_{o(in)}$	V_{IL}		–0.3	+0.8	V
Input Loading RDY	I_{IL}	V_{in} = 0V, V_{CC} = 5.25V	–10	–300	µA
Input Leakage Current Logic (Excluding RDY)	I_{in}	V_{in} = 0 to 5.25V, V_{CC} = 0	–	2.5	µA
$\varnothing_{o(in)}$			–	10.0	µA
Three–State (Off State) Input Current DB0–DB7	I_{TSI}	V_{in} = 0.4 to 2.4V, V_{CC} = 5.25V	–	±10	µA
Output High Voltage DB0–DB7, A0–A15, R/$\overline{W}$	V_{OH}	I_{LOAD} = –100µA, V_{CC} = 4.75V	2.4	–	V
Output Low Voltage DB0–DB7, A0–A15, R/$\overline{W}$	V_{OL}	I_{LOAD} = 1.6mA, V_{CC} = 4.75V	–	0.4	V
Power Dissipation	P_D	V_{CC} = 5.25V	–	700	mW
Capaticance $\overline{RES}$, RDY,	C_{in}	V_{in} = 0, T_A = +25°C, f = 1MHz	–	10	pF
DB0–DB7			–	15	pF
A0–A15, R/$\overline{W}$	C_{out}		–	12	pF
$\varnothing_{o(in)}$	$C_{\varnothing_{o(in)}}$		–	15	pF

Dynamic Operating Characteristics: (V_{CC} = 5V ±5%, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Cycle Time	T_{CYC}		1.00	40	µs
$\varnothing_{o(in)}$ Low Time	$T_{L\varnothing o}$	Note 2	480	–	ns
$\varnothing_{o(in)}$ High Time	$T_{H\varnothing o}$	Note 2	460	–	ns
$\varnothing_o$ Neg to $\varnothing_1$ Pos Delay	T_{01+}	Load = 100pF	10	70	ns
$\varnothing_o$ Neg to $\varnothing_2$ Neg Delay	T_{02-}	Load = 100pF	5	65	ns
$\varnothing_o$ Pos to $\varnothing_1$ Neg Delay	T_{01-}	Load = 100pF	5	65	ns
$\varnothing_o$ Pos to $\varnothing_2$ Pos Delay	T_{02+}	Load = 100pF	15	75	ns
$\varnothing_{\alpha(in)}$ Rise and Fall Time	T_{RO}, T_{FO}	Note 3	0	30	ns
$\varnothing_{1(OUT)}$ Pulse Width	$T_{PWH\phi_1}$		$T_{L\phi_o}$–20	$T_{L\phi_o}$	ns
$\varnothing_{2(OUT)}$ Pulse Width	$T_{PWH\phi_2}$		$T_{L\phi_o}$–40	$T_{L\phi_o}$–10	ns
Delay Between $\varnothing_1$ and $\varnothing_2$	T_D		5	–	ns
$\varnothing_1$ and $\varnothing_2$ Rise and Fall Times	T_R, T_F	Load = 1TTL load +30pF, Note 3	–	25	ns

Note 2. Measured at 50% points.

Note 3. Measured between 10% and 90% points.

Dynamic Operating Characteristics (Cont'd): (V_{CC} = 5V ±5%, T_A = 0 to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
R/$\overline{W}$ Setup Time	T_{RWS}		–	225	ns
R/$\overline{W}$ Hold Time	T_{RWH}		30	–	ns
Address Setup Time	T_{ADS}		–	225	ns
Address Hold Time	T_{ADH}		30	–	ns
Read Access Time	T_{ACC}		–	650	ns
Read Data Setup Time	T_{DSU}		100	–	ns
Read Data Hold Time	T_{HR}		10	–	ns
Write Data Setup Time	T_{MDS}		20	175	ns
Write Data Hold Time	T_{HW}		60	150	ns
Sync Setup Time	T_{SYS}		–	350	ns
Sync Hold Time	T_{SYH}		30	–	ns
RDY Setup Time	T_{RS}	Note 4	200	–	ns

Note 4. RDY must never switch states within T_{RS} to end of $\varnothing_2$.

Pin Connection Diagram