



■ Pin Configurations

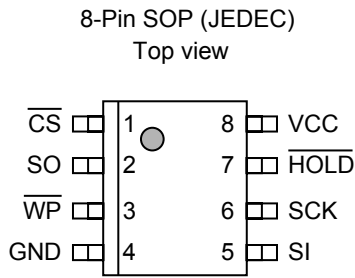


Figure 1

S-25C080A0I-J8T1G

Table 1

Pin No.	Symbol	Description
1	$\overline{CS}^{*1}$	Chip select input
2	SO	Serial data output
3	$\overline{WP}^{*1}$	Write protect input
4	GND	Ground
5	SI <sup>*1</sup>	Serial data input
6	SCK <sup>*1</sup>	Serial clock input
7	$\overline{HOLD}^{*1}$	Hold input
8	VCC	Power supply

\*1. All input pins have the CMOS structure. Do not set the input pins in high impedance during operation.

**Remark** See Dimensions for details of the package drawings.

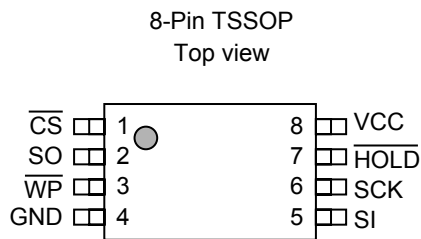


Figure 2

S-25C080A0I-T8T1G

Table 2

Pin No.	Symbol	Description
1	$\overline{CS}^{*1}$	Chip select input
2	SO	Serial data output
3	$\overline{WP}^{*1}$	Write protect input
4	GND	Ground
5	SI <sup>*1</sup>	Serial data input
6	SCK <sup>*1</sup>	Serial clock input
7	$\overline{HOLD}^{*1}$	Hold input
8	VCC	Power supply

\*1. All input pins have the CMOS structure. Do not set the input pins in high impedance during operation.

**Remark** See Dimensions for details of the package drawings.

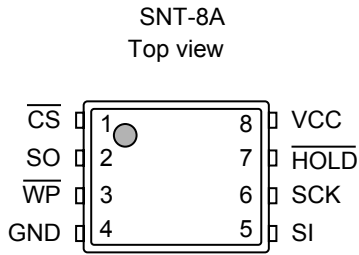


Figure 3

S-25C080A0I-I8T1G

Table 3

Pin No.	Symbol	Description
1	$\overline{CS}^{*1}$	Chip select input
2	SO	Serial data output
3	$\overline{WP}^{*1}$	Write protect input
4	GND	Ground
5	SI <sup>*1</sup>	Serial data input
6	SCK <sup>*1</sup>	Serial clock input
7	$\overline{HOLD}^{*1}$	Hold input
8	VCC	Power supply

\*1. All input pins have the CMOS structure. Do not set the input pins in high impedance during operation.

**Remark** See Dimensions for details of the package drawings.

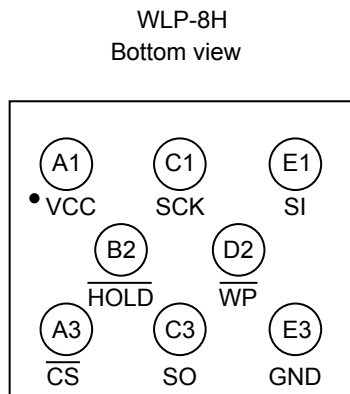


Figure 4

S-25C080A0I-H8T3

Table 4

Pin No.	Symbol	Description
A1	VCC	Power supply
A3	$\overline{CS}^{*1}$	Chip select input
B2	$\overline{HOLD}^{*1}$	Hold input
C1	SCK <sup>*1</sup>	Serial clock input
C3	SO	Serial data output
D2	$\overline{WP}^{*1}$	Write protect input
E1	SI <sup>*1</sup>	Serial data input
E3	GND	Ground

\*1. All input pins have the CMOS structure. Do not set the input pins in high impedance during operation.

**Remark** See Dimensions for details of the package drawings.

■ Block Diagram

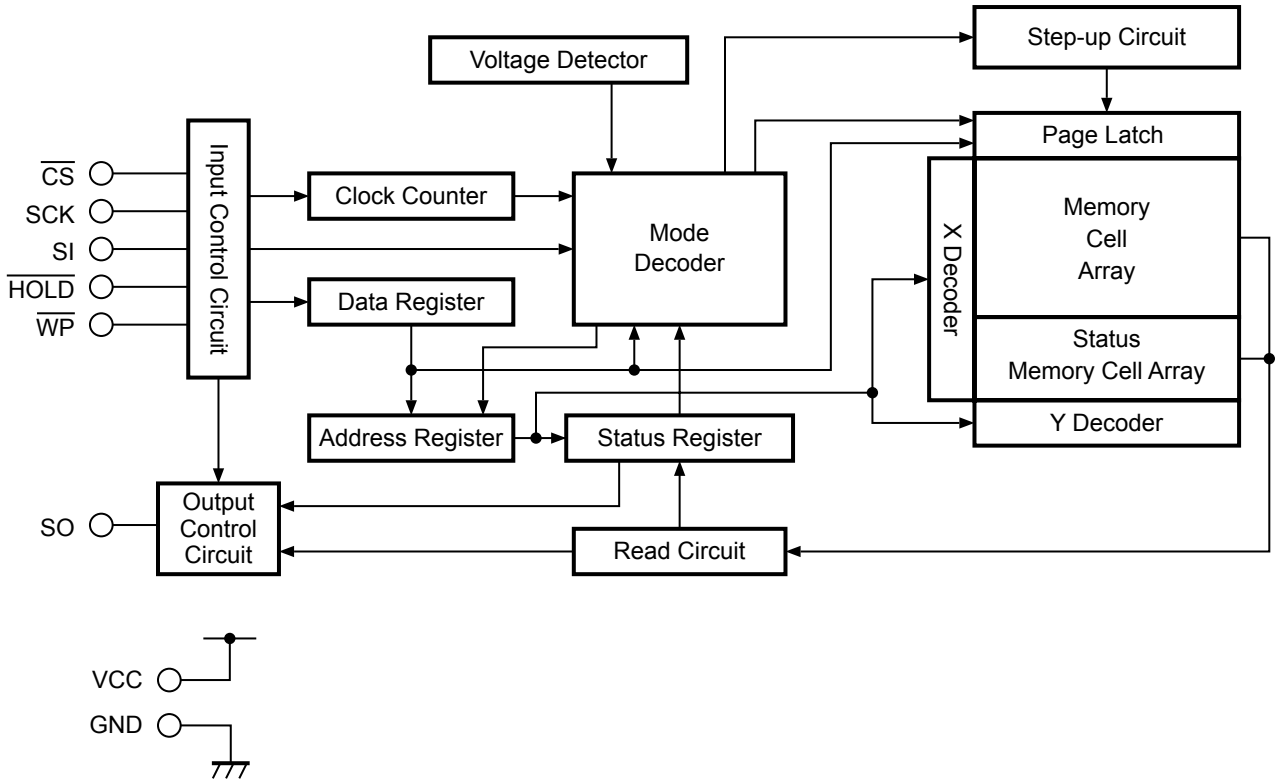


Figure 5

## ■ Absolute Maximum Ratings

Table 5

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.3 to +7.0	V
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Operation ambient temperature	T <sub>opr</sub>	-40 to +85	°C
Storage temperature	T <sub>sta</sub>	-65 to +150	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Recommended Operating Conditions

Table 6

Item	Symbol	Condition	Min.	Max.	Unit
Power supply voltage	V <sub>CC</sub>	Read Operation	1.6	5.5	V
		Write Operation	1.7	5.5	V
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 1.6 to 5.5 V	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 1.0	V
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 1.6 to 5.5 V	-0.3	0.3 × V <sub>CC</sub>	V

## ■ Pin Capacitance

Table 7

(Ta = 25 °C, f = 1.0 MHz, V<sub>CC</sub> = 5 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V (CS, SCK, SI, WP, HOLD)	–	8	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V (SO)	–	10	pF

## ■ Endurance

Table 8

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N <sub>W</sub>	+25°C	10 <sup>6</sup>	–	cycles / word <sup>*1</sup>

\*1. For each address (Word: 8 bits)

## ■ Data Retention

Table 9

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	–	+25°C	100	–	year

■ DC Electrical Characteristics

Table 10

Item	Symbol	Condition	V <sub>CC</sub> = 1.6 to 2.5 V f <sub>SCK</sub> = 2.0 MHz		V <sub>CC</sub> = 2.5 to 4.5 V f <sub>SCK</sub> = 5.0 MHz		V <sub>CC</sub> = 4.5 to 5.5 V f <sub>SCK</sub> = 5.0 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I <sub>CC1</sub>	No load at SO pin	–	1.5	–	2.0	–	2.5	mA

Table 11

Item	Symbol	Condition	V <sub>CC</sub> = 1.7 to 2.5 V f <sub>SCK</sub> = 2.0 MHz		V <sub>CC</sub> = 2.5 to 4.5 V f <sub>SCK</sub> = 5.0 MHz		V <sub>CC</sub> = 4.5 to 5.5 V f <sub>SCK</sub> = 5.0 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I <sub>CC2</sub>	No load at SO pin	–	2.0	–	2.5	–	3.0	mA

Table 12

Item	Symbol	Condition	V <sub>CC</sub> = 1.6 to 2.5 V		V <sub>CC</sub> = 2.5 to 4.5 V		V <sub>CC</sub> = 4.5 to 5.5 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I <sub>SB</sub>	$\overline{CS} = V_{CC}$ , SO = Open Other inputs are V <sub>CC</sub> or GND	–	1.5	–	1.5	–	1.5	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	–	1.0	–	1.0	–	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> = GND to V <sub>CC</sub>	–	1.0	–	1.0	–	1.0	μA
Low level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 2.0 mA	–	–	–	0.4	–	0.4	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 1.5 mA	–	0.4	–	0.4	–	0.4	V
High level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = –2.0 mA	–	–	0.8 × V <sub>CC</sub>	–	0.8 × V <sub>CC</sub>	–	V
	V <sub>OL2</sub>	I <sub>OH</sub> = –0.4 mA	0.8 × V <sub>CC</sub>	–	0.8 × V <sub>CC</sub>	–	0.8 × V <sub>CC</sub>	–	V

## ■ AC Electrical Characteristics

**Table 13 Measurement Conditions**

Input pulse voltage	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100 pF

**Table 14**

Item	Symbol	$V_{CC} = 1.6$ to $2.5$ V		$V_{CC} = 2.5$ to $4.5$ V		$V_{CC} = 4.5$ to $5.5$ V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	$f_{SCK}$	–	2.0	–	5.0	–	5.0	MHz
CS setup time during CS falling	$t_{CSS,CL}$	150	–	90	–	90	–	ns
CS setup time during CS rising	$t_{CSS,CH}$	150	–	90	–	90	–	ns
CS deselect time	$t_{CDS}$	200	–	90	–	90	–	ns
CS hold time during CS falling	$t_{CSH,CL}$	200	–	90	–	90	–	ns
CS hold time during CS rising	$t_{CSH,CH}$	150	–	90	–	90	–	ns
SCK clock time “H” *1	$t_{HIGH}$	200	–	90	–	90	–	ns
SCK clock time “L” *1	$t_{LOW}$	200	–	90	–	90	–	ns
Rising time of SCK clock *2	$t_{RSK}$	–	1	–	1	–	1	μs
Falling time of SCK clock *2	$t_{FSK}$	–	1	–	1	–	1	μs
SI data input setup time	$t_{DS}$	50	–	20	–	20	–	ns
SI data input hold time	$t_{DH}$	60	–	30	–	30	–	ns
SCK “L” hold time during HOLD rising	$t_{SKH,HH}$	150	–	70	–	70	–	ns
SCK “L” hold time during HOLD falling	$t_{SKH,HL}$	100	–	40	–	40	–	ns
SCK “H” setup time during HOLD falling	$t_{SKS,HL}$	150	–	60	–	60	–	ns
SCK “H” setup time during HOLD rising	$t_{SKS,HH}$	150	–	60	–	60	–	ns
Disable time of SO output *2	$t_{OZ}$	–	200	–	100	–	100	ns
Delay time of SO output	$t_{OD}$	–	150	–	70	–	70	ns
Hold time of SO output	$t_{OH}$	0	–	0	–	0	–	ns
Rising time of SO output *2	$t_{RO}$	–	100	–	40	–	40	ns
Falling time of SO output *2	$t_{FO}$	–	100	–	40	–	40	ns
Disable time of SO output during HOLD falling *2	$t_{OZ,HL}$	–	200	–	100	–	100	ns
Delay time of SO output during HOLD rising *2	$t_{OD,HH}$	–	150	–	50	–	50	ns
WP setup time	$t_{WS1}$	0	–	0	–	0	–	ns
WP hold time	$t_{WH1}$	0	–	0	–	0	–	ns
WP release / setup time	$t_{WS2}$	0	–	0	–	0	–	ns
WP release / hold time	$t_{WH2}$	60	–	30	–	30	–	ns

\*1. The clock cycle of the SCK clock (frequency  $f_{SCK}$ ) is  $1/f_{SCK}$  μs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as  $(1/f_{SCK}) = t_{LOW} (\text{Min.}) + t_{HIGH} (\text{Min.})$  by minimizing the SCK clock cycle time.

\*2. These are values of sample and not 100% tested.





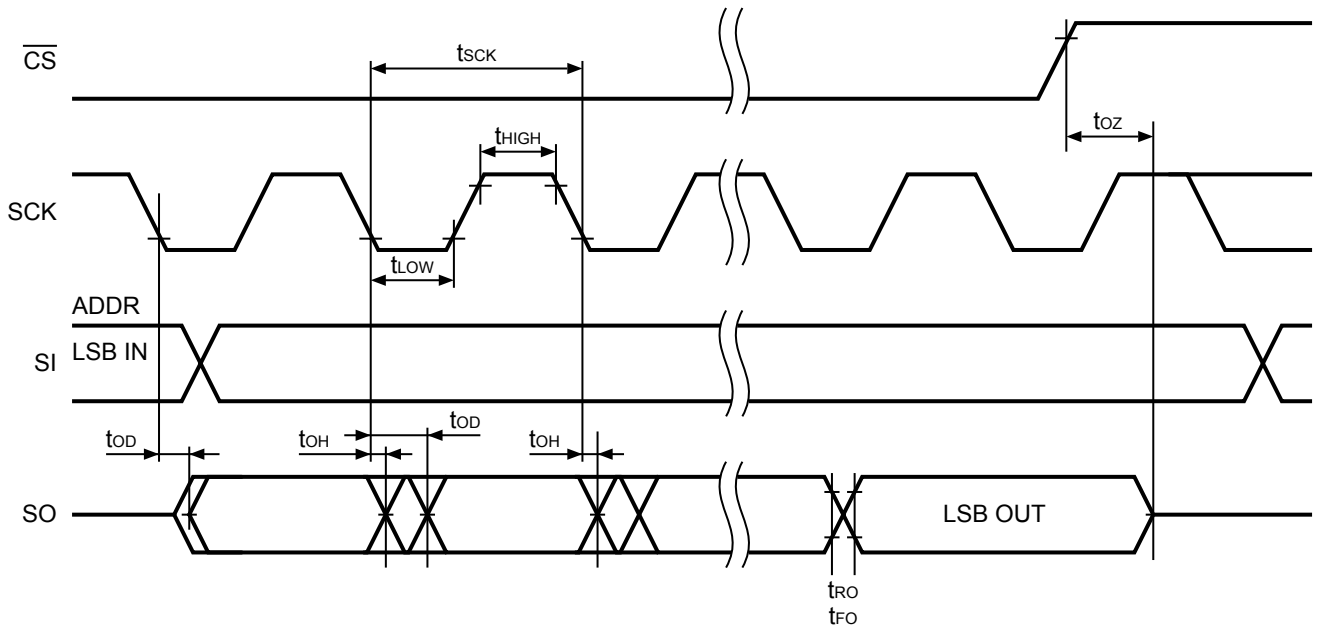


Figure 8 Serial output timing

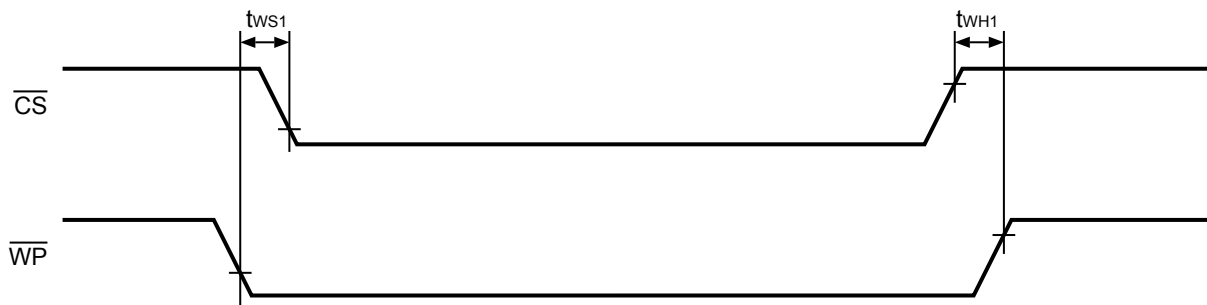


Figure 9 Valid timing in Write protect

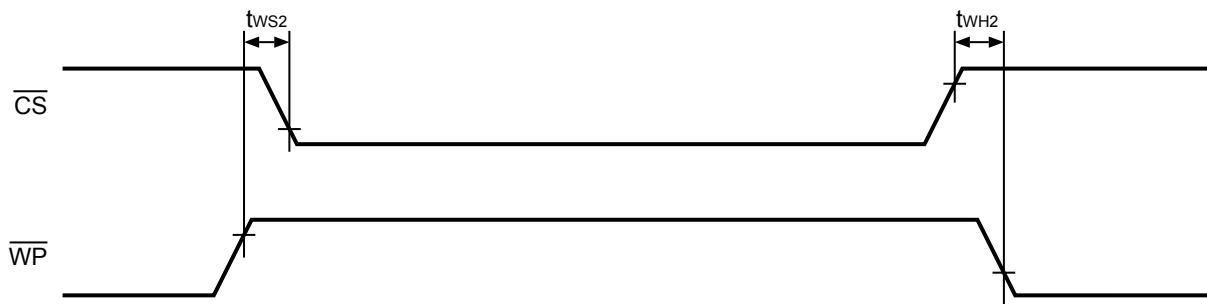


Figure 10 Invalid timing in Write protect

## ■ Pin Functions

### 1. $\overline{\text{CS}}$ (Chip select input) Pin

This is an input pin to set a chip in the select status. In the “H” input level, the device is in the non-select status and its output is high impedance. The device is in standby as long as it is not in Write inside. The device goes in active by setting the chip select to “L”. Input any instruction code after power-on and a falling of chip select.

### 2. SI (Serial data input) pin

This pin is to input serial data. This pin receives an instruction code, an address and Write data. This pin latches data at rising edge of serial clock.

### 3. SO (Serial data output) pin

This pin is to output serial data. The data output changes according to falling edge of serial clock.

### 4. SCK (Serial clock input) pin

This is a clock input pin to set the timing of serial data. An instruction code, an address and Write data are received at a rising edge of clock. Data is output during falling edge of clock.

### 5. $\overline{\text{WP}}$ (Write protect input) pin

Write protect is purposed to protect the area size against the Write instruction (BP1, BP0 in the status register). Fix this pin “H” or “L” not to set it in the floating state.

Refer to “■ Protect Operation” for details.

### 6. $\overline{\text{HOLD}}$ (HOLD input) pin

This pin is used to pause serial communications without setting the device in the non-select status.

In the hold status, the serial output goes in high impedance, the serial input and the serial clock go in “Don’t care”.

During the hold operation, be sure to set the device in active by setting the chip select ( $\overline{\text{CS}}$  pin) to “L”.

Refer to “■ Hold Operation” for details.

## ■ Instruction Setting

**Table 16** is the list of instruction for the S-25C080A. The instruction is able to be input by changing the  $\overline{CS}$  pin "H" to "L". Input the instruction in the MSB first. Each instruction code is organized with 1-byte as shown below. If the S-25C080A receives any invalid instruction code, the device goes in the non-select status.

**Table 16**

Instruction	Operation	Instruction code	Address		Data
		SCK input clock 1 to 8	SCK input clock 9 to 16	SCK input clock 17 to 24	SCK input clock 25 to 32
WREN	Write enable	0000 0110	–	–	–
WRDI	Write disable	0000 0100	–	–	–
RDSR	Read the status register	0000 0101	b7 to b0 output *1	–	–
WRSR	Write in the status register	0000 0001	b7 to b0 input	–	–
READ	Read memory data	0000 0011	A15 to A8 *2	A7 to A0	D7 to D0 output *3
WRITE	Write memory data	0000 0010	A15 to A8 *2	A7 to A0	D7 to D0 input

\*1. Sequential data reading is possible.

\*2. The higher addresses A15 to A10 = Don't care.

\*3. After outputting data in the specified address, data in the following address is output.

## ■ Operation

### 1. Status register

The status register's organization is below. The status register can Write and Read by a specific instruction.

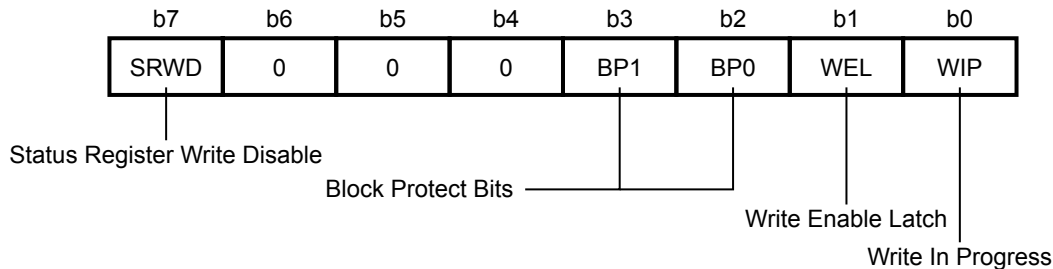


Figure 11 Organization of status register

The status / control bits of the status register as follows.

#### 1. 1 SRWD (b7) : Status Register Write Disable

Bit SRWD operates in conjunction with the Write protect signal ( $\overline{WP}$ ). With a combination of bit SRWD and signal  $\overline{WP}$  (SRWD = "1",  $\overline{WP}$  = "L"), this device goes in Hardware Protect status. In this case, the bits composed of the nonvolatile bit in the status register (SRWD, BP1, BP0) go in Read Only, so that the WRSR instruction is not performed.

#### 1. 2 BP1, BP0 (b3, b2) : Block Protect

Bit BP1 and BP0 are composed of the nonvolatile bit. The area size of Software Protect against WRITE instruction is defined by them. Rewriting these bits is possible by the WRSR instruction. To protect the memory area against the WRITE instruction, set either or both of bit BP1 and BP0 to "1". Rewriting bit BP1 and BP0 is possible unless they are in Hardware Protect mode. Refer to "■ Protect Operation" for details of "Block Protect".

#### 1. 3 WEL (b1) : Write Enable Latch

Bit WEL shows the status of internal Write Enable Latch. Bit WEL is set by the WREN instruction only. If bit WEL is "1", this is the status that Write Enable Latch is set. If bit WEL is "0", Write Enable Latch is in reset, so that the device does not receive the WRITE or WRSR instruction. Bit WEL is reset after these operations;

- the power supply voltage is dropping
- power-on
- after performing WRDI
- after the Write operation by the WRSR instruction has completed
- after the Write operation by the WRITE instruction has completed

#### 1. 4 WIP (b0) : Write In Progress

Bit WIP is Read Only and shows whether the internal memory is in the Write operation or not by the WRITE or WRSR instruction. Bit WIP is "1" during the Write operation but "0" during any other status.

**2. Write enable (WREN)**

Before writing data (WRITE and WRSR), be sure to set bit Write Enable Latch (WEL). This instruction is to set bit WEL. Its operation is below.

After selecting the device by the chip select ( $\overline{CS}$ ), input the instruction code from serial data input (SI). To set bit WEL, set the device in the non-select status by  $\overline{CS}$  at the 8th clock of the serial clock (SCK). To cancel the WREN instruction, input the clock different from a specified value (n = 8 clock) while  $\overline{CS}$  is in "L".

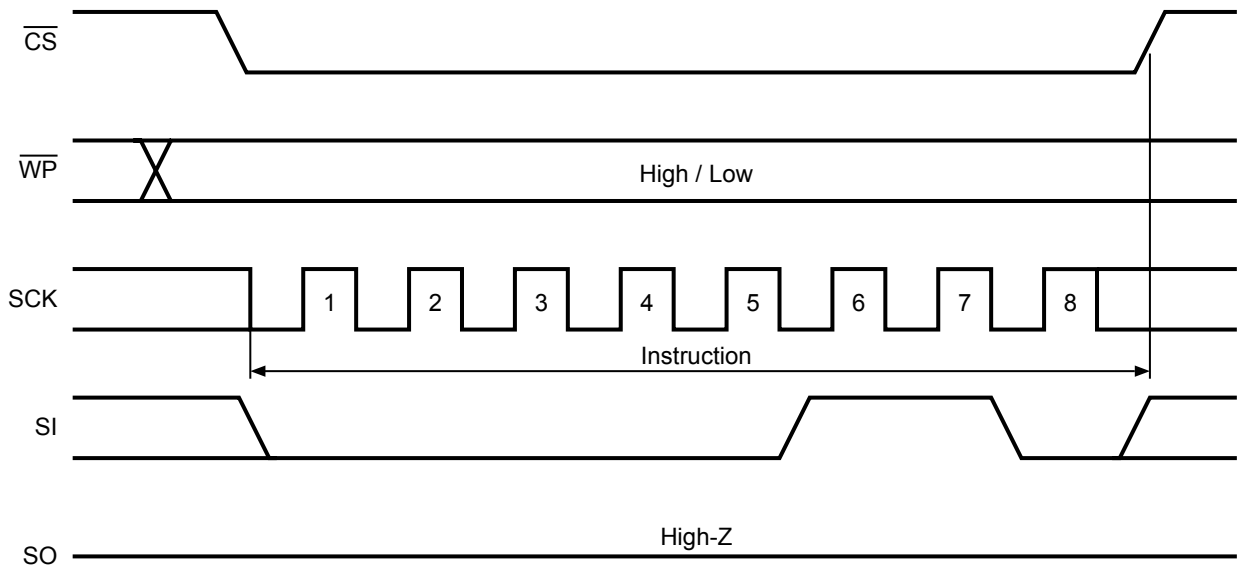


Figure 12 WREN operation

### 3. Write disable (WRDI)

The WRDI instruction is one of ways to reset bit Write Enable Latch (WEL). After selecting the device by the chip select ( $\overline{\text{CS}}$ ), input the instruction code from serial data input (SI).

To reset bit WEL, set the device in the non-select status by  $\overline{\text{CS}}$  at the 8th clock of the serial clock.

To cancel the WRDI instruction, input the clock different from a specified value ( $n = 8$  clock) while  $\overline{\text{CS}}$  is in "L". Bit WEL is reset after the operations shown below.

- The power supply voltage is dropping and power-on
- After performing WRDI
- After the completion of Write operation by the WRSR instruction
- After the completion of Write operation by the WRITE instruction

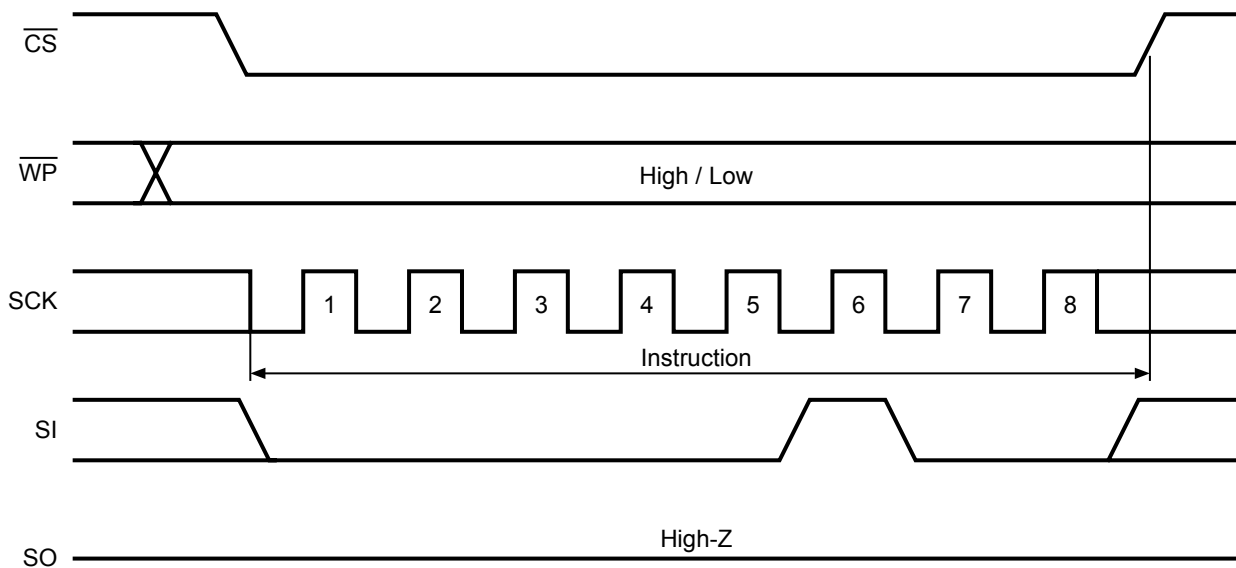


Figure 13 WRDI operation

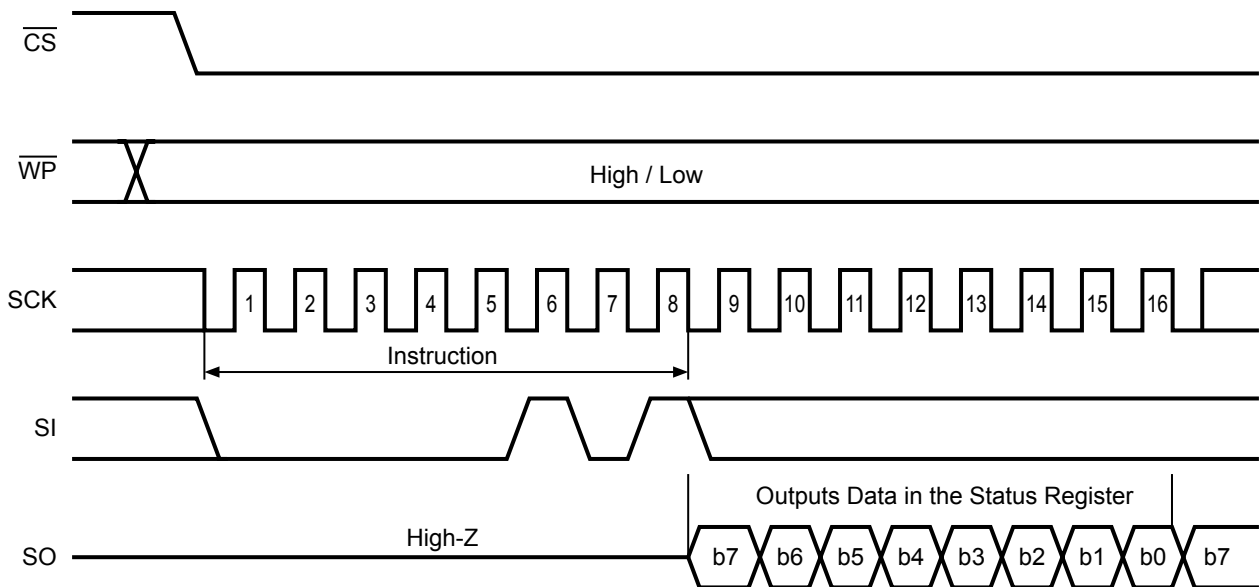
**4. Read the status register (RDSR)**

Reading data in the status register is possible by the RDSR instruction. During the Write operation, it is possible to confirm the progress by checking bit WIP.

Set the chip select ( $\overline{CS}$ ) "L" first. After that, input the instruction code from serial data input (SI). The status of bit in the status register is output from serial data output (SO). Sequential Read is available for the status register. To stop the Read cycle, set  $\overline{CS}$  to "H".

It is possible to read the status register always. The bits in it are valid and can be read by RDSR even in the Write cycle.

However, during the Write cycle in progress, the nonvolatile bits SRWD, BP1, BP0 are fixed in a certain value. These updated values of bit can be obtained by inputting another new RDSR instruction after the Write cycle has completed. Contrarily, two of Read Only bits WEL and WIP are being updated while the Write cycle is in progress.



**Figure 14 RDSR operation**

### 5. Write in the status register (WRSR)

The values of status register (SRWD, BP1, BP0) can be rewritten by inputting the WRSR instruction. But b6, b5, b4, b1, b0 of status register cannot be rewritten. b6 to 4 are always data "0" when reading the status register.

Before inputting the WRSR instruction, set bit WEL by the WREN instruction. The operation of WRSR is shown below.

Set the chip select ( $\overline{CS}$ ) "L" first. After that, input the instruction code and data from serial data input (SI). To start WRSR Write ( $t_{PR}$ ), set the chip select ( $\overline{CS}$ ) to "H" after inputting data or before inputting a rising of the next serial clock. It is possible to confirm the operation status by reading the value of bit WIP during WRSR Write. Bit WIP is "1" during Write, "0" during any other status. Bit WEL is reset when Write is completed.

With the WRSR instruction, the values of BP1 and BP0; which determine the area size the users can handle as the Read Only memory; can be changed. Besides bit SRWD can be set or reset by the WRSR instruction depending on the status of Write protect  $\overline{WP}$ . With a combination of bit SRWD and Write protect  $\overline{WP}$ , the device can be set in Hardware Protect mode (HPM). In this case, the WRSR instruction is not be performed (Refer to "■ Protect Operation").

Bit SRWD and BP1, BP0 keep the value which is the one prior to the WRSR instruction during the WRSR instruction. The newly updated value is changed when the WRSR instruction has completed.

To cancel the WRSR instruction, input the clock different from a specified value ( $n = 16$  clock) while  $\overline{CS}$  is in "L".

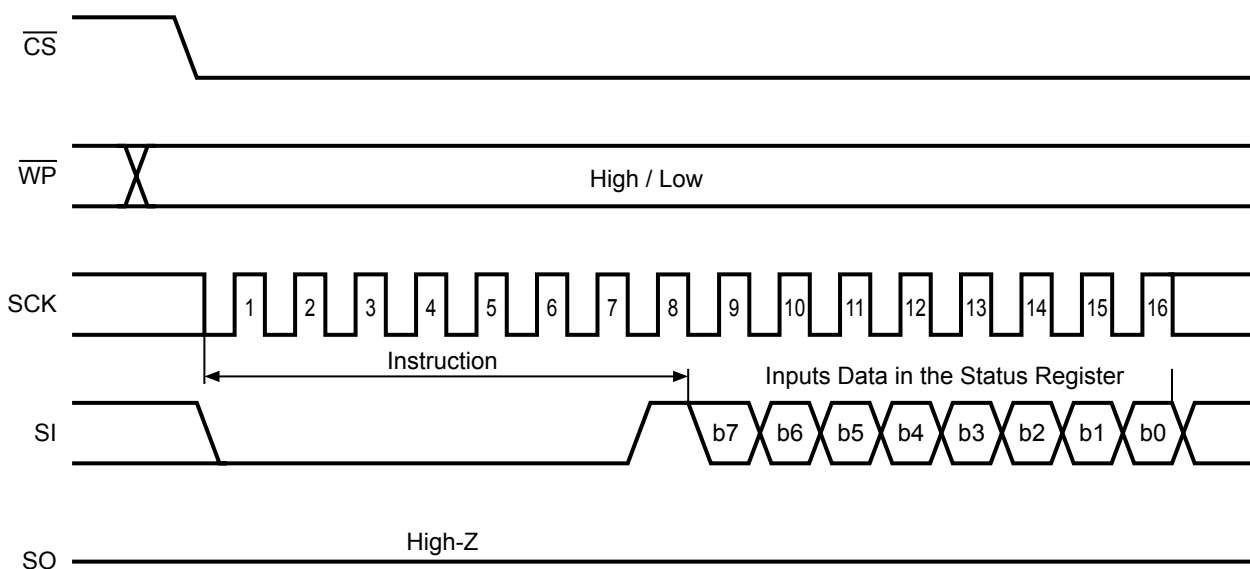


Figure 15 WRSR operation

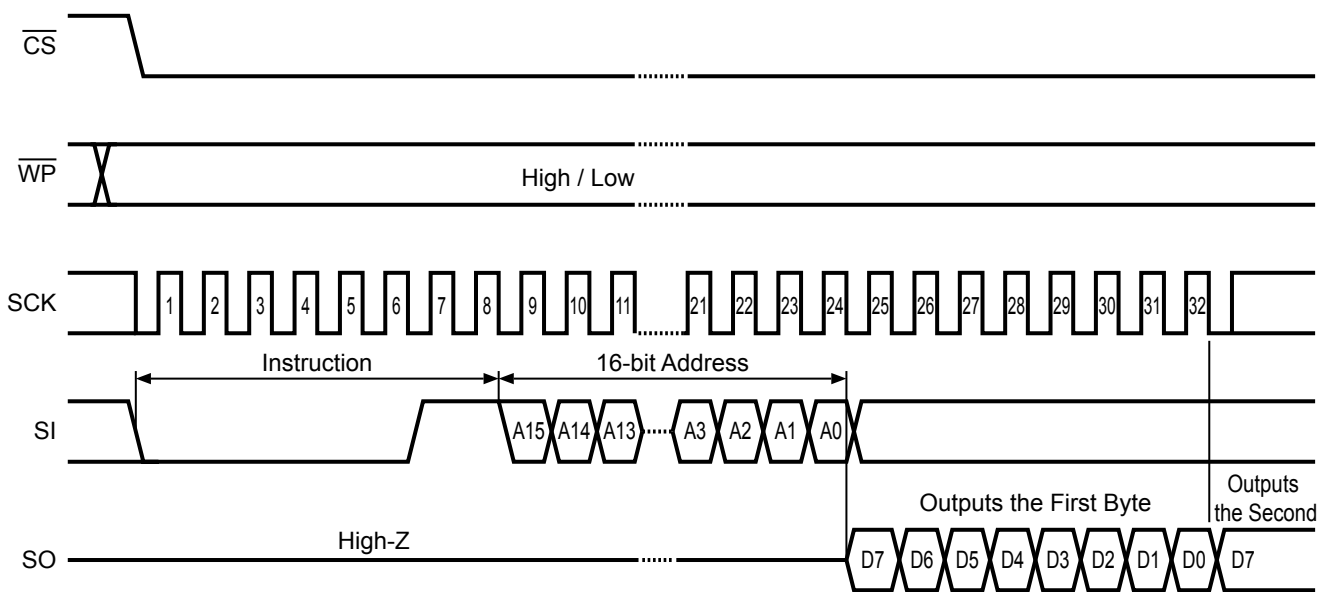


**6. Read memory data (Read)**

The Read operation is shown below. Input the instruction code and the address from serial data input (SI) after inputting “L” to the chip select ( $\overline{CS}$ ). The input address is loaded to the internal address counter, and data in the address is output from the serial data output (SO).

Next, by inputting the serial clock (SCK) keeping the chip select ( $\overline{CS}$ ) in “L”, the address is automatically incremented so that data in the following address is sequentially output. The address counter rolls over to the first address by increment in the last address.

To finish the Read cycle, set  $\overline{CS}$  to “H”. It is possible to raise the chip select always during the cycle. During Write, the read instruction code is not be accepted or operated.



**Remark** The higher addresses A15 to A10 = Don't care.

**Figure 16 Read operation**

**7. Write memory data (Write)**

Figure 17 shows the timing chart when inputting 1-byte data. Input the instruction code, the address and data from serial data input (SI) after inputting “L” to the chip select ( $\overline{CS}$ ). To start Write ( $t_{PR}$ ), set the chip select ( $\overline{CS}$ ) to “H” after inputting data or before inputting a rising of the next serial clock. Bit WIP and WEL are reset to “0” when Write has completed.

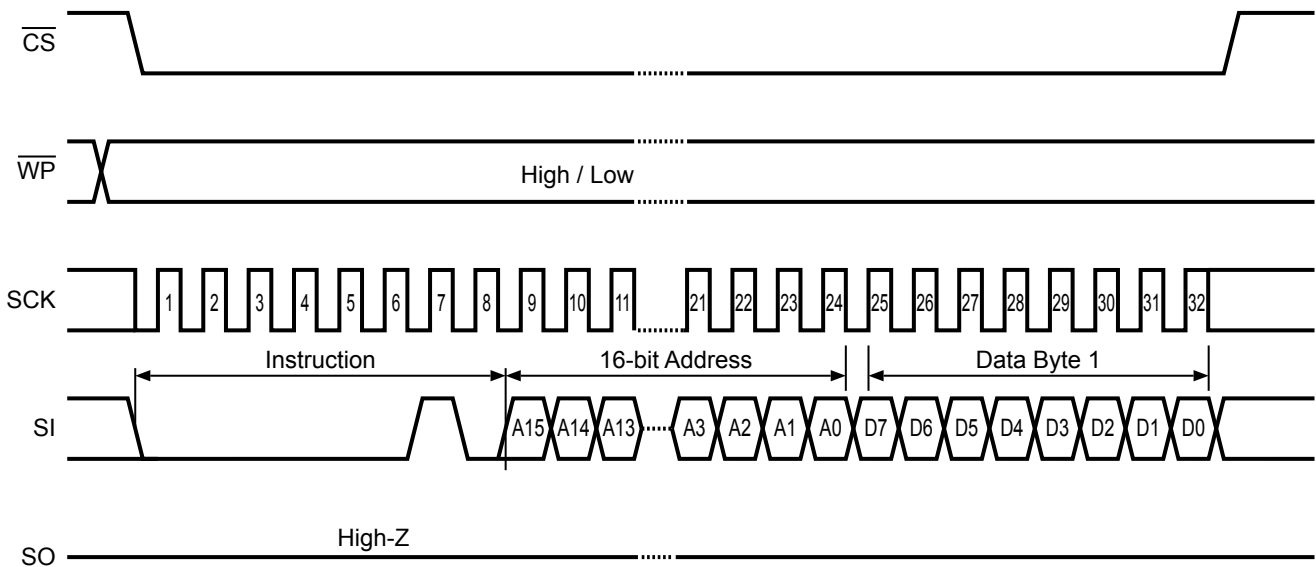
The S-25C080A can Page Write of 32 bytes. Its function to transmit data is as same as Byte Write basically, but it operates Page Write by receiving sequential 8-bit Write data as much data as page size has. Input the instruction code, the address and data from serial data input (SI) after inputting “L” in  $\overline{CS}$ , as the Write operation (page) shown in Figure 18. Input the next data while keeping  $\overline{CS}$  in “L”. After that, repeat inputting data of 8-bit sequentially. At the end, by setting  $\overline{CS}$  to “H”, the Write operation starts ( $t_{PR}$ ).

5 of the lower bits in the address are automatically incremented every time when receiving Write data of 8-bit. Thus, even if Write data exceeds 32 bytes, the higher bits in the address do not change. And 5 of lower bits in the address roll over so that Write data which is previously input is overwritten.

These are cases when the Write instruction is not accepted or operated.

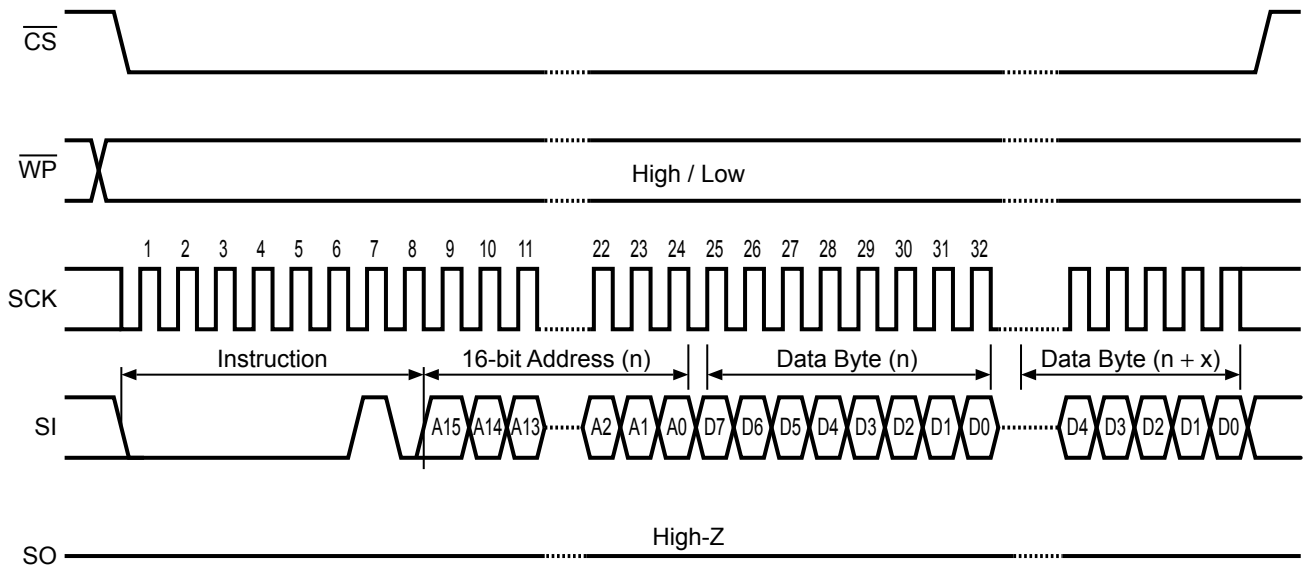
- Bit WEL is not set to “1” (not set to “1” beforehand immediately before the Write instruction)
- During Write
- The address to be written is in the protect area by BP1 and BP0.

To cancel the Write instruction, input the clock different from a specified value ( $n = 24 + m \times 8\text{clock}$ ) while  $\overline{CS}$  is in “L”.



**Remark** The higher addresses A15 to A10 = Don't care.

**Figure 17 Write operation (1 byte)**



**Remark** The higher addresses A15 to A10 = Don't care.

**Figure 18 Write operation (Page)**

**■ Protect Operation**

**Table 17** shows the block settings of Write protect. **Table 18** shows the protect operation for the device. As long as bit SRWD, the Status Register Write Disable bit, in the status register is reset to “0” (it is in reset before the shipment), the value of status register can be changed.

These are two statuses when bit SRWD is set to “1”.

- Write in the status register is possible; Write protect ( $\overline{WP}$ ) is in “H”.
- Write in the status register is impossible; Write protect ( $\overline{WP}$ ) is in “L”. Therefore the Write protect area which is set by protect bit (BP1, BP0) in the status register cannot be changed.

These operations are to set Hardware Protect (HPM).

- After setting bit SRWD, set Write protect ( $\overline{WP}$ ) to “L”.
- Set bit SRWD completed setting Write protect ( $\overline{WP}$ ) to “L”.

**Figure 9** and **10** show the Valid timing in Write protect and Invalid timing in Write protect during the cycle Write to the status register.

By inputting “H” to Write protect ( $\overline{WP}$ ), Hardware Protect (HPM) is released. If the Write protect ( $\overline{WP}$ ) is “H”, Hardware Protect (HPM) does not function, Software Protect (SPM) which is set by the protect bits in the status register (BP1, BP0) only works.

**Table 17 The block settings of Write protect**

Status register		The area of Write protect	Address of Write protect block
BP1	BP0		
0	0	0 %	None
0	1	25 %	300h to 3FFh
1	0	50 %	200h to 3FFh
1	1	100 %	000h to 3FFh

**Table 18 Protect operation**

Mode	$\overline{WP}$ pin	Bit SRWD	Bit WEL	Write protect block	General block	Status register
Software Protect (SPM)	1	X	0	Write disable	Write disable	Write disable
	1	X	1	Write disable	Write enable	Write enable
	X	0	0	Write disable	Write disable	Write disable
	X	0	1	Write disable	Write enable	Write enable
Hardware Protect (HPM)	0	1	0	Write disable	Write disable	Write disable
	0	1	1	Write disable	Write enable	Write disable

**Remark** X = Don't care

## ■ Hold Operation

The hold operation is used to pause serial communications without setting the device in the non-select status. In the hold status, the serial data output goes in high impedance, and both of the serial data input and the serial clock go in "Don't care". Be sure to set the chip select ( $\overline{CS}$ ) to "L" to set the device in the select status during the hold status.

Generally, during the hold status, the device holds the select status. But if setting the device in the non-select status, the users can finish the operation even in progress.

**Figure 19** shows the hold operation. Set Hold ( $\overline{HOLD}$ ) to "L" when the serial clock (SCK) is in "L", Hold ( $\overline{HOLD}$ ) is switched at the same time the hold status starts. If setting Hold ( $\overline{HOLD}$ ) to "H", Hold ( $\overline{HOLD}$ ) is switched at the same time the hold status ends.

Set Hold ( $\overline{HOLD}$ ) to "L" when the serial clock (SCK) is in "H"; the hold status starts when the serial clock goes in "L" after Hold ( $\overline{HOLD}$ ) is switched. If setting Hold ( $\overline{HOLD}$ ) to "H", the hold status ends when the serial clock goes in "L" after Hold ( $\overline{HOLD}$ ) is switched.

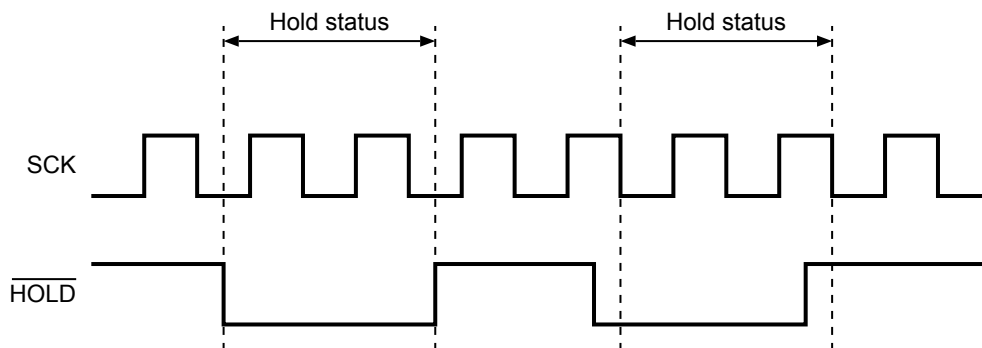


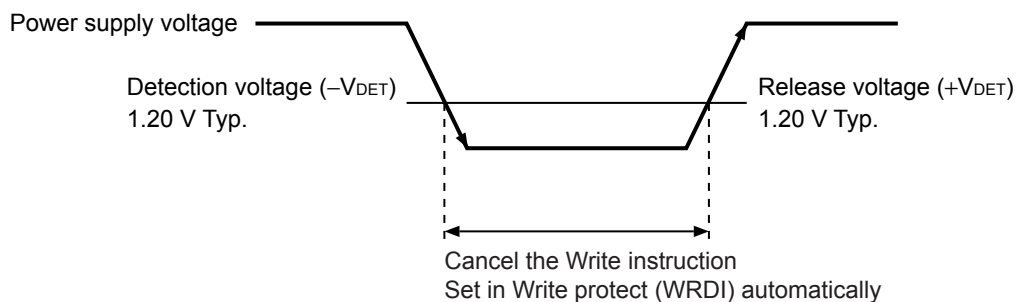
Figure 19 Hold operation

## ■ Write Protect Function during the Low Power Supply Voltage

The S-25C080A has a built-in detection circuit which operates with the low power supply voltage. The S-25C080A cancels the Write operation (WRITE, WRSR) when the power supply voltage drops and power-on, at the same time, goes in the Write protect status (WRDI) automatically to reset bit WEL. Its detection and release voltages are 1.20 V typ. (Refer to **Figure 20**).

To operate Write, after the power supply voltage dropped once but rose to the voltage level which allows Write again, be sure to set the Write Enable Latch bit (WEL) before operating Write (WRITE, WRSR).

In the Write operation, data in the address written during the low power supply voltage is not assured.



**Figure 20** Operation during low power supply voltage

## ■ I/O Pin

### 1. Connection of input pin

All input pins in S-25C080A have the CMOS structure. Do not set these pins in high impedance during operation when you design. Especially, set the  $\overline{CS}$  input in the non-select status "H" during power-on/off and standby. The error Write does not occur as long as the  $\overline{CS}$  pin is in the non-select status "H". Set the  $\overline{CS}$  pin to  $V_{CC}$  via a resistor (the pull-up resistor of 10 to 100 k $\Omega$ ).

To prevent the error for sure, it is recommended to set other input pins than the  $\overline{CS}$  pin via a pull-up resistor.

### 2. Equivalent circuit of I/O pin

**Figure 21** and **22** show the equivalent circuits of input pins in S-25C080A. A pull-up and pull-down elements are not included in each input pin, pay attention not to set it in the floating state when you design.

**Figure 23** shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" level/"L" level/high impedance.

## 2.1 Input pin

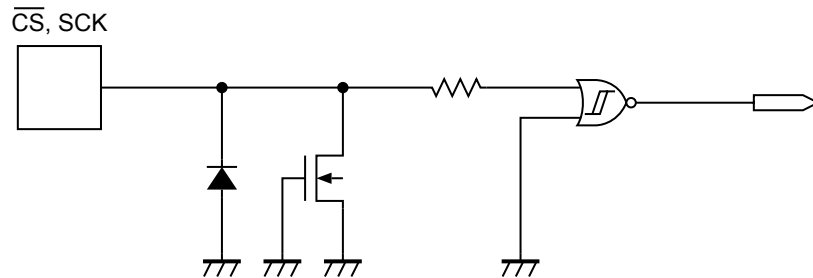


Figure 21  $\overline{\text{CS}}$ , SCK Pin

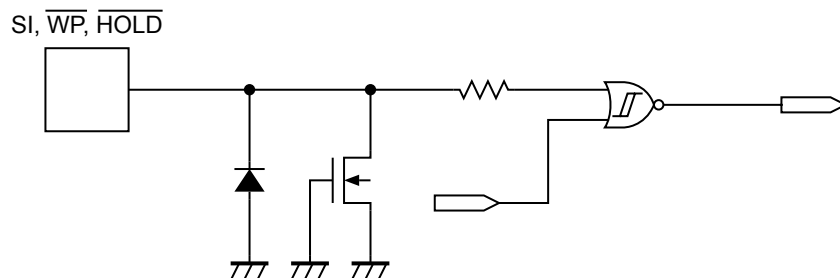


Figure 22 SI,  $\overline{\text{WP}}$ ,  $\overline{\text{HOLD}}$  Pin

## 2.2 Output pin

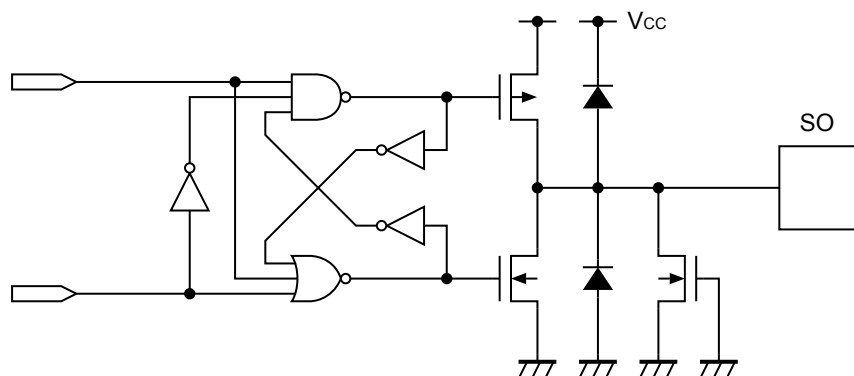


Figure 23 SO Pin

## 3. Precaution for use

- Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.
- Operations with moisture on the E<sup>2</sup>PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E<sup>2</sup>PROM up from low temperature tank during the evaluation. Be sure that not remain frost on the E<sup>2</sup>PROM pin to prevent malfunction by short-circuit. Also attention should be paid in using on environment, which is easy to dew for the same reason.

## ■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

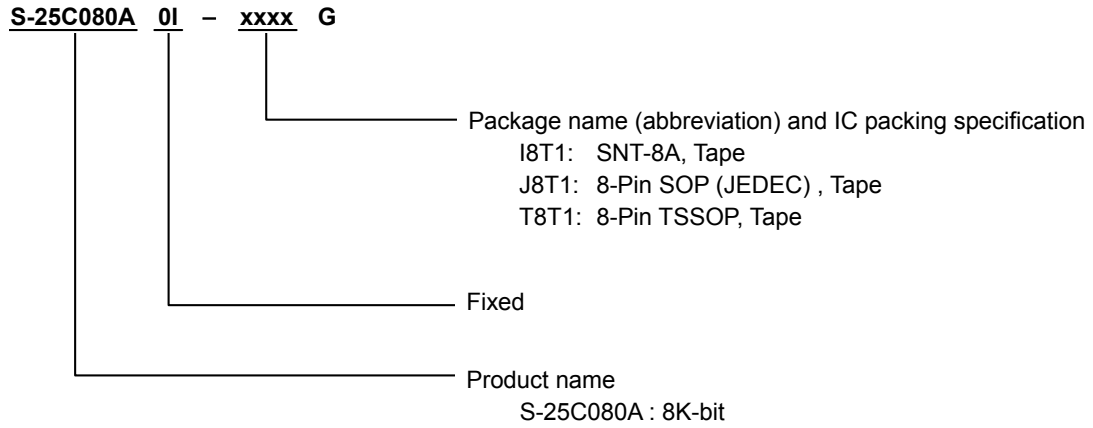
## ■ Precautions for WLP package

- The side of device silicon substrate is exposed to the marking side of device package. Since this portion has lower strength against the mechanical stress than the standard plastic package, chip, crack, etc should be careful of the handling of a package enough. Moreover, the exposed side of silicon has electrical potential of device substrate, and needs to be kept out of contact with the external potential.
- In this package, the overcoat of the resin of translucence is carried out on the side of device area. Keep it mind that it may affect the characteristic of a device when exposed a device in the bottom of a high light source.

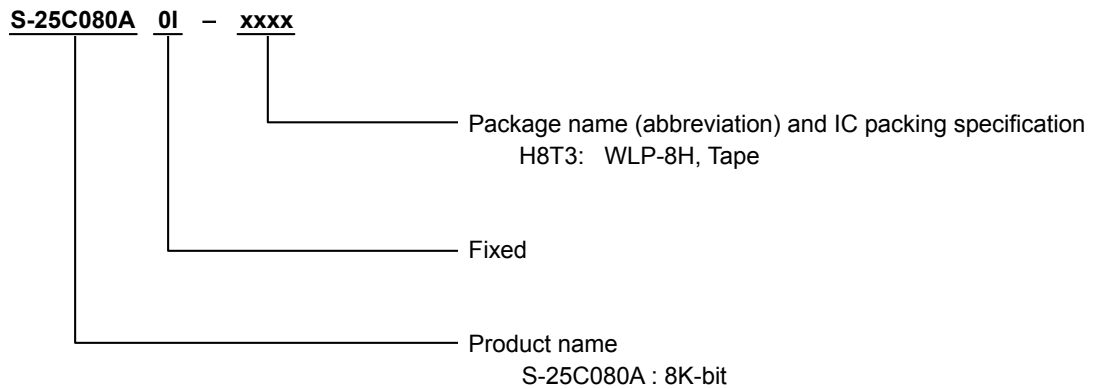


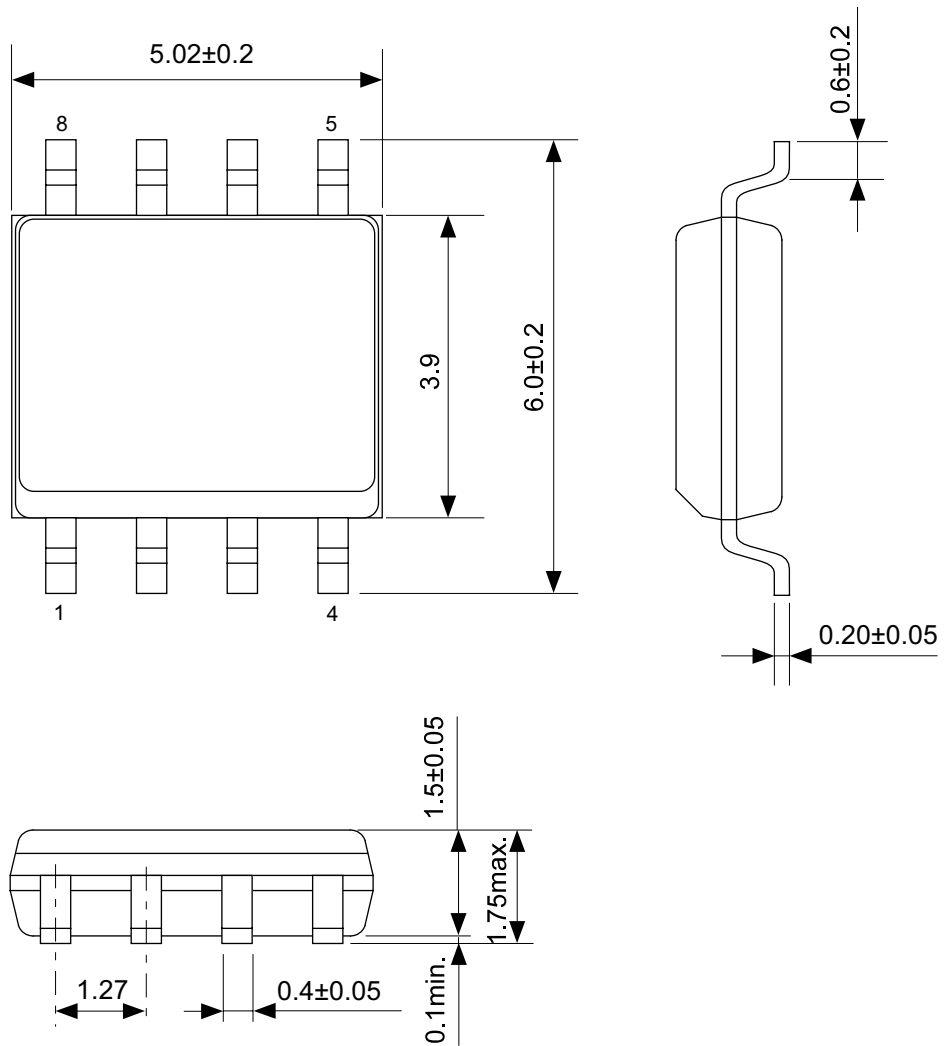
■ Product Name Structure

1. 8-Pin SOP(JEDEC), 8-Pin TSSOP, SNT-8A Packages



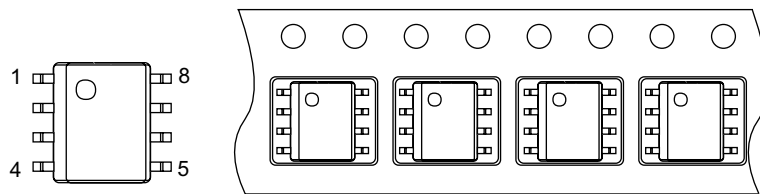
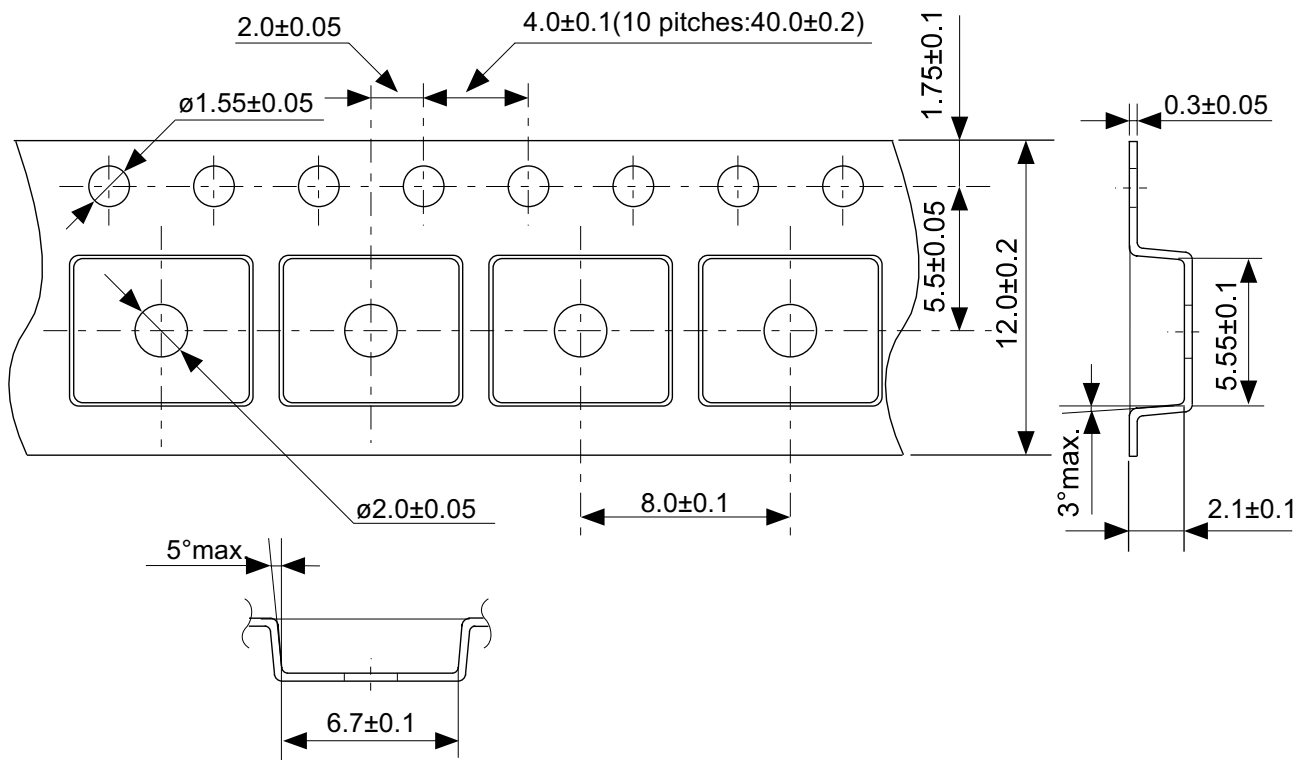
2. WLP-8H Package





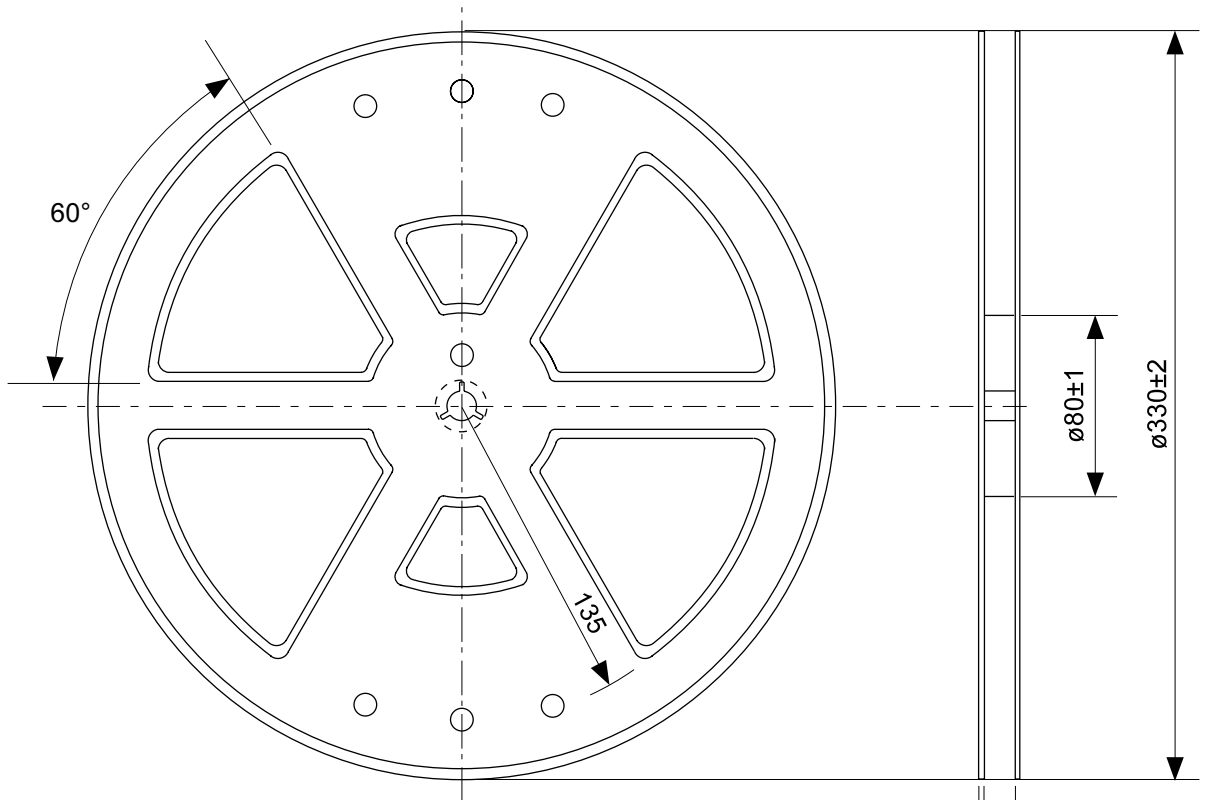
No. FJ008-A-P-SD-2.1

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

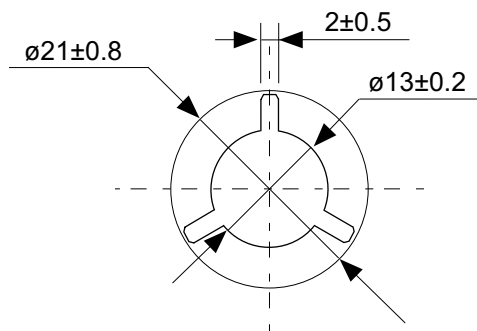


No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

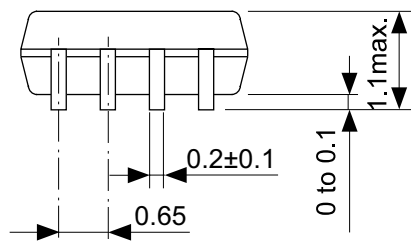
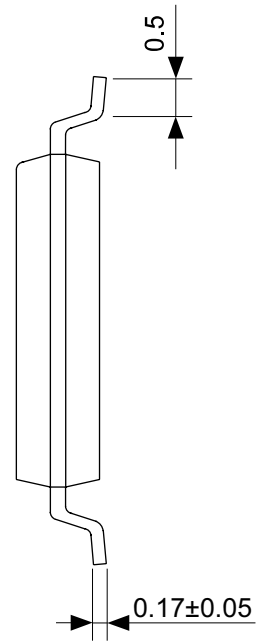
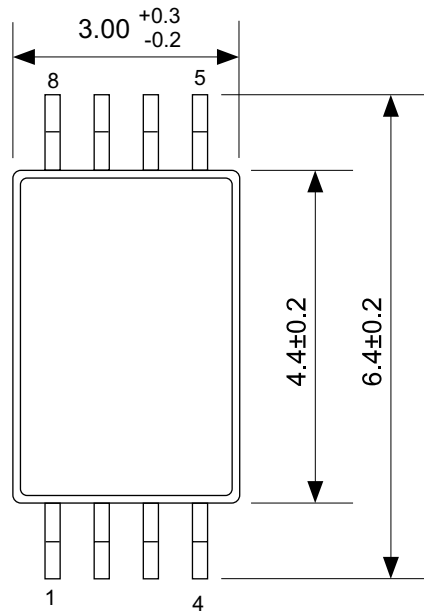


Enlarged drawing in the central part



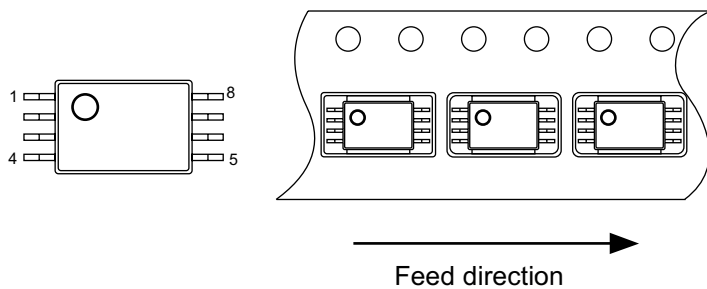
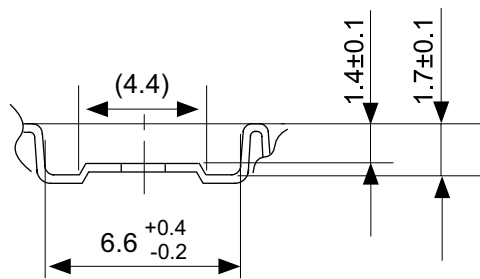
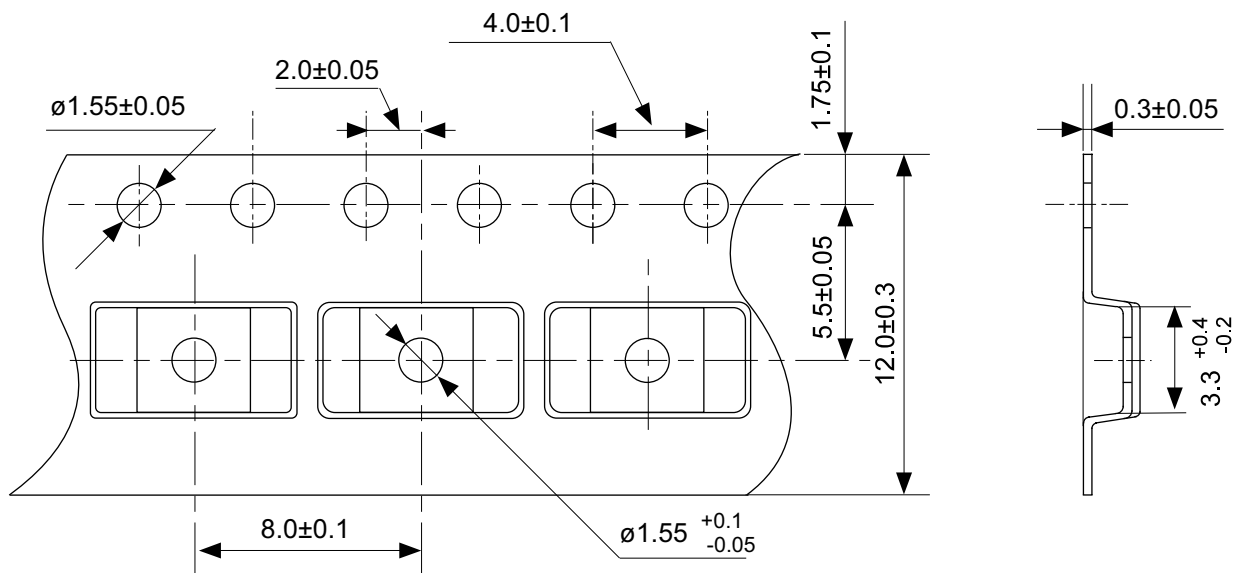
No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			



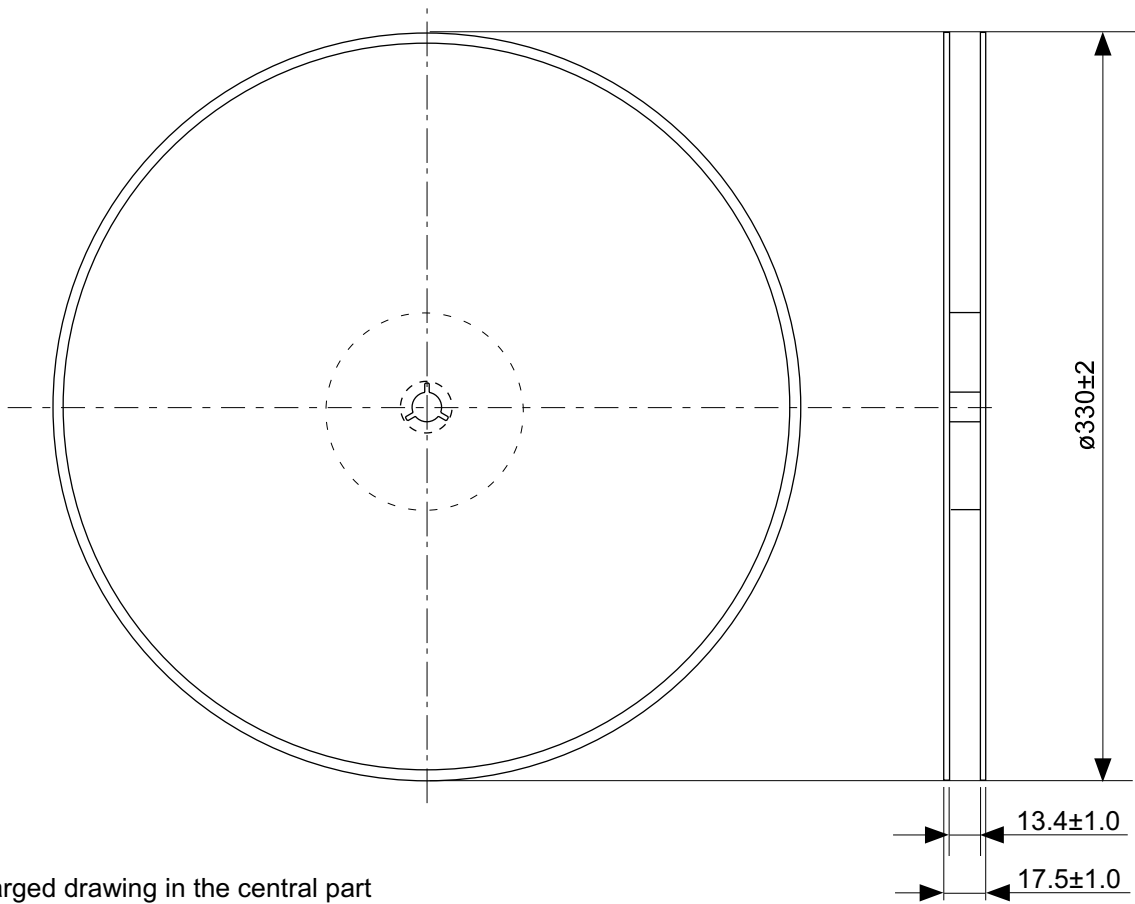
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

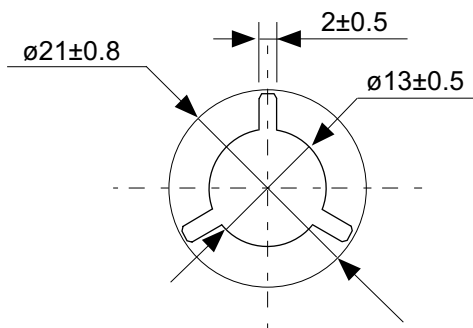


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

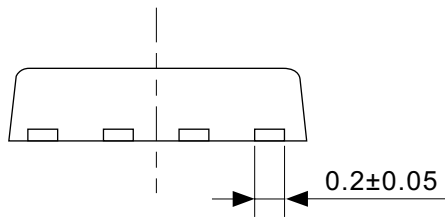
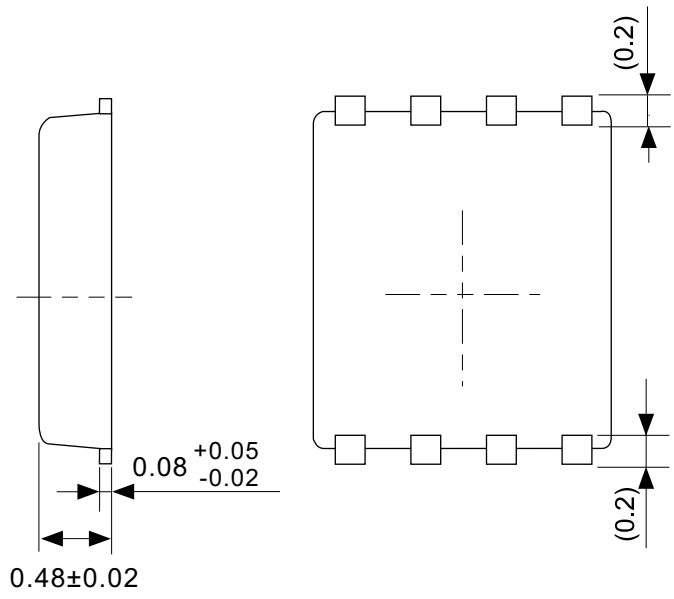
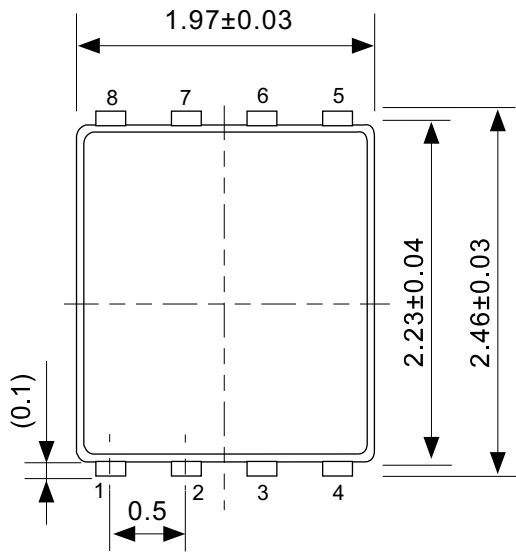


Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

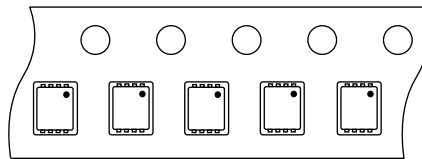
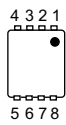
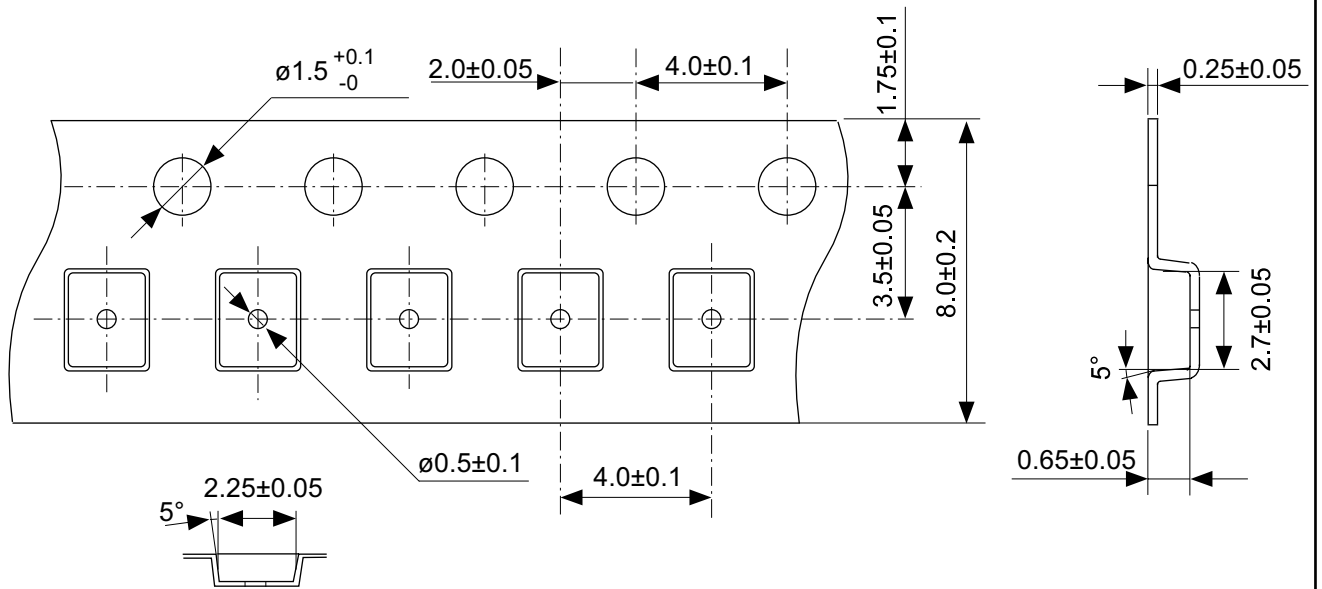
TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			



No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

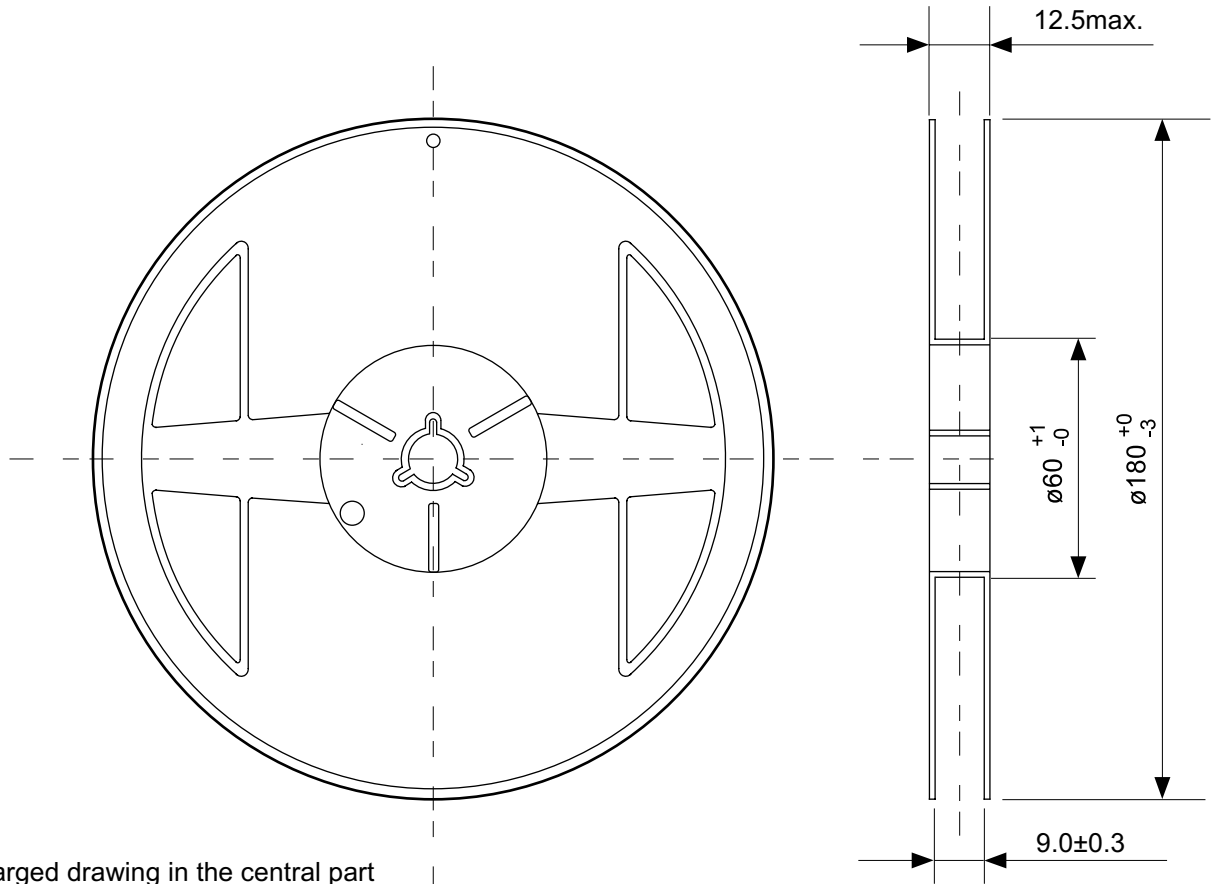




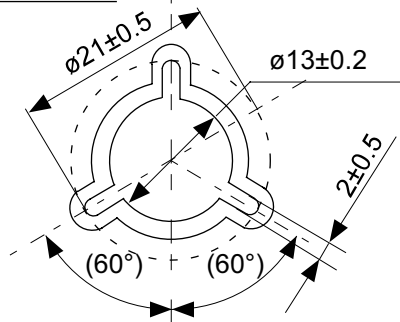
Feed direction

No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

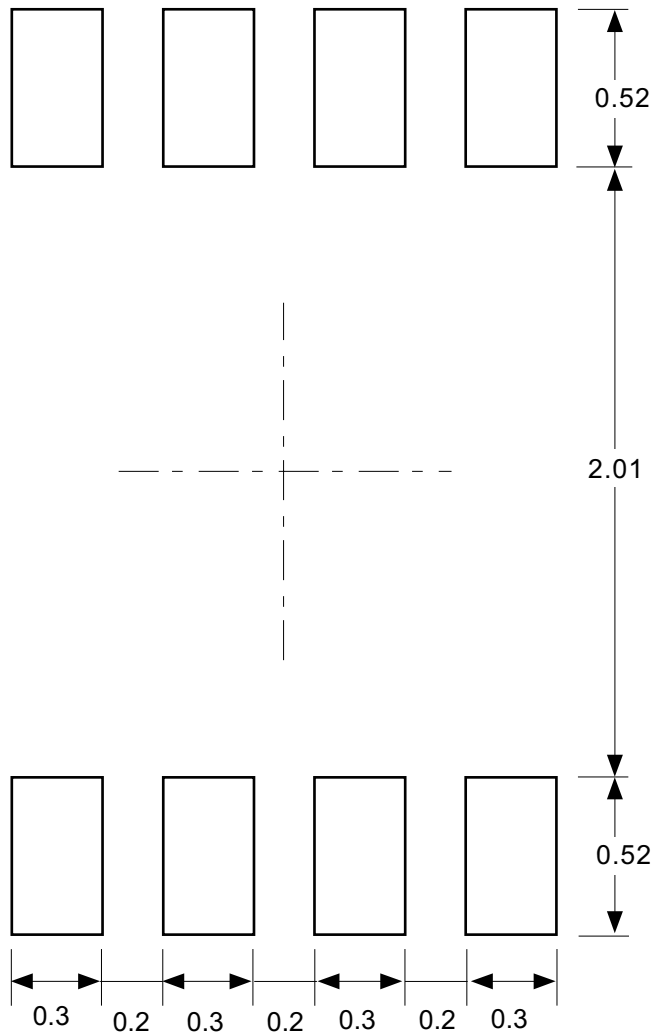


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

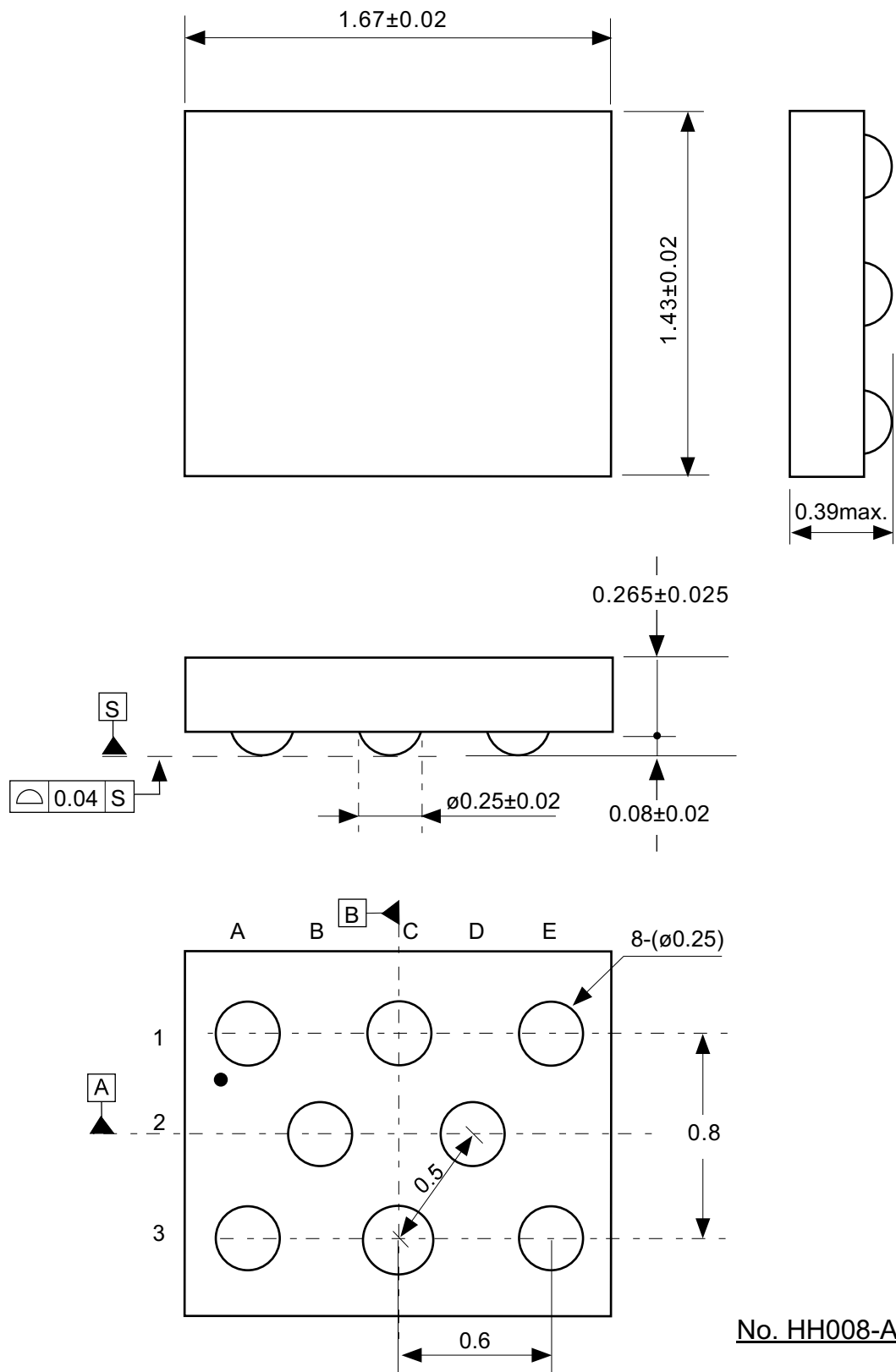


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がる場合がありますのでご配慮ください。

No. PH008-A-L-SD-3.0

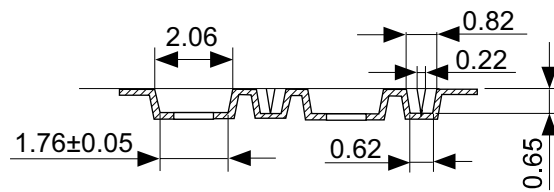
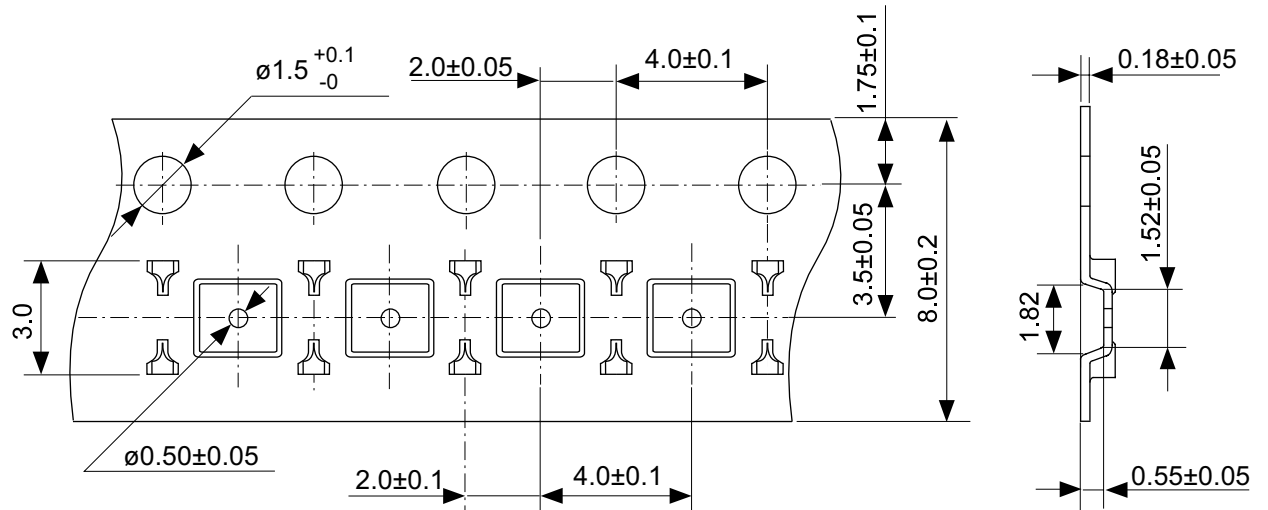
TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	




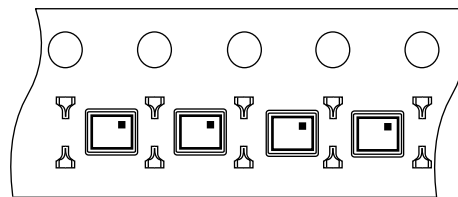
No. HH008-A-P-SD-1.0

TITLE	WLP-8H-A-PKG Dimensions
No.	HH008-A-P-SD-1.0
SCALE	
UNIT	mm

Seiko Instruments Inc.



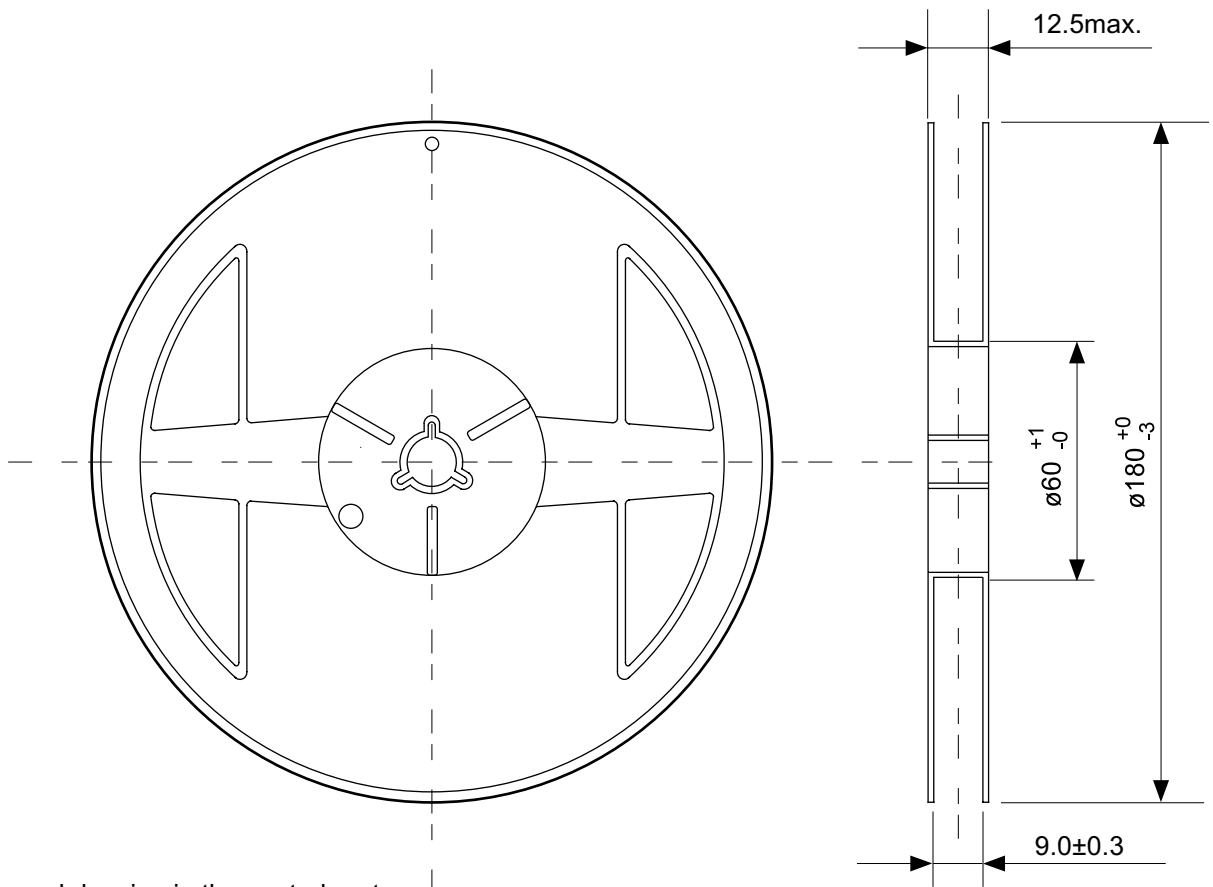
E1C1 A1  
  
 E3C3 A3



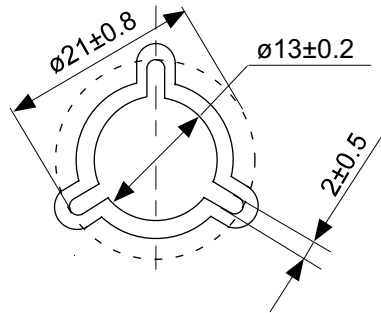
→  
 Feed direction

No. HH008-A-C-SD-1.0

TITLE	WLP-8H-A-Carrier Tape
No.	HH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. HH008-A-R-SD-1.0

TITLE	WLP-8H-A-Reel		
No.	HH008-A-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm	MATERIAL	PS
Seiko Instruments Inc.			

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.