

## NTE6664 Integrated Circuit 64K–Bit Dynamic RAM

**Description:**

The NTE6664 is a 65,536 Bit, high–speed, dynamic Random Access Memory. Organized as 65,536 one–bit words and fabricated using HMOS high–performance N–Channel silicon–gate technology, this 5V only dynamic RAM combines high performance with low cost and improved reliability.

By multiplying row– and column– address inputs, the NTE6664 requires only eight address lines and permits packaging in a standard 16–Lead DIP package. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by  $\overline{\text{CAS}}$  allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The NTE6664 incorporates a one–transistor cell design and dynamic storage techniques. In addition to the  $\overline{\text{RAS}}$ –only refresh mode, the refresh control function available on Pin1 provides two additional modes of refresh, automatic and self refresh.

**Features:**

- Single +5V Operation ( $\pm 10\%$ )
- Maximum Access Time: 150ns
- Low Power Dissipation:  
     302.5mW Max (Active)  
     22mW Max (Standby)
- Three State Data Output
- Early–Write Common I/O Capability
- 128 Cycle, 2ms Refresh
- Control on Pin1 for Automatic or Self Refresh
- $\overline{\text{RAS}}$ –Only Refresh Mode
- $\overline{\text{CAS}}$  Controlled Output
- Fast Page Mode Cycle Time
- Low Soft Error Rate: < 0.1% per 1000 Hrs

**Absolute Maximum Ratings:** (Note 1)

Voltage on $V_{CC}$ Supply Relative to $V_{SS}$ , $V_{CC}$ .....	–2 to +7V
Voltage Relative to $V_{SS}$ for Any Pin Except $V_{CC}$ , $V_{in}$ , $V_{out}$ .....	–1 to +7V
Data Out Current (Short Circuit), $I_{out}$ .....	50mA
Power Dissipation, $P_D$ .....	1W
Operating Temperature Range, $T_A$ .....	0 to +70°C
Storage Temperature Range, $T_{stg}$ .....	–65° to +150°C

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect the device reliability.

**Recommended Operating Conditions:** (Note 2,  $T_A = 0$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Logic 1 Voltage, All Inputs	$V_{IH}$	2.4	–	6.5	V
Logic 0 Voltage, All Inputs (Note 3)	$V_{IL}$	–1.0	–	0.8	V

Note 2. All voltages referenced to  $V_{SS}$ .

Note 3. The device will withstand undershoots to the  $-2\text{V}$  level with a maximum pulse width of 20ns at the  $-1.5\text{V}$  level. This is periodically sampled rather than 100% tested.

**DC Characteristics:** ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$V_{CC}$ Power Supply Current	$I_{CC1}$	$t_{RC} = 270\text{ns}$ , Note 4	–	–	55	mA
$V_{CC}$ Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS} = \overline{CAS} = V_{IH}$	–	–	4	mA
$V_{CC}$ Power Supply Current During $\overline{RAS}$ only Refresh Cycles	$I_{CC3}$	$t_{RC} = 270\text{ns}$ , Note 4	–	–	45	mA
Input Leakage Current Any Input Except REFRESH	$I_{lkg(L)}$	$V_{SS} < V_{in} < V_{CC}$	–	–	10	$\mu\text{A}$
REFRESH Input Current	$I_{lkg(F)}$	$V_{SS} < V_{in} < V_{CC}$	–	–	20	$\mu\text{A}$
Output Leakage Current	$I_{lkg(O)}$	$\overline{CAS}$ at Logic 1, $0 \leq V_{out} \leq 5.5\text{V}$	–	–	10	$\mu\text{A}$
Output Logic 1 Voltage	$V_{OH}$	$I_{out} = -4\text{mA}$	2.4	–	–	V
Output Logic 0 Voltage	$V_{OL}$	$I_{out} = 4\text{mA}$	–	–	0.4	V

Note 4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.

**Capacitance:** ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $f = 1\text{MHz}$ ,  $T_A = +25^\circ\text{C}$ , Note 5, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance A0 – A7, D RAS, CAS, WRITE, REFRESH	$C_{in}$		–	3	5	pF
			–	6	8	
Output Capacitance Q	$C_{out}$	$\overline{CAS} = V_{IH}$ to Disable Output	–	5	7	pF

Note 5. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation:  $C = I\Delta t/\Delta V$ .

**Read, Write, and Read–Modify–Write Cycles:** ( $V_{CC} = 5\text{V} \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$  unless otherwise specified, Notes 6, 7, and 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Random Read or Write Cycle Time	$t_{RC}$	Note 9, Note 10	270	–	–	ns
Read–Write Cycle Time	$t_{RWC}$	Note 9, Note 10	280	–	–	ns
Access Time from $\overline{RAS}$	$t_{RAC}$	Note 11, Note 13	–	–	150	ns
Access Time from $\overline{CAS}$	$t_{CAC}$	Note 12, Note 13	–	–	75	ns
Output Buffer and Turn–Off Delay	$t_{OFF}$	Note 19	0	–	30	ns
$\overline{RAS}$ Precharge Time	$t_{RP}$		100	–	–	ns
$\overline{RAS}$ Pulse Width	$t_{RAS}$		150	–	10000	ns
$\overline{CAS}$ Pulse Width	$t_{CAS}$		75	–	10000	ns

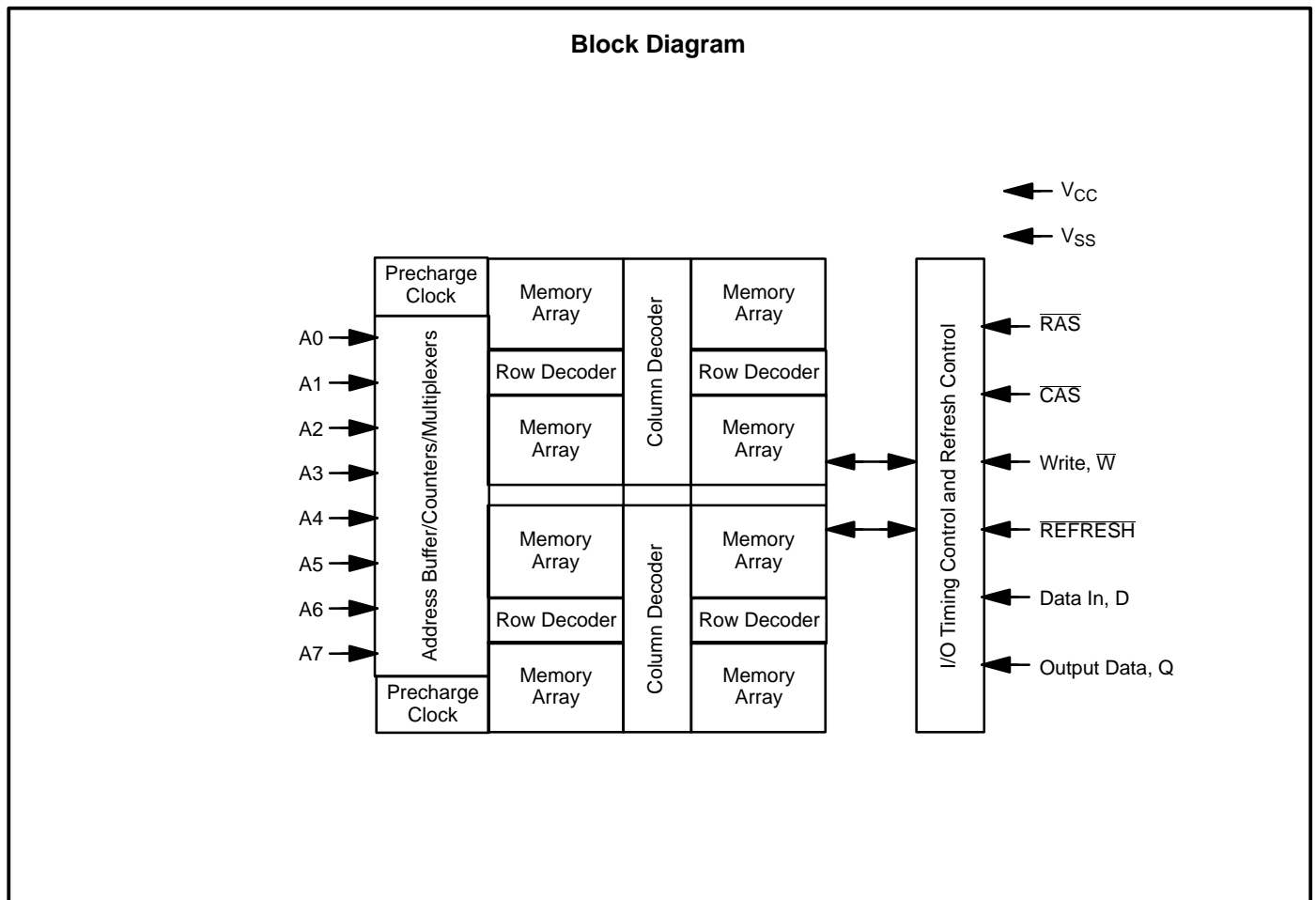
**Read, Write, and Read–Modify–Write Cycles (Cont'd):** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0$  to  $+70^\circ\text{C}$  unless otherwise specified, Notes 6, 7, and 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
RAS to CAS Delay Time	$t_{\text{RCD}}$	Note 14	25	–	75	ns
Row Address Setup Time	$t_{\text{ASR}}$		0	–	–	ns
Row Address Hold Time	$t_{\text{RAH}}$		20	–	–	ns
Column Address Setup Time	$t_{\text{ASC}}$		0	–	–	ns
Column Address Hold Time	$t_{\text{CAH}}$		35	–	–	ns
Column Address Hold Time Referenced to RAS	$t_{\text{AR}}$	Note 18	95	–	–	ns
Transition Time (Rise and Fall)	$t_{\text{T}}$		3	–	50	ns
Read Command Setup Time	$t_{\text{RCS}}$		0	–	–	ns
Read Command Hold Time Referenced to CAS	$t_{\text{RCH}}$	Note 15	0	–	–	ns
Read Command Hold Time Referenced to RAS	$t_{\text{RRH}}$	Note 15	0	–	–	ns
Write Command Hold Time	$t_{\text{WCH}}$		35	–	–	ns
Write Command Hold Time Referenced to RAS	$t_{\text{WCR}}$	Note 18	95	–	–	ns
Write Command Pulse Width	$t_{\text{WP}}$		35	–	–	ns
Write Command to RAS Lead Time	$t_{\text{RWL}}$		45	–	–	ns
Write Command to CAS Lead Time	$t_{\text{CWL}}$		45	–	–	ns
Data in Setup Time	$t_{\text{DS}}$	Note 16	0	–	–	ns
Data in Hold Time	$t_{\text{DH}}$	Note 16	35	–	–	ns
Data in Hold Time Referenced to RAS	$t_{\text{DHR}}$	Note 18	95	–	–	ns
CAS to RAS Precharge Time	$t_{\text{CRP}}$		–10	–	–	ns
RAS Hold Time	$t_{\text{RSH}}$		75	–	–	ns
Refresh Period	$t_{\text{REFSH}}$		–	–	2	ms
Write Command Setup Time	$t_{\text{WCS}}$	Note 17	–10	–	–	ns
CAS to Write Delay	$t_{\text{CWD}}$	Note 17	45	–	–	ns
RAS to Write Delay	$t_{\text{RWD}}$	Note 17	120	–	–	ns
CAS Hold Time	$t_{\text{CSH}}$		150	–	–	ns
CAS Precharge Time (Page Mode Cycle Only)	$t_{\text{CP}}$		60	–	–	ns
Page Mode Cycle Time	$t_{\text{PC}}$		145	–	–	ns
RAS to REFRESH Delay	$t_{\text{RFD}}$		–10	–	–	ns
REFRESH Period (Battery Backup Mode)	$t_{\text{FBP}}$		2000	–	–	ns
REFRESH to RAS Precharge Time (Battery Backup Mode)	$t_{\text{FBR}}$		320	–	–	ns
REFRESH Cycle Time (Auto Pulse Mode)	$t_{\text{FC}}$		270	–	–	ns
REFRESH Pulse Period (Auto Period Mode)	$t_{\text{FP}}$		60	–	2000	ns
REFRESH to RAS Setup Time (Auto Pulse Mode)	$t_{\text{FSR}}$		–30	–	–	ns
REFRESH to RAS Delay Time (Auto Pulse Mode)	$t_{\text{FRD}}$		320	–	–	ns
REFRESH Inactive Time	$t_{\text{FI}}$		60	–	–	ns
RAS to REFRESH Lead Time	$t_{\text{FRL}}$		370	–	–	ns
RAS Inactive Time During REFRESH	$t_{\text{FRI}}$		370	–	–	ns

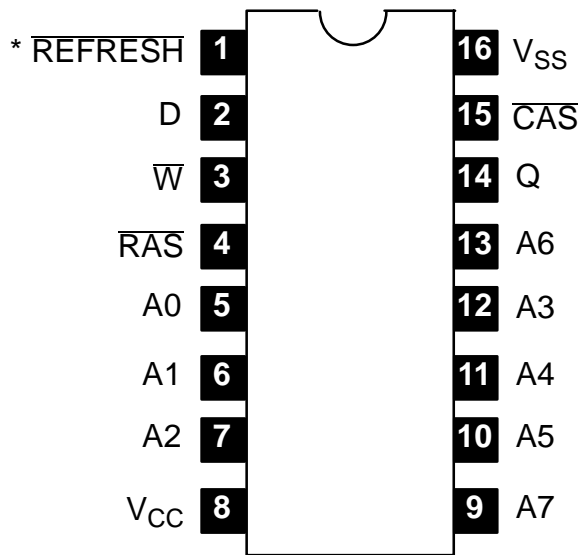
Note 6.  $V_{\text{IH}}$  min and  $V_{\text{IL}}$  max are reference levels for measuring timing of input signals. Transition times are measured between  $V_{\text{IH}}$  and  $V_{\text{IL}}$ .

Note 7. An initial pause of 100 $\mu\text{s}$  is required after power-up followed by 8 RAS cycles before proper device operation is guaranteed.

- Note 8. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- Note 9. The specification for  $t_{RC}(\min)$  and  $t_{RMW}(\min)$  are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ) is assured.
- Note 10. AC measurements  $t_T = 5\text{ns}$ .
- Note 11. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ .
- Note 12. Assumes that  $t_{RCD} \geq t_{RCD}(\max)$ .
- Note 13. Measured with a current load equivalent to 2 TTL ( $-200\mu\text{A}$ ,  $+4\text{mA}$ ) loads and  $100\text{pF}$  with the data output trip points set at  $V_{OH} = 2\text{V}$  and  $V_{OL} = 0.8\text{V}$ .
- Note 14. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met,  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Note 15. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
- Note 16. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in random write cycles and to  $\overline{\text{WRITE}}$  leading edge in delayed write or read-modify-write cycles.
- Note 17.  $t_{WCS}$ ,  $t_{CWD}$ , and  $t_{RWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \geq t_{CWD}(\min)$  and  $t_{RWD} \geq t_{RWD}(\min)$ , the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- Note 19.  $t_{OFF}(\max)$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.



### Pin Connection Diagram



\* If pin is not used, it should be connected to V<sub>CC</sub> through a 10k resistor.

