8-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT30 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT30 provide the 8-input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL HC	TYPICAL HCT	UNIT
$t_{PHL}/$ t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y	$C_L = 15$ pF $V_{CC} = 5$ V	12	12	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	15	15	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
f_o = output frequency in MHz V_{CC} = supply voltage in V
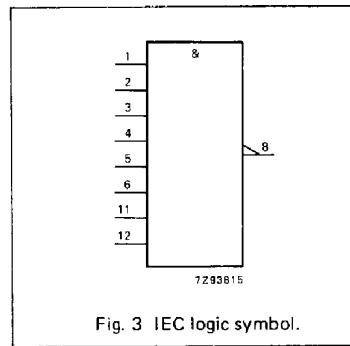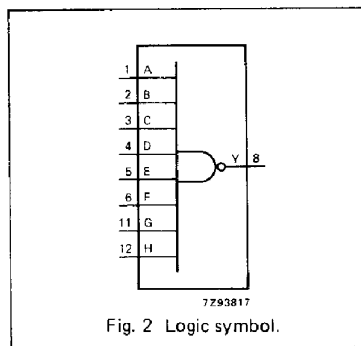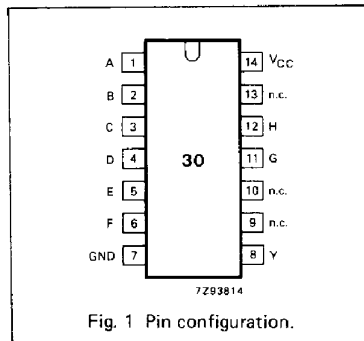$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
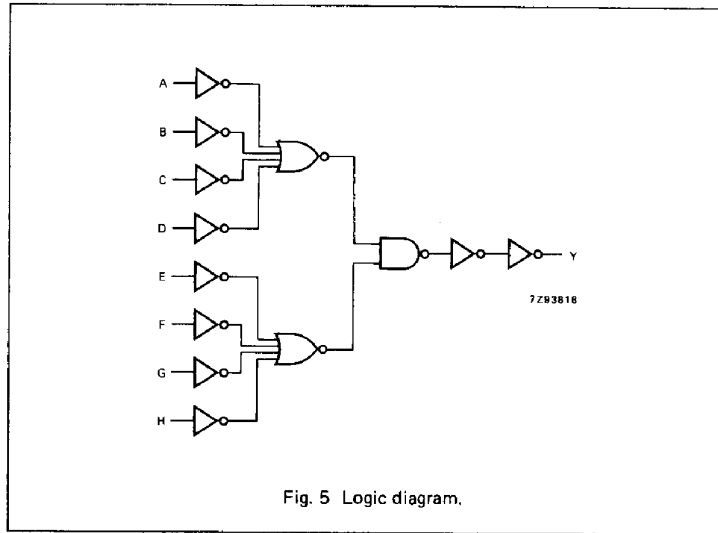For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

14-lead DIL; plastic (SOT27).
14-lead mini-pack; plastic (SO14; SOT108A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	A	data input
2	B	data input
3	C	data input
4	D	data input
5	E	data input
6	F	data input
7	GND	ground (0 V)
8	Y	data output
9, 10, 13	n.c.	not connected
11	G	data input
12	H	data input
14	V_{CC}	positive supply voltage

Fig. 1 Pin configuration.

Fig. 2 Logic symbol.

Fig. 3 IEC logic symbol.

Fig. 4 Functional diagram;
Y = $\overline{ABCDEFGH}$.

Fig. 5 Logic diagram.
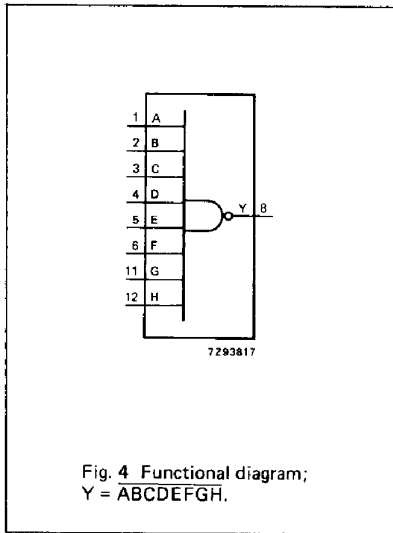
FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74 HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC							UNIT	V_{CC} V	TEST CONDITIONS WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y		41 15 12	130 26 22		165 33 28		195 39 33	ns	2.0 4.5 6.0	Fig. 6
$t_{THL}/$ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
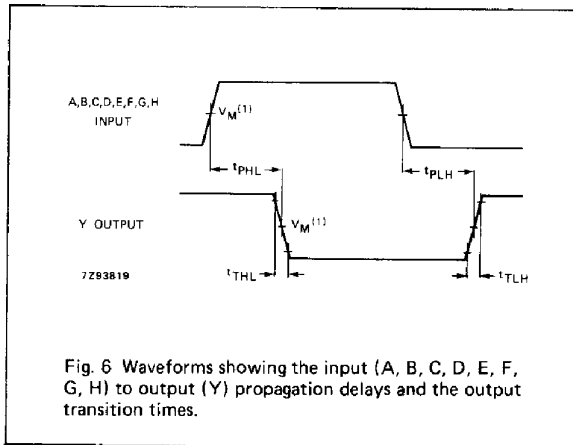I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current ($\triangle I_{CC}$) for a unit load of 1 is given in the family specifications.
To determine $\triangle I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A, B, C, D, E, F, G, H	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT							UNIT	V_{CC} V	TEST CONDITIONS WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
$t_{PHL}/$ t_{PLH}	propagation delay A, B, C, D, E, F, G, H to Y		16	28		35		42	ns	4.5	Fig. 6
$t_{THL}/$ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6

AC WAVEFORMS

A,B,C,D,E,F,G,H
INPUT V_M[1]

Y OUTPUT V_M[1]

7Z93819

t_{PHL} t_{PLH}

t_{THL} t_{TLH}

Fig. 6 Waveforms showing the input (A, B, C, D, E, F, G, H) to output (Y) propagation delays and the output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
    HCT: V_M = 1.3 V; V_I = GND to 3 V.