

QUAD 2-INPUT AND GATE

FEATURES

- Output capability: standard
- ICC category: SSI

GENERAL DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY	C _L = 15 pF V _{CC} = 5 V	7	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

- f_i = input frequency in MHz
- f_o = output frequency in MHz
- Σ (C_L × V_{CC}² × f_o) = sum of outputs
- C_L = output load capacitance in pF
- V_{CC} = supply voltage in V

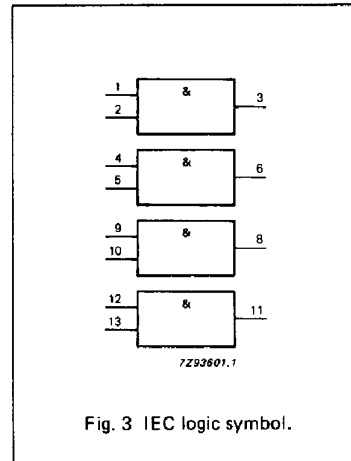
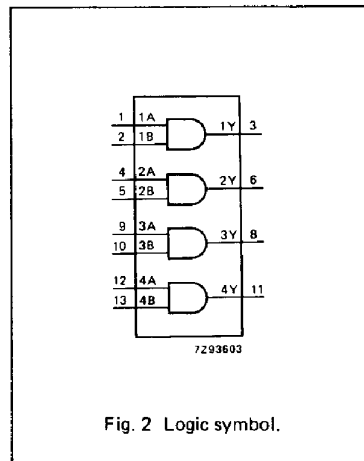
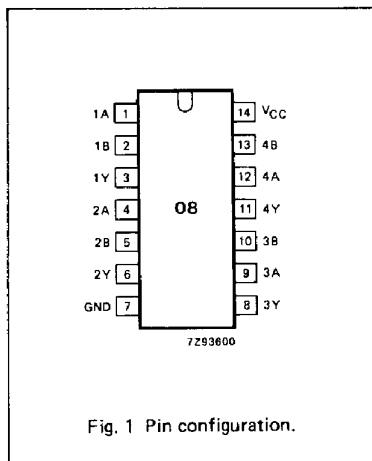
2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

- 14-lead DIL; plastic (SOT27)
- 14-lead mini pack; plastic (SO14; SOT108A)

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V _{CC}	positive supply voltage



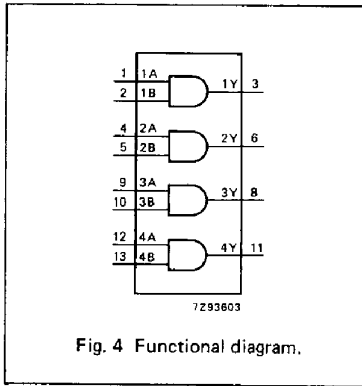


Fig. 4 Functional diagram.

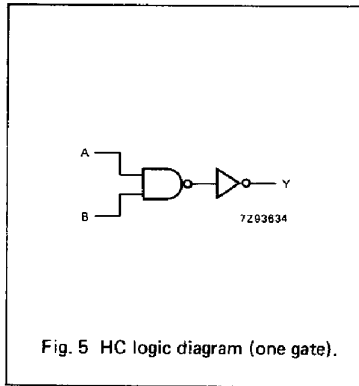


Fig. 5 HC logic diagram (one gate).

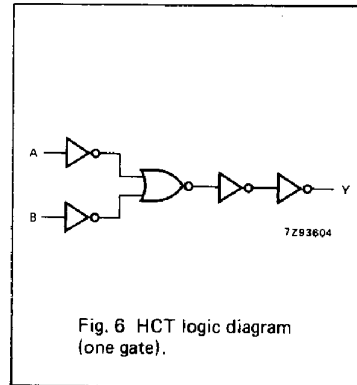


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{pHL} / t _{pLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0 Fig. 7	
t _{rHL} / t _{rLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0 Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

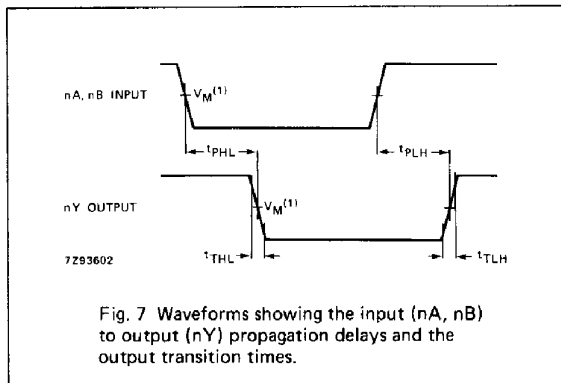
INPUT	UNIT LOAD COEFFICIENT
nA, nB	0.6

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY		14	24		30		36	ns	4.5	Fig. 7
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.