DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4067B MSI
16-channel analogue multiplexer/demultiplexer

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

16-channel analogue multiplexer/demultiplexer

HEF4067B MSI

DESCRIPTION

The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

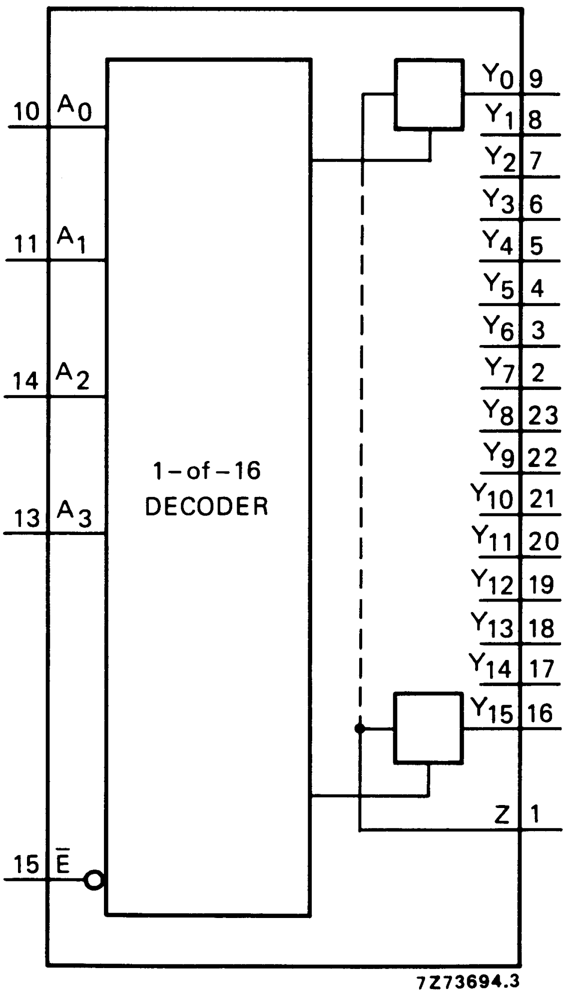


Fig.1 Functional diagram.

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3.

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

HEF4067BP(N):	24-lead DIL; plastic (SOT101-1)
HEF4067BD(F):	24-lead DIL; ceramic (cerdip) (SOT94)
HEF4067BT(D):	24-lead SO; plastic (SOT137-1)

( ): Package Designator North America

PINNING

Y_0 to Y_{15}	independent inputs/outputs
A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
Z	common input/output

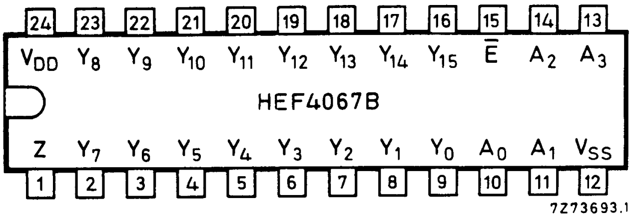


Fig.2 Pinning diagram.

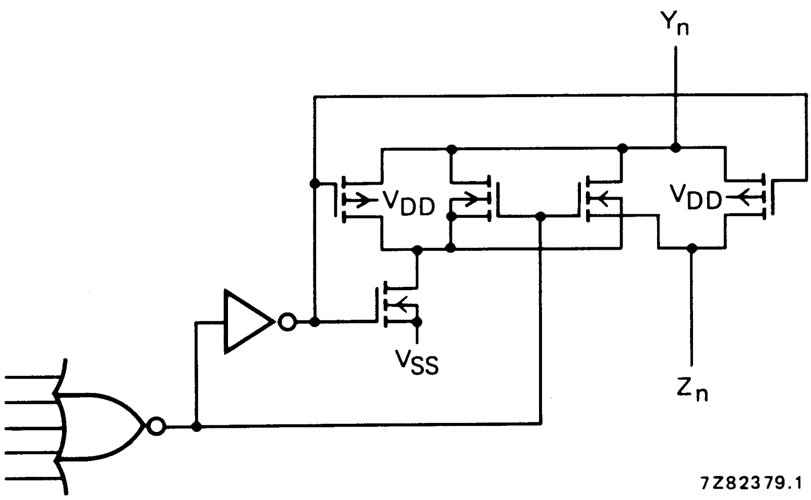


Fig.3 Schematic diagram (one switch).

FUNCTION TABLE

INPUTS					CHANNEL
$\overline{E}$	A_3	A_2	A_1	A_0	ON
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	none

Note

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial

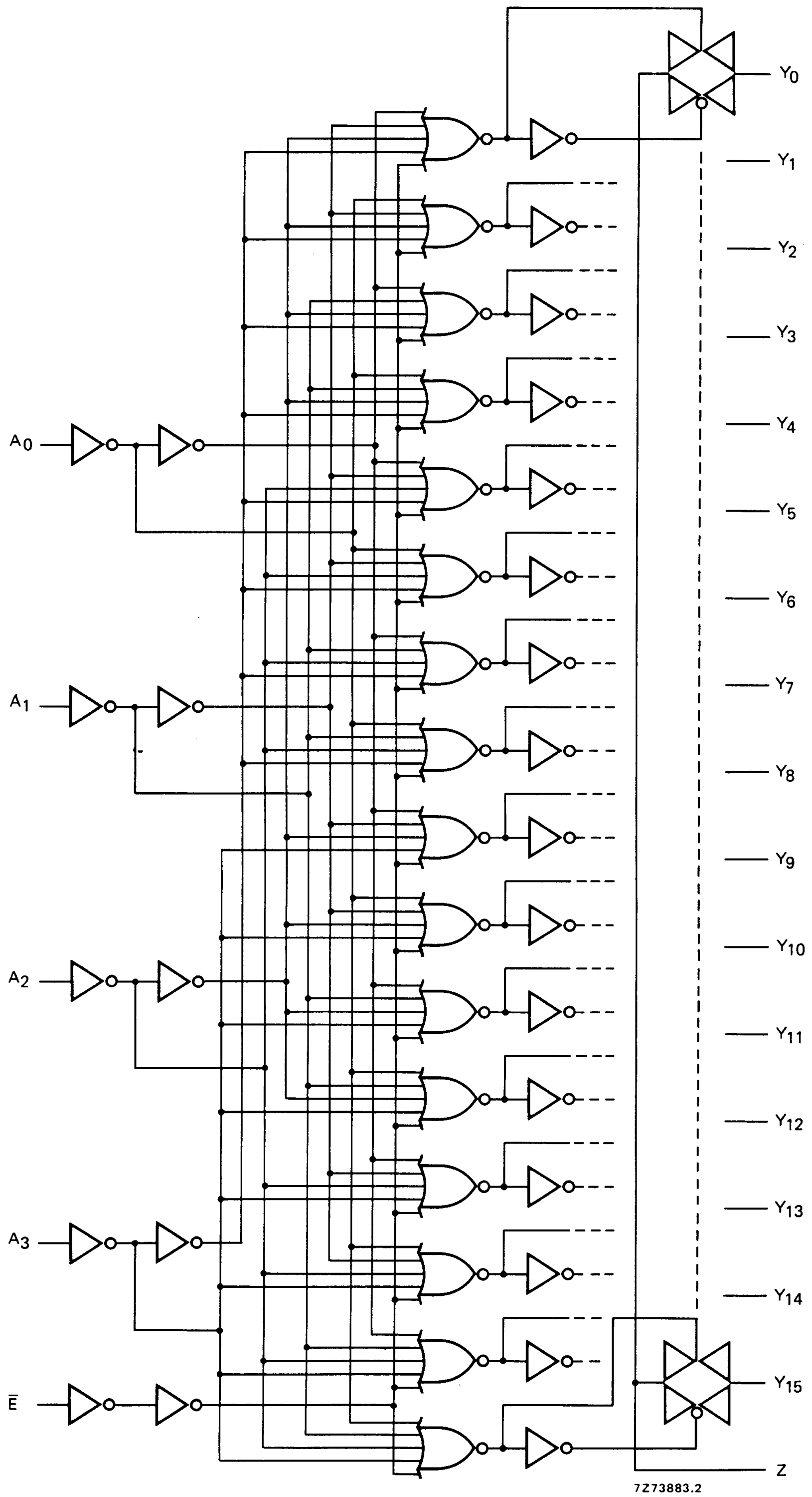


Fig.4 Logic diagram.

DC CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	SYMBOL	TYP.	MAX.		CONDITIONS
ON resistance	5	R_{ON}	350	2500	Ω	V_{is} = V_{SS} to V_{DD} see Fig.5
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_{is} = V_{SS} see Fig.5
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_{is} = V_{DD} see Fig.5
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	25	–	Ω	V_{is} = V_{SS} to V_{DD} see Fig.5
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

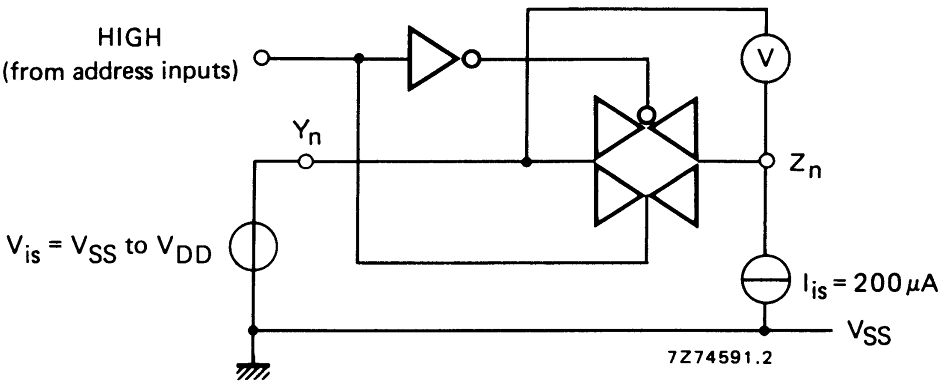
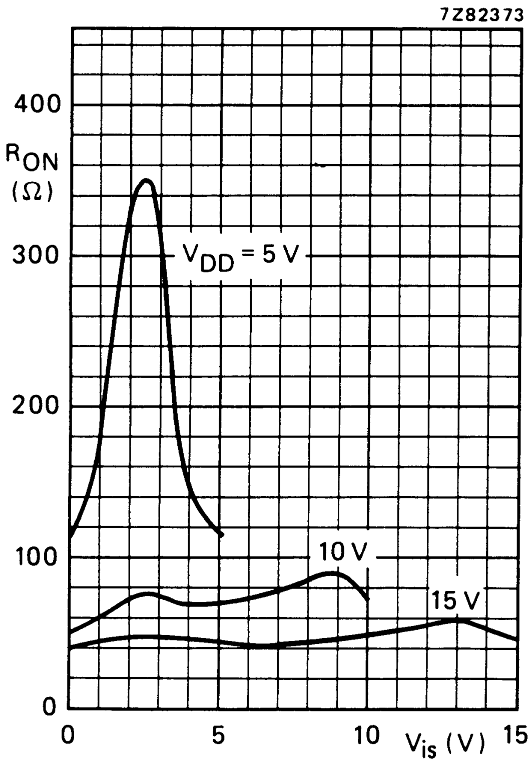


Fig.5 Test set-up for measuring R_{ON}.



I_{is} = 200 μA
V_{SS} = 0 V

Fig.6 Typical R_{ON} as a function of input voltage.

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS}.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,100\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$5\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$13\,300\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS (1), (2)

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		30	60	ns	
HIGH to LOW	10	t_{PHL}	15	25	ns	note 3
	15		10	20	ns	
	5		25	50	ns	
LOW to HIGH	10	t_{PLH}	10	20	ns	note 3
	15		10	20	ns	
$A_n \rightarrow V_{os}$	5		190	380	ns	
HIGH to LOW	10	t_{PHL}	70	145	ns	note 4
	15		50	100	ns	
	5		175	345	ns	
LOW to HIGH	10	t_{PLH}	70	140	ns	note 4
	15		50	100	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		195	385	ns	
HIGH	10	t_{PHZ}	140	280	ns	note 5
	15		130	260	ns	
	5		215	435	ns	
LOW	10	t_{PLZ}	180	355	ns	note 5
	15		170	340	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		155	315	ns	
HIGH	10	t_{PZH}	70	135	ns	note 5
	15		50	100	ns	
	5		170	340	ns	
LOW	10	t_{PZL}	70	140	ns	note 5
	15		50	100	ns	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.	
Distortion, sine-wave response	5		0,25	%	
	10		0,04	%	note 6
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	
	10		1	MHz	note 7
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	
	10		50	mV	note 8
	15		–	mV	
OFF-state feed-through	5		–	MHz	
	10		1	MHz	note 9
	15		–	MHz	
ON-state frequency response	5		13	MHz	
	10		40	MHz	note 10
	15		70	MHz	

Notes

1. V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
2. V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.
3. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; V_{is} = V_{DD} (square-wave); see Fig.7.
4. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{SS}; A_n = V_{DD} (square-wave); V_{is} = V_{DD} and R_L to V_{SS} for t_{PLH}; V_{is} = V_{SS} and R_L to V_{DD} for t_{PHL}; see Fig.7.
5. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ = V_{DD} (square-wave);
   V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Fig.7.
6. R_L = 10 kΩ; C_L = 15 pF; channel ON; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig.8.
7. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});

   $$20\ \log\frac{V_{os}}{V_{is}} = -50\ \text{dB; see Fig.9.}$$

8. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; $\overline{E}$ or A_n = V_{DD} (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig.7.
9. R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});

   $$20\ \log\frac{V_{os}}{V_{is}} = -50\ \text{dB; see Fig.8.}$$

10. R_L = 1 kΩ; C_L = 5 pF; channel ON; V_{is} = ½ $V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});

   $$20\ \log\frac{V_{os}}{V_{is}} = -3\ \text{dB; see Fig.8.}$$

16-channel analogue multiplexer/demultiplexer

HEF4067B
MSI

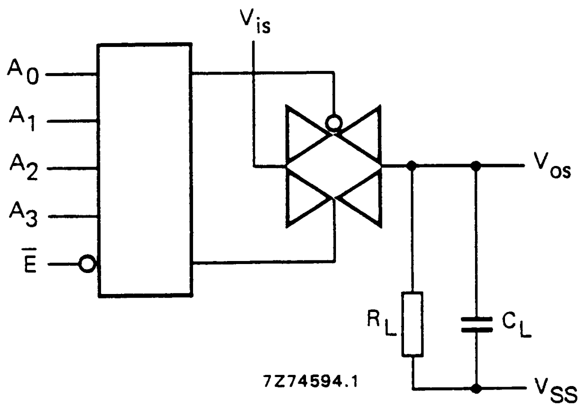


Fig.7

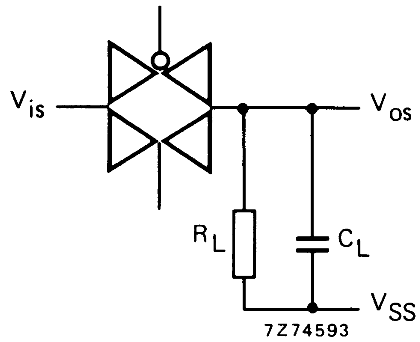


Fig.8

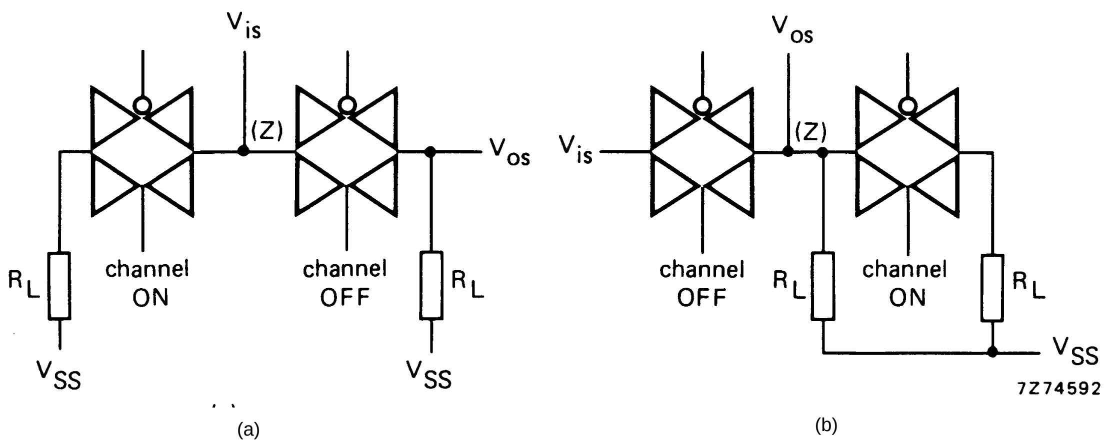


Fig.9

APPLICATION INFORMATION

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.