DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT157
Quad 2-input multiplexer

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Quad 2-input multiplexer 74HC/HCT157

FEATURES

- Non-inverting data path
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT157 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT157 are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions.

Moving the data from two groups of registers to four common output buses is a common use of the “157”. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The “157” is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The logic equations are:

$1Y = \overline{E}.(1I_1.S + 1I_0.\overline{S})$

$2Y = \overline{E}.(2I_1.S + 2I_0.\overline{S})$

$3Y = \overline{E}.(3I_1.S + 3I_0.\overline{S})$

$4Y = \overline{E}.(4I_1.S + 4I_0.\overline{S})$

The “157” is identical to the “158” but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	nI_0, nI_1 to nY		11	13	ns
	$\overline{E}$ to nY		11	12	ns
	S to nY		12	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	70	70	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from source 1
4, 7, 9, 12	1Y to 4Y	multiplexer outputs
8	GND	ground (0 V)
15	$\overline{E}$	enable input (active LOW)
16	V_{CC}	positive supply voltage

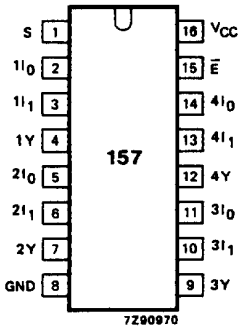


Fig.1 Pin configuration.

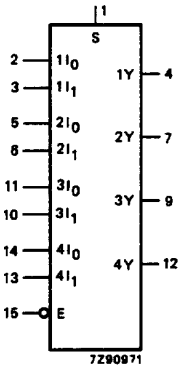


Fig.2 Logic symbol.

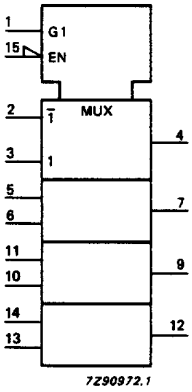


Fig.3 IEC logic symbol.

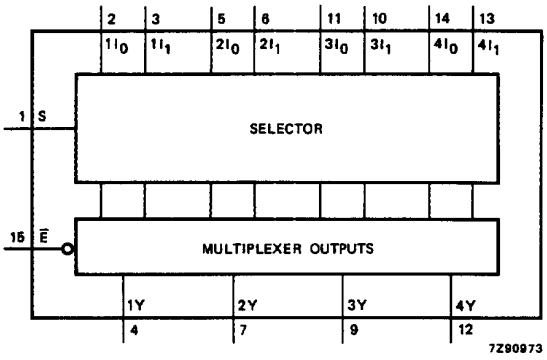


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS				OUTPUT
$\bar{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care

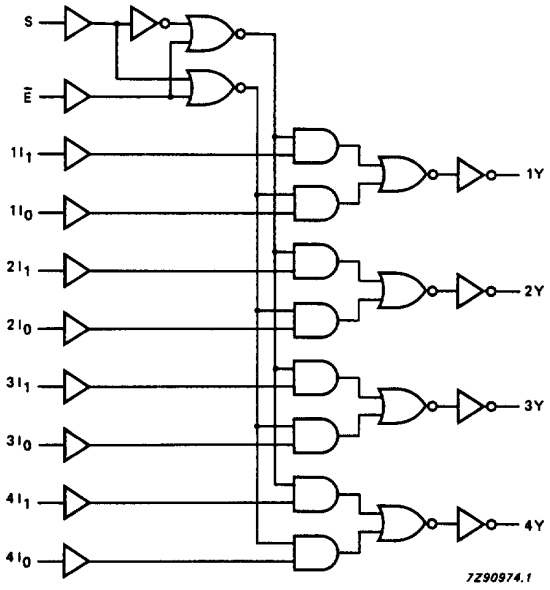


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		36 13 10	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to nY		39 14 11	115 23 20		145 29 25		175 35 30	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6 and Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

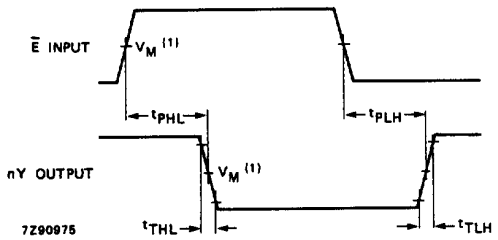
INPUT	UNIT LOAD COEFFICIENT
nI_0	1.00
nI_1	1.00
$\overline{E}$	0.60
S	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

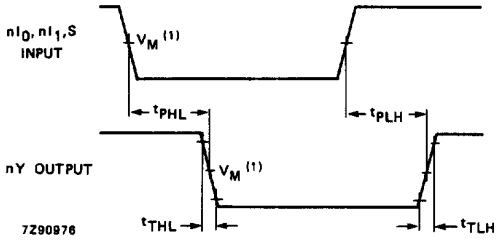
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		16	27		34		41	ns	4.5	Fig.7
t_{PHL}/ t_{PLH}	propagation delay $\overline{E}$ to nY		15	26		33		39	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay S to nY		22	37		46		56	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6 and Fig.7

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the enable input ($\overline{E}$) to output (nY) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the data inputs (nI_n) and common data select input (S) to output (nY) propagation delays.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.