# QUAD BUFFER/LINE DRIVER; 3-STATE

#### **FEATURES**

- Output capability: bus driver
- I<sub>CC</sub> category: MSI

#### **GENERAL DESCRIPTION**

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs,

SYMBOL	PARAMETER	CONDITIONS	TYF	418117	
	PARAMETER	CONDITIONS	HC	нст	UNIT
tPHL/ tPLH	propagation delay nA to nY	C <sub>L</sub> = 15 pF V <sub>CC</sub> = 5 V	9	11	ns
CI	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	notes 1 and 2	23	24	pF

$$GND = 0 V; T_{amb} = 25 \, ^{\circ}C; t_r = t_f = 6 \, \text{ns}$$

#### Notes

1. CPD is used to determine the dynamic power dissipation (PD in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_0)$$
 where:

f<sub>i</sub> = input frequency in MHz f<sub>o</sub> = output frequency in MHz CL = output load capacitance in pF

VCC = supply voltage in V

 $\Sigma (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

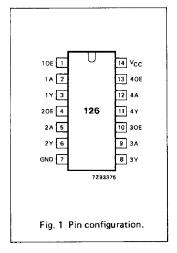
# **PACKAGE OUTLINES**

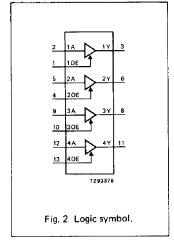
14-lead DIL; plastic (SOT27)

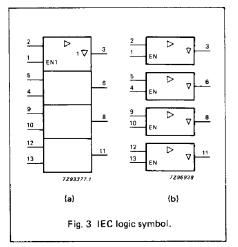
14-lead mini pack; plastic (SO14; SOT108A)

#### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	10E to 40E	output enable inputs (active HIGH)
2, 5, 9, 12	1A to 4A	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	vcc	positive supply voltage

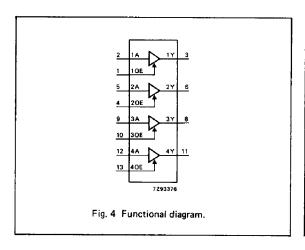


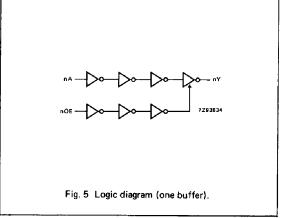




December 1990

# 74HC/HCT126 MSI





# **FUNCTION TABLE**

INPL	JTS	OUTPUT				
nOE	nA	nY				
н	L	L.				
H	H	н				
L	Х	Z				

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

January 1986

# DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

ICC category: MSI

#### **AC CHARACTERISTICS FOR 74HC**

GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ 

SYMBOL PAI		T <sub>amb</sub> (°C)							LIANT	TEST CONDITIONS		
		74HC								WAVEFORMS		
	PARAMETER	+25		-40 to +85		-40 to +125		UNIT	V <sub>CC</sub>	WAVEFORMS		
		min.	typ.	max.	min.	max.	min.	max.			I	
tPHL/ tPLH	propagation delay nA to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 6	
tPZH/	3-state output enable time nOE to nY	-	41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7	
tPHZ/ tPLZ	3-state output disable time nOE to nY		41 15 12	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 7	
<sup>t</sup> THL <sup>/</sup> <sup>t</sup> TLH	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6	

# 74HC/HCT126 MSI

# DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I<sub>CC</sub> category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

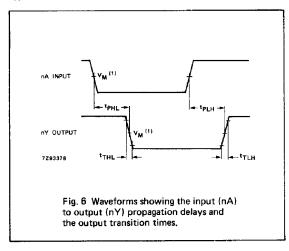
INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

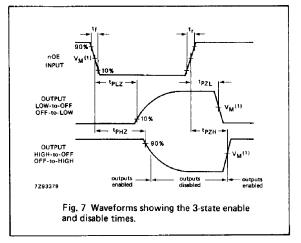
### **AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL PARAMETER		T <sub>amb</sub> (°C)								TEST CONDITIONS		
	PARAMETER	74HCT						,,				
	TANAMETER	+25		-40 to +85		-40 to +125		UNIT	V <sub>CC</sub>	WAVEFORMS		
		min,	typ.	max.	min.	max.	min.	max.				
<sup>t</sup> PHL/ <sup>t</sup> PLH	propagation delay nA to nY		14	24		30		36	ns	4.5	Fig. 6	
<sup>t</sup> PZH/ <sup>t</sup> PZL	3-state output enable time nOE to nY		13	25		31		38	ns	4.5	Fig. 7	
t <sub>PHZ</sub> / tPLZ	3-state output disable time nOE to nY		18	28		35		42	ns	4.5	Fig. 7	
<sup>t</sup> THL/ <sup>t</sup> TLH	output transition time	•	5	12		15		18	ns	4.5	Fig. 6	

#### **AC WAVEFORMS**





# Note to AC waveforms

(1) HC :  $V_M = 50\%$ ;  $V_1 = GND$  to  $V_{CC}$ . HCT:  $V_M = 1.3 \, V$ ;  $V_1 = GND$  to  $3 \, V$ .