

# DS26C31T/DS26C31M

## CMOS Quad TRI-STATE® Differential Line Driver

### General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

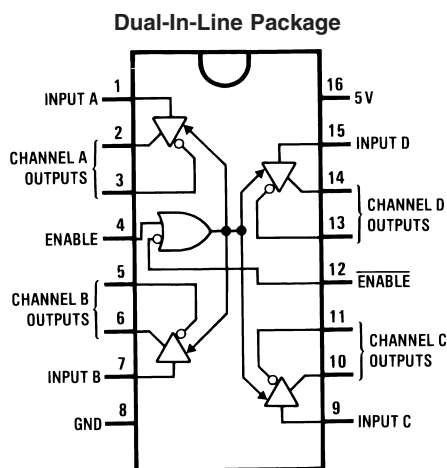
The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to  $V_{CC}$  and ground.

### Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when  $V_{CC} = 0V$
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

### Connection Diagrams

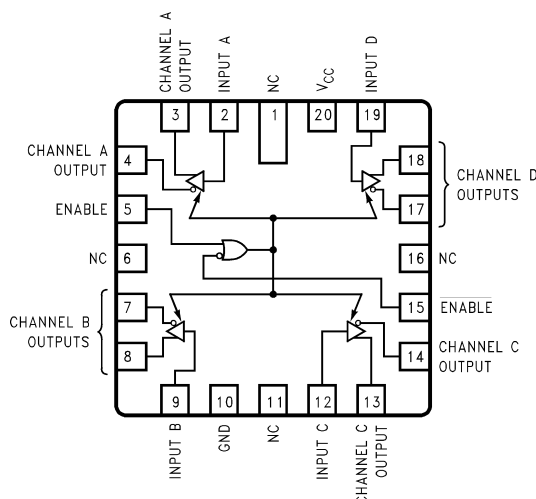


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Top View

Order Number DS26C31TM or DS26C31TN  
See NS Package Number M16A or N16E  
For Complete Military Product Specifications,  
refer to the appropriate SMD or MDS.  
Order Number DS26C31ME/883, DS26C31MJ/883  
or DS26C31MW/883  
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



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### Truth Table

ENABLE	ENABLE	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state  
X = Irrelevant  
H = High logic state  
Z = TRI-STATE (high impedance)

**Absolute Maximum Ratings** (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to 7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5V to $V_{CC}$ +1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to 7V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 150$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 150$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Max. Power Dissipation ( $P_D$ ) @25°C (Note 3)	
Ceramic "J" Pkg.	2419 mW
Plastic "N" Pkg.	1736 mW

SOIC "M" Pkg.	1226 mW
Ceramic "W" Pkg.	1182 mW
Ceramic "E" Pkg.	2134 mW

Lead Temperature ( $T_L$ )

(Soldering, 4 sec.) 260°C

This device does not meet 2000V ESD Rating. (Note 13)

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.50	5.50	V
DC Input or Output Voltage ( $V_{IN}$ , $V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )			
DS26C31T	-40	+85	°C
DS26C31M	-55	+125	°C
Input Rise or Fall Times ( $t_r$ , $t_f$ )		500	ns

**DC Electrical Characteristics** $V_{CC} = 5V \pm 10\%$  (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IH}$	High Level Input Voltage		2.0			V
$V_{IL}$	Low Level Input Voltage				0.8	V
$V_{OH}$	High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = -20$ mA	2.5	3.4		V
$V_{OL}$	Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = 20$ mA		0.3	0.5	V
$V_T$	Differential Output Voltage	$R_L = 100\Omega$ (Note 5)	2.0	3.1		V
$ V_T  -  \overline{V_T} $	Difference In Differential Output	$R_L = 100\Omega$ (Note 5)			0.4	V
$V_{OS}$	Common Mode Output Voltage	$R_L = 100\Omega$ (Note 5)		1.8	3.0	V
$ V_{OS} - \overline{V_{OS}} $	Difference In Common Mode Output	$R_L = 100\Omega$ (Note 5)			0.4	V
$I_{IN}$	Input Current	$V_{IN} = V_{CC}$ , GND, $V_{IH}$ , or $V_{IL}$			$\pm 1.0$	$\mu A$
$I_{CC}$	Quiescent Supply Current (Note 6)	DS26C31T	$V_{IN} = V_{CC}$ or GND	200	500	$\mu A$
		$I_{OUT} = 0$ $\mu A$		0.8	2.0	mA
		DS26C31M	$V_{IN} = V_{CC}$ or GND	200	500	$\mu A$
		$I_{OUT} = 0$ $\mu A$		0.8	2.1	mA
$I_{OZ}$	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $\overline{ENABLE} = V_{IL}$ $ENABLE = V_{IH}$		$\pm 0.5$	$\pm 5.0$	$\mu A$
$I_{SC}$	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND (Notes 5, 7)	-30		-150	mA
$I_{OFF}$	Output Leakage Current Power Off (Note 5)	DS26C31T	$V_{OUT} = 6V$		100	$\mu A$
		$V_{CC} = 0V$	$V_{OUT} = -0.25V$		-100	$\mu A$
		DS26C31M	$V_{OUT} = 6V$		100	$\mu A$
		$V_{CC} = 0V$	$V_{OUT} = 0V$ (Note 8)		-100	$\mu A$

## DC Electrical Characteristics (Continued)

**Note 1:** Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:** Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

**Note 3:** Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.

**Note 4:** Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

**Note 5:** See EIA Specification RS-422 for exact test conditions.

**Note 6:** Measured per input. All other inputs at  $V_{CC}$  or GND.

**Note 7:** This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

**Note 8:** The DS26C31M (–55°C to +125°C) is tested with  $V_{OUT}$  between +6V and 0V while RS-422A condition is +6V and –0.25V.

## Switching Characteristics

$V_{CC} = 5V \pm 10\%$ ,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns (Figures 1, 2, 3, 4) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
$t_{PLH}, t_{PHL}$	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	(Note 9)	S1 Open		0.5	2.0	3.0	ns
$t_{TLH}, t_{THL}$	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
$t_{PZH}$	Output Enable Time	S1 Closed		11	19	22	ns
$t_{PZL}$	Output Enable Time	S1 Closed		13	21	28	ns
$t_{PHZ}$	Output Disable Time (Note 10)	S1 Closed		5	9	12	ns
$t_{PLZ}$	Output Disable Time (Note 10)	S1 Closed		7	11	14	ns
$C_{PD}$	Power Dissipation Capacitance (Note 11)			50			pF
$C_{IN}$	Input Capacitance			6			pF

**Note 9:** Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

**Note 10:** Output disable time is the delay from ENABLE or  $\overline{ENABLE}$  being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

**Note 11:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## Comparison Table of Switching Characteristics into "LS-Type" Load

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns (Figures 2, 4, 5, 6) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
$t_{PLH}, t_{PHL}$	Propagation Delays Input to Output	$C_L = 30$ pF S1 Closed S2 Closed	6	8	10	15	ns
Skew	(Note 9)	$C_L = 30$ pF S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
$t_{THL}, t_{TLH}$	Differential Output Rise and Fall Times	$C_L = 30$ pF S1 Closed S2 Closed	4	6			ns
$t_{PLZ}$	Output Disable Time (Note 10)	$C_L = 10$ pF S1 Closed S2 Open	6	9	15	35	ns

## Comparison Table of Switching Characteristics into “LS-Type”

### Load (Continued)

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$  (Figures 2, 4, 5, 6) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
$t_{PHZ}$	Output Disable Time (Note 10)	$C_L = 10\text{ pF}$ S1 Open S2 Closed	4	7	15	25	ns
$t_{PZL}$	Output Enable Time	$C_L = 30\text{ pF}$ S1 Closed S2 Open	14	20	20	30	ns
$t_{PZH}$	Output Enable Time	$C_L = 30\text{ pF}$ S1 Open S2 Closed	11	17	20	30	ns

**Note 12:** This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.

**Note 13:** ESD Rating:

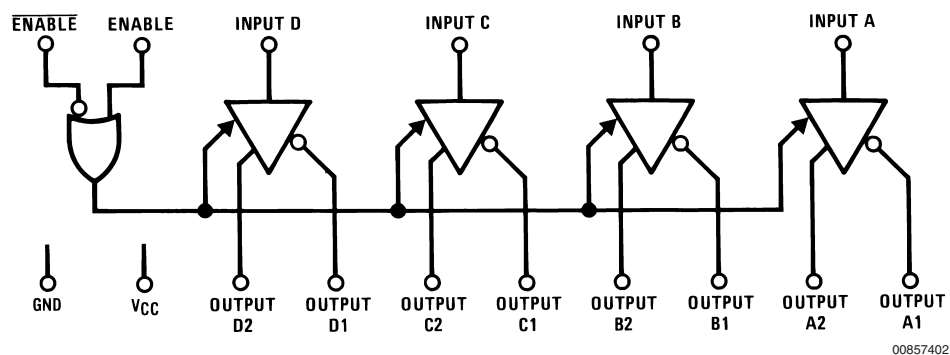
HBM (1.5 k $\Omega$ , 100 pF)

Inputs  $\geq 1500V$

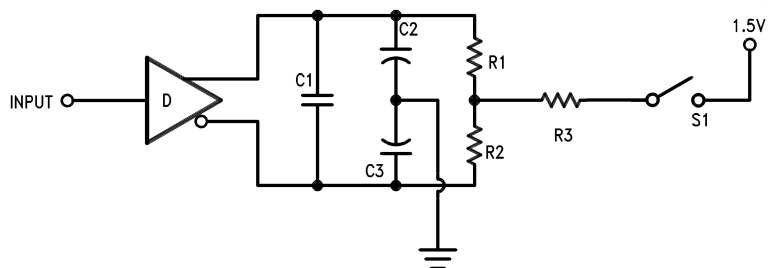
Outputs  $\geq 1000V$

EIAJ (0 $\Omega$ , 200 pF)  $\geq 350V$

### Logic Diagram



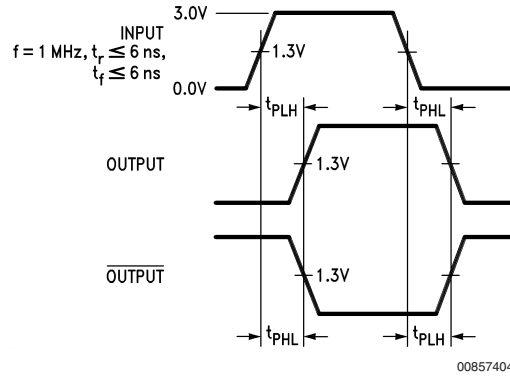
### AC Test Circuit and Switching Time Waveforms



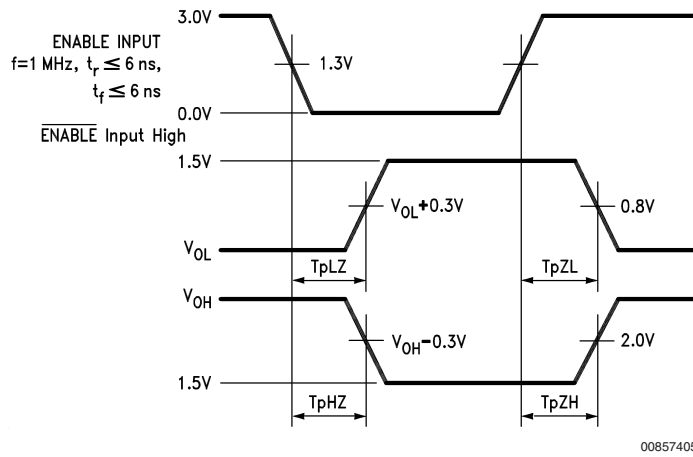
**Note:**  $C1 = C2 = C3 = 40\text{ pF}$  (Including Probe and Jig Capacitance);  $R1 = R2 = 50\Omega$ ,  $R3 = 500\Omega$ .

FIGURE 1. AC Test Circuit

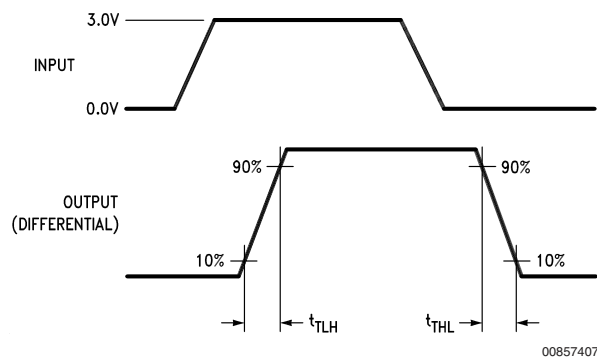
# AC Test Circuit and Switching Time Waveforms (Continued)



**FIGURE 2. Propagation Delays**



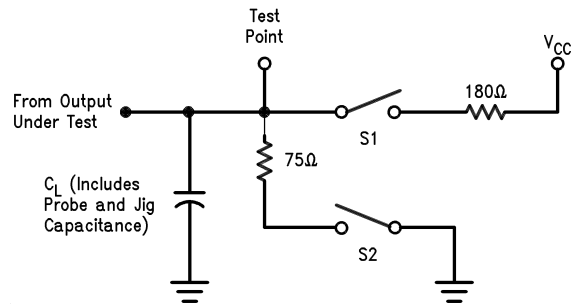
**FIGURE 3. Enable and Disable Times**



Input pulse;  $f = 1 \text{ MHz}$ , 50%;  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$

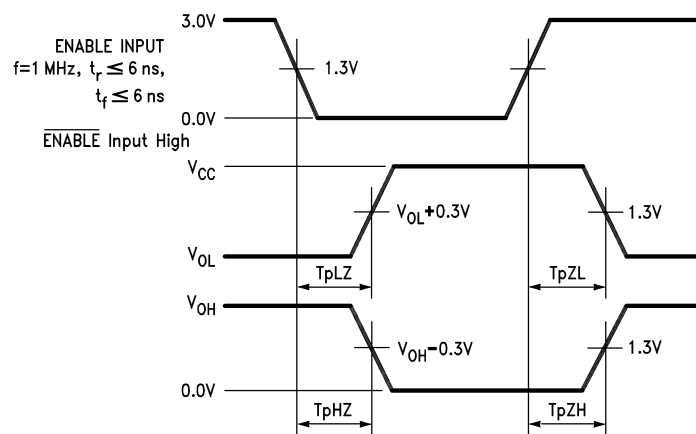
**FIGURE 4. Differential Rise and Fall Times**

## AC Test Circuit and Switching Time Waveforms (Continued)



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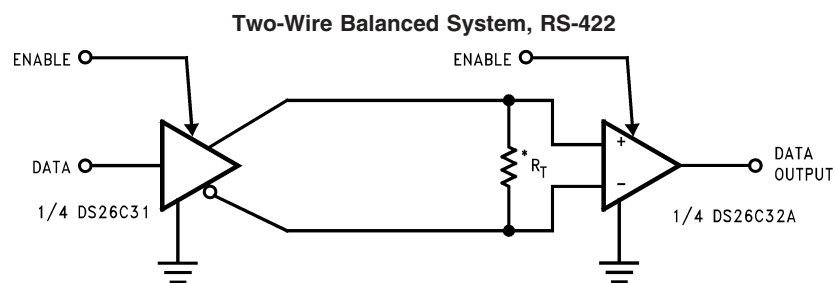
FIGURE 5. Load AC Test Circuit for "LS-Type" Load



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FIGURE 6. Enable and Disable Times for "LS-Type" Load

## Typical Applications

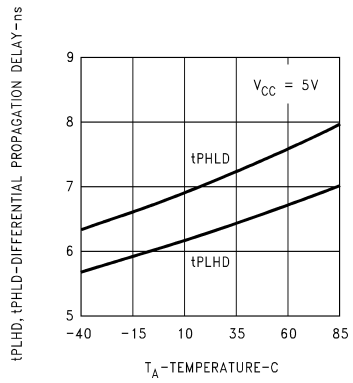


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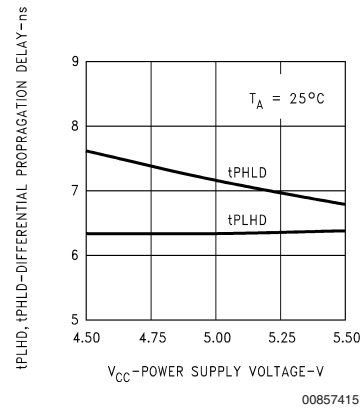
\* $R_T$  is optional although highly recommended to reduce reflection.

## Typical Performance Characteristics

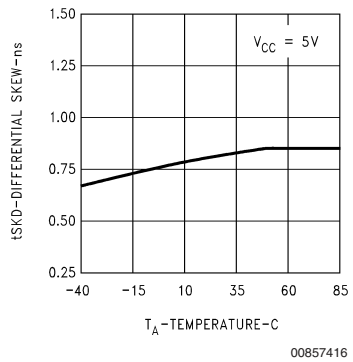
**Differential Propagation Delay vs Temperature**



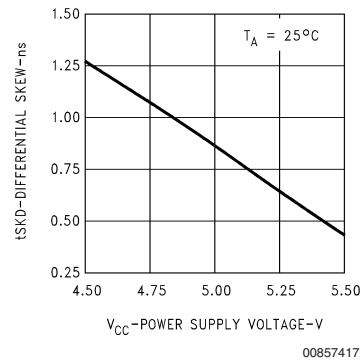
**Differential Propagation Delay vs Power Supply Voltage**



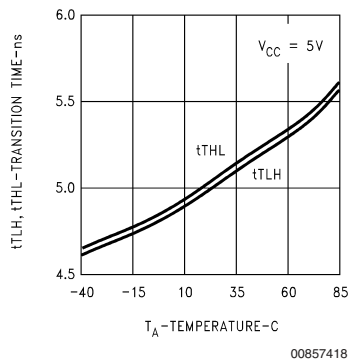
**Differential Skew vs Temperature**



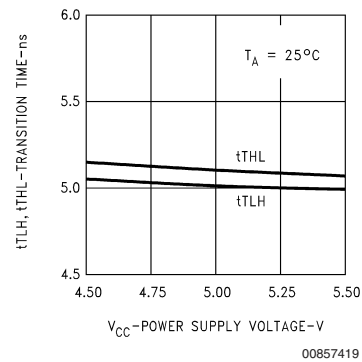
**Differential Skew vs Power Supply Voltage**



**Differential Transition Time vs Temperature**

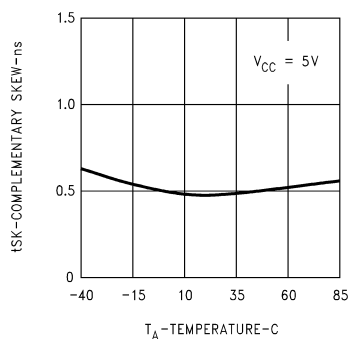


**Differential Transition Time vs Power Supply Voltage**



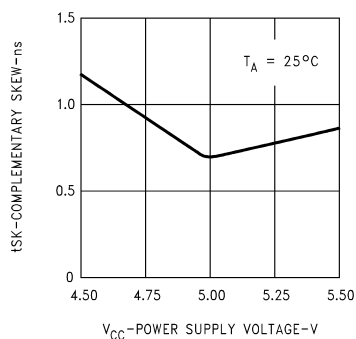
# Typical Performance Characteristics (Continued)

## Complementary Skew vs Temperature



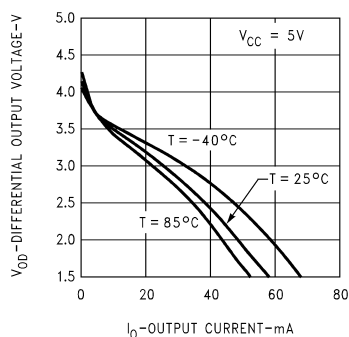
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## Complementary Skew vs Power Supply Voltage



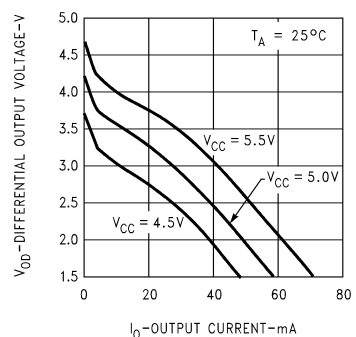
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## Differential Output Voltage vs Output Current



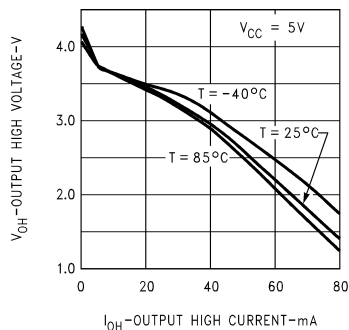
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## Differential Output Voltage vs Output Current



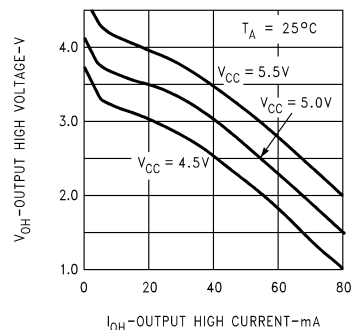
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## Output High Voltage vs Output High Current



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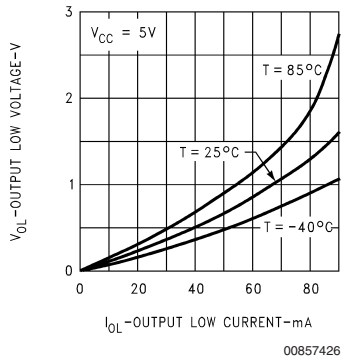
## Output High Voltage vs Output High Current



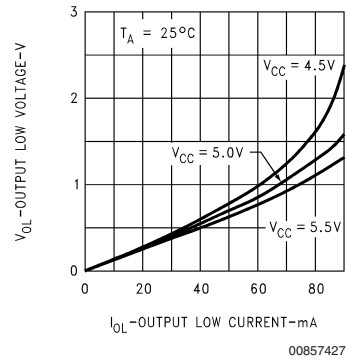
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# Typical Performance Characteristics (Continued)

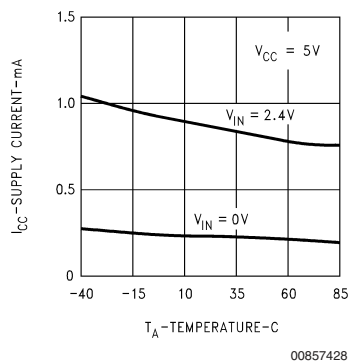
**Output Low Voltage vs  
Output Low Current**



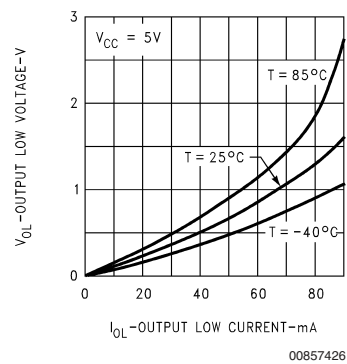
**Output Low Voltage vs  
Output Low Current**



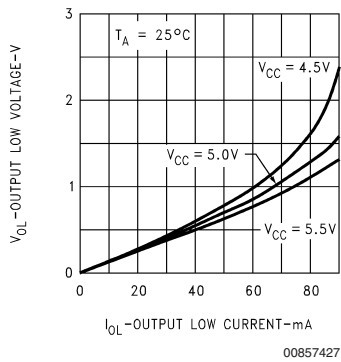
**Supply Current  
vs Temperature**



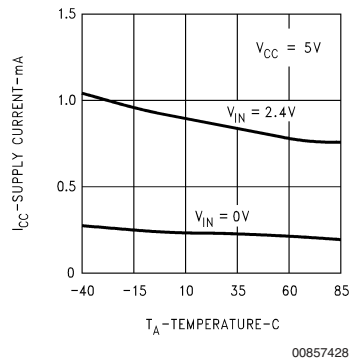
**Output Low Voltage vs  
Output Low Current**



**Output Low Voltage vs  
Output Low Current**

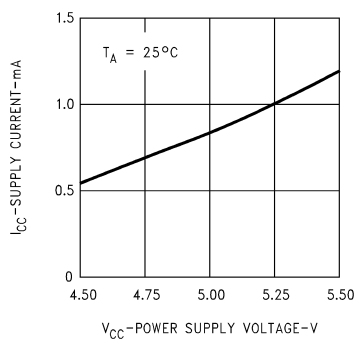


**Supply Current  
vs Temperature**



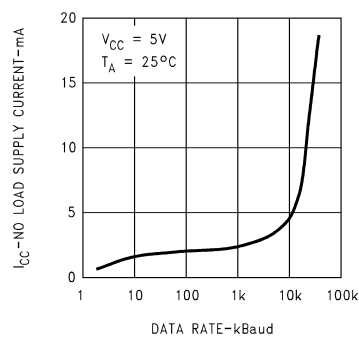
# Typical Performance Characteristics (Continued)

## Supply Current vs Power Supply Voltage



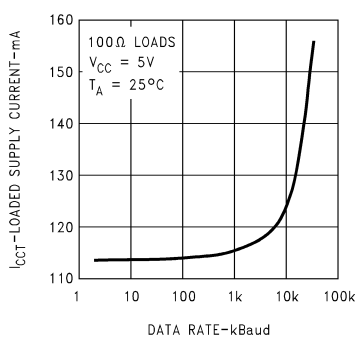
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## No Load Supply Current vs Data Rate



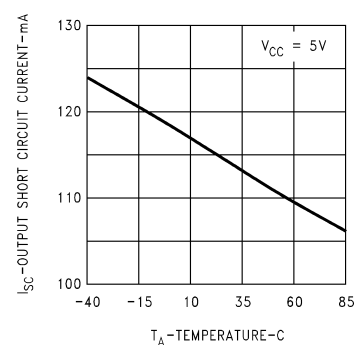
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## Loaded Supply Current vs Data Rate



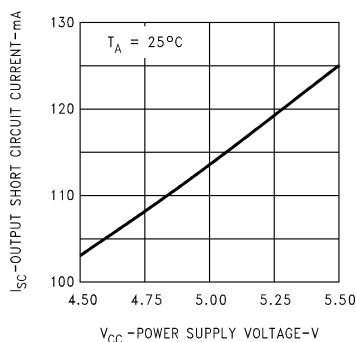
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## Output Short Circuit Current vs Temperature



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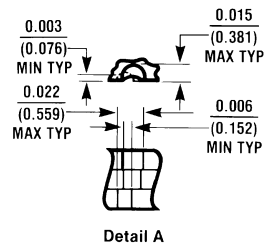
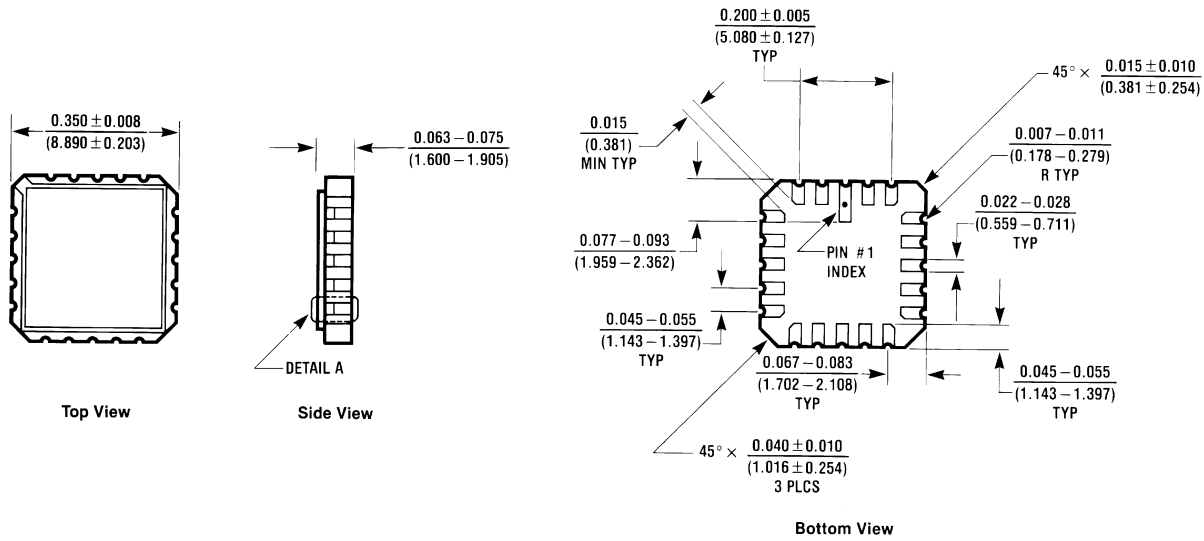
## Output Short Circuit Current vs Power Supply Voltage



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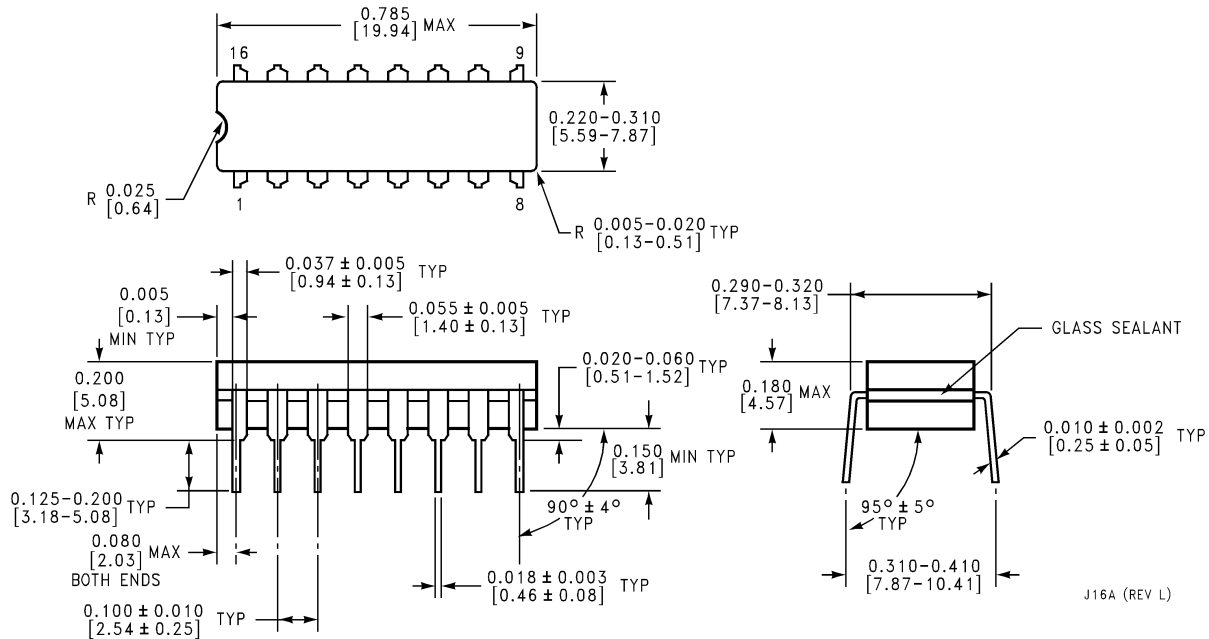
# Physical Dimensions inches (millimeters)

unless otherwise noted



E20A (REV D)

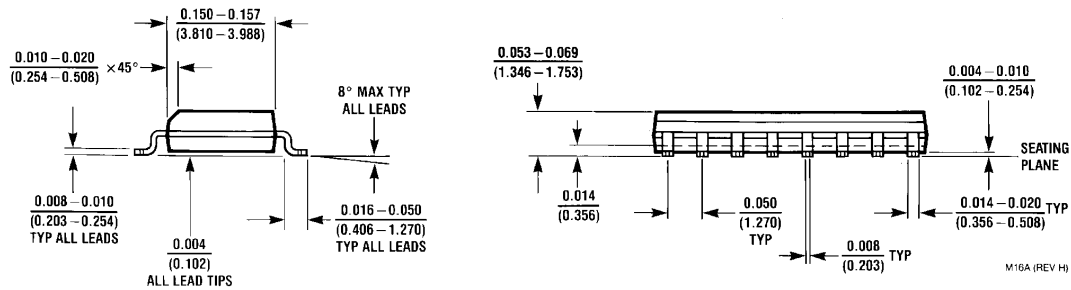
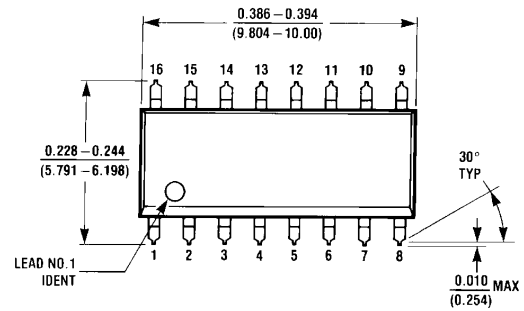
**20-Lead Ceramic Leadless Chip Carrier (E)**  
**Order Number DS26C31ME/883**  
**NS Package Number E20A**



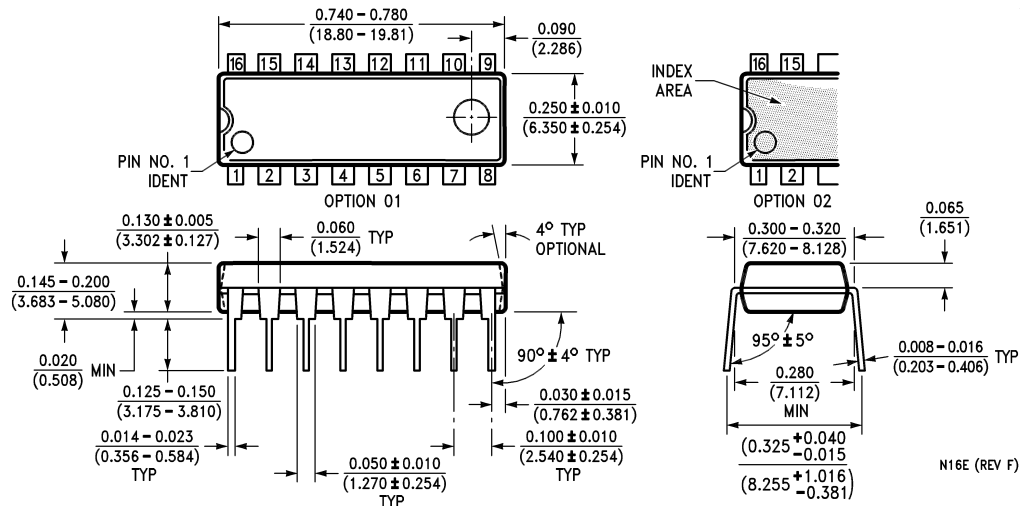
J16A (REV L)

**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DS26C31MJ/883**  
**NS Package Number J16A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

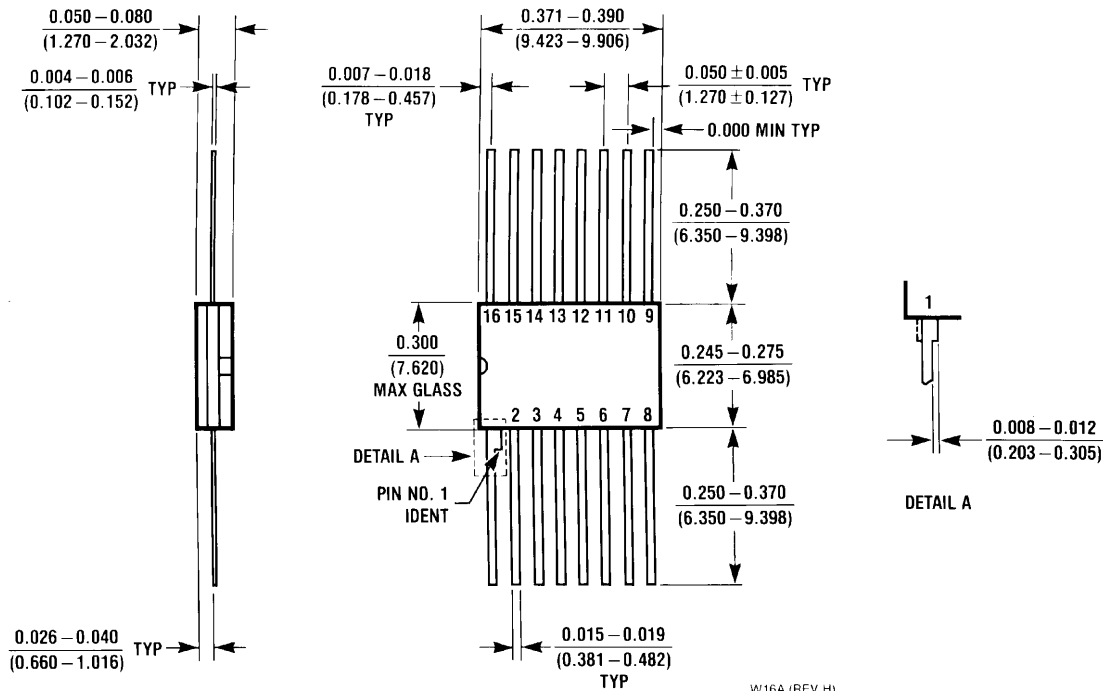


**Molded Package Small Outline (M)**  
**Order Number DS26C31TM**  
**NS Package Number M16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DS26C31TN**  
**NS Package Number N16E**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flatpak Package (W)**  
**Order Number DS26C31MW/883**  
**NS Package Number W16A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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 Email: [ap.support@nsc.com](mailto:ap.support@nsc.com)

**National Semiconductor**  
**Japan Customer Support Center**  
 Fax: 81-3-5639-7507  
 Email: [jpn.feedback@nsc.com](mailto:jpn.feedback@nsc.com)  
 Tel: 81-3-5639-7560