

IR2130D

3-PHASE DRIVER

Features

- Hermetic
- Floating channels designed for bootstrap operation
Fully operational to +400V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description

The IR2130D is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor.

Product Summary

V_{OFFSET}	400V max.
I_{O+/-}	200 mA / 420 mA
V_{OUT}	10 - 20V
t_{on/off} (typ.)	675 & 425 ns
Deadtime (typ.)	0.9 μs

An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output driver has a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SO}. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units	
V _{B1,2,3}	High Side Floating Supply Absolute Voltage	-0.3	V _{S1,2,3} + 20	V	
V _{S1,2,3}	High Side Floating Supply Offset Voltage	V _{SO} - 5	V _{SO} + 400		
V _{HO1,2,3}	High Side Output Voltage	V _{S1,2,3} - 0.3	V _{S1,2,3} + 0.3		
V _{CC}	Low Side Fixed Supply Voltage	-0.3	20		
V _{SO}	Low Side Driver Return	-5	V _{CC} + 0.3		
V _{LO1,2,3}	Low Side Output Voltage	V _{SO} - 0.3	V _{CC} + 0.3		
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	-0.3	V _{CC} + 0.3		
V _{FLT}	Fault Output Voltage	-0.3	V _{CC} + 0.3		
V _{CAO}	Operational Amplifier Output Voltage	-0.3	V _{CC} + 0.3		
V _{CA-}	Operational amplifier Inverting Input Voltage	-0.3	V _{CC} + 0.3		
dV _S /dt	Allowable Offset Supply Voltage Transient (Fig. 16)	—	50		V/nS
P _D	Package Power Dissipation @ TA < 25°C (Fig. 19)	—	1.5		W
R _{thJA}	Thermal Resistance, Junction to Ambient	—	70		°C/W
T _J	Junction Temperature	-55	125	°C	
T _S	Storage Temperature	-55	150		
T _L	Lead Temperature (Soldering, 10 seconds)	—	300		
	Weight	6.1 (typical)		g	

IR2130D

International
IR Rectifier

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to VS0. The VS offset rating is tested with all supplies biased at 15V differential.

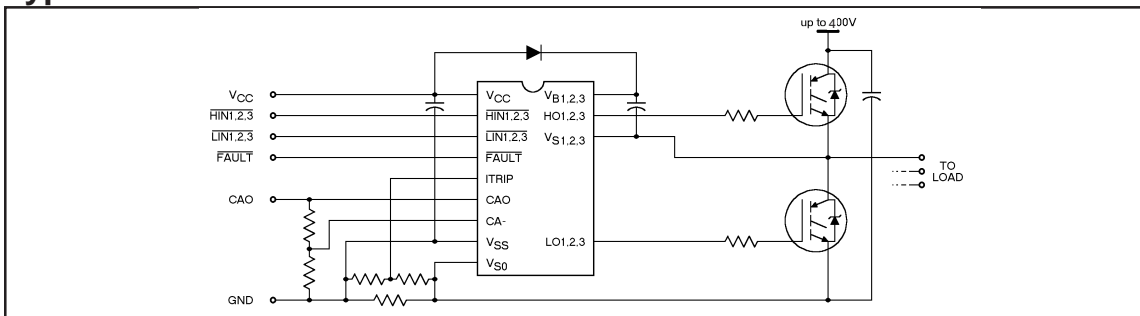
Symbol	Parameter	Min.	Max.	Units
V _{B1,2,3}	High Side Floating Supply Voltage	V _{S1,2,3} + 10	V _{S1,2,3} + 20	V
V _{S1,2,3}	High Side Floating Supply Offset Voltage	V _{SO} - 5	V _{SO} + 400	
V _{HO1,2,3}	High Side Output Voltage	V _{S1,2,3}	V _{B1,2,3}	
V _{CC}	Low Side Fixed Supply Voltage	10	20	
V _{SS}	Logic Ground	-5	5	
V _{LO1,2,3}	Low Side Output Voltage	0	V _{CC}	
V _{IN}	Logic Input Voltage (HIN, LIN & SD)	V _{SS}	V _{SS} + 5	
V _{FLT}	Fault Output Voltage	V _{SS}	V _{CC}	
V _{CAO}	Operational Amplifier Output Voltage	V _{SS}	5	
V _{CA-}	Operational Amplifier Inverting Input Voltage	V _{SS}	5	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{B1,2,3}) = 15V, V_{S0,1,2,3} = V_{SS}. C_L = 1000 pF unless otherwise specified.

Symbol	Parameter	T _j = 25°C			T _j = -55 to 125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
t _{on}	Turn-On Propagation Delay (all six channels)	500	675	850	—	850	ns	C _L = 1000pF V _{S1,2,3} = 0 to 400 V V _{IN} = 0 & 5 V
t _r	Turn-On Rise Time (all six channels)	—	80	125	—	175		
t _{off}	Turn-Off Propagation Delay (all six channels)	300	425	550	—	600		
t _f	Turn-Off Fall Time (all six channels)	—	35	55	—	85		
DT	Deadtime (LS Turn-off to HS Turn-on & HS Turn-off to LS Turn-on)	0.4	0.9	1.3	0.25	1.5	μs	C _L = 1000pF, V _{IN} = 0 & 5V
t _{trip}	ITRIP to Output Shutdown Prop. Delay	400	660	920	—	1100	ns	V _{IN} , V _{ITRIP} = 0 & 5V
t _{flt}	ITRIP to FAULT Indication Delay	335	590	845	—	1000		
t _{fltclr}	LIN1, 2, 3 To FAULT Clear Time	5.5	10	12.5	—	—	μs	
t _{flt,in}	Input Filter Time (all six inputs)	—	310	—	—	—	ns	V _{IN} = 0 & 5V
t _{bl}	ITRIP Blanking Time	—	400	—	—	—	ns	V _{ITRIP} = 1V
SR+	Amplifier Slew Rate (+)	4.4	6.2	—	2.7	—	V/μs	
SR-	Amplifier Slew Rate (-)	2.4	3.2	—	1.5	—	V/μs	

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS1}, 2, 3) = 15V, V_{SO1}, 2, 3 = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1, 2, 3 & LIN1, 2, 3. The V_O and I_O parameters are referenced to V_{SO1}, 2, 3.

Symbol	Parameter	T _j = 25°C			T _j =55-125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
I _{LK}	Offset Supply Leakage Currents	—	—	50	—	500	μA	V _B = V _S =400V
I _{QBS}	Quiescent V _{BS} Supply Current	—	15	30	—	45		V _{IN} = 0V or 5V
I _{QCC}	Quiescent V _{CC} Supply Current	—	3.0	4.0	—	6.0	mA	V _{IN} = 0V or 5V
I _{IN} ⁺	Logic "1" Input Bias Current(OUT= HI)	—	450	650	—	1050		V _{IN} = 0V
I _{IN} ⁻	Logic "0" Input Bias Current(OUT=LO)	—	225	400	—	—	μA	V _{IN} = 5V
I _{ITRIP} ⁺	"High" ITRIP Bias Current	—	75	150	—	—		ITRIP = 5V
I _{ITRIP} ⁻	"Low" ITRIP Bias Current	—	—	100	—	170	nA	ITRIP =0V
V _{IN.IH}	Logic "0" Input Voltage (OUT = LO)	—	—	—	2.2	—	V	
V _{IN.IL}	Logic "1" Input Voltage (OUT = HI)	—	—	—	—	0.8		
V _{IT,TH} ⁺	ITRIP Input Positive Going Threshold	400	490	580	350	580	mV	
V _{OS}	Amplifier Input Offset Voltage	—	—	30	—	—	mV	V _{SO} = CA- = 0.2V
R _{on,FLT}	FAULT- Low On Resistance	—	55	75	—	150	Ω	
I _{CA} ⁻	CA- Input Bias Current	—	0.5	4.0	—	4.0	nA	CA- = 2.5V
V _{CCUV} ⁺	V _{CC} Supply Undervoltage Positive Going Threshold	8.3	9.0	10.6	8.0	10.7	V	
V _{CCUV} ⁻	V _{CC} Supply Undervoltage Negative Going Threshold	8.0	8.7	10.5	7.7	10.5		
V _{BSUV} ⁺	V _{BS} Supply Undervoltage Positive Going Threshold	7.5	8.4	9.2	—	—	V	
V _{BSUV} ⁻	V _{BS} Supply Undervoltage Negative Going Threshold	7.1	8.0	8.8	—	—		
I _O ⁺	Output High Short Circuit Pulsed Current	200	250	—	—	—	mA	V _{OUT} = V _{IN-} = 0V PW ≤ 10μS
I _O ⁻	Output Low Short Circuit Pulsed Current	420	500	—	—	—		V _{OUT} =15, V _{IN-} =5V PW ≤ 10μS
V _{OH,Amp}	Amplifier High Level Output Voltage	5.0	5.2	5.4	4.9	5.6	V	CA- = 0V, V _{SO} =1V
V _{OL,Amp}	Amplifier Low Level Output Voltage	—	2.5	20	—	20	mV	CA- = 1V, V _{SO} =0V
I _{SRC,Amp}	Amplifier Output Source Current	2.3	4.0	—	1.5	—	mA	CA- = 0V, V _{SO} =1V, CA0=4V
I _{SNK,Amp}	Amplifier Output Sink Current	1.0	2.1	—	0.5	—		CA- = 1V, V _{SO} =0V, CA0=2V
CMRR	Amplifier Common Mode Rejection Ratio	60	80	—	—	—	dB	CA- =V _{SO} =0.1V & 5V
PSRR	Amplifier Power Supply Rejection Ratio	55	75	—	—	—		CA- = V _{SO} =0.2V V _{CC} = 10V & 20V
V _{OH}	High Level Output Voltage	—	—	100	—	100	mV	V _{IN-} = 0V, I _O = 0A
V _{OL}	Low Level Output Voltage	—	—	100	—	100		V _{IN-} = 5V, I _O = 0A

Static Electrical Characteristics Continued

V_{BIAS} (V_{CC} , $V_{BS1, 2, 3}$) = 15V, $V_{SO1, 2, 3}$ = V_{SS} unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1, 2, 3 & LIN1, 2, 3. The V_O and I_O parameters are referenced to $V_{SO1, 2, 3}$.

Symbol	Parameter	T _j = 25°C			T _j = 55 to 125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
$I_{O+, Amp}$	Amplifier Output High Short Circuit Circuit	—	4.5	6.5	—	8.0		CA- = 0V, V_{SO} = 5V V_{CAO} = 0V
$I_{O-, Amp}$	Amplifier Output High Short Circuit Circuit	—	3.2	5.2	—	7.0		CA- = 5V, V_{SO} = 0V V_{CAO} = 5V

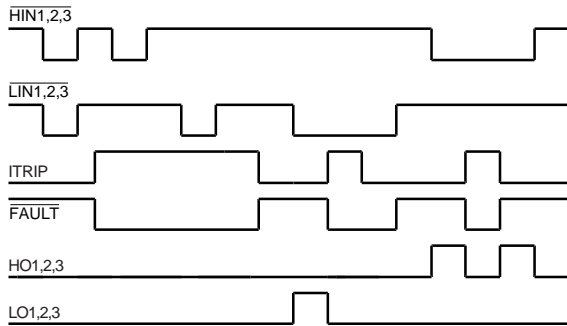


Figure 1. Input/Output Timing Diagram

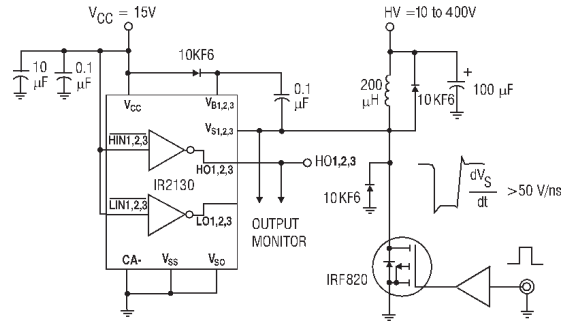


Figure 2. Floating Supply Voltage Transient Test Circuit

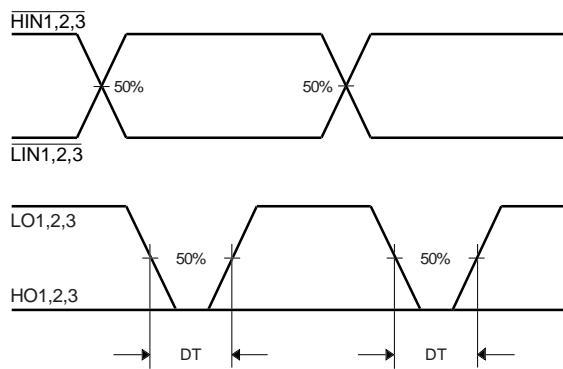


Figure 3. Deadtime Waveform Definitions

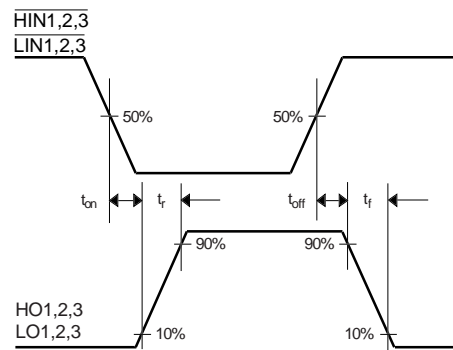


Figure 4. Input/Output Switching Time Waveform Definitions

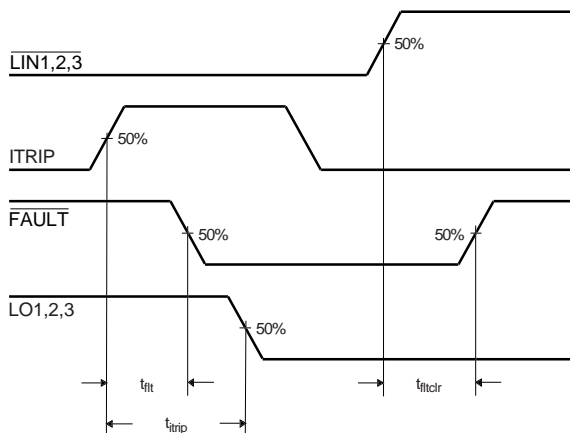


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

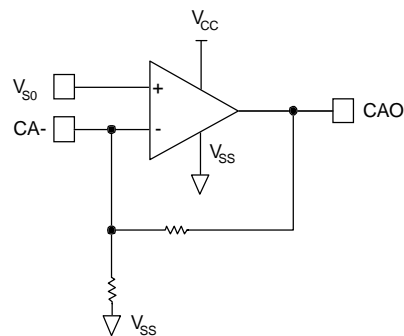


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

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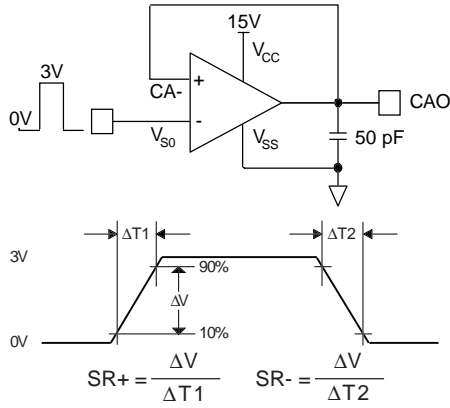


Figure 7. Operational Amplifier Slew Rate Measurement

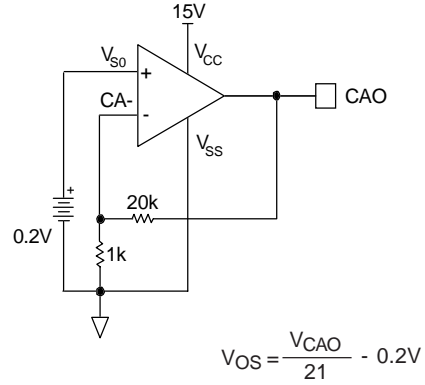


Figure 8. Operational Amplifier Input Offset Voltage Measurement

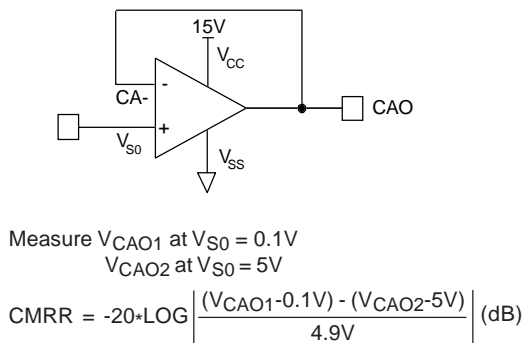


Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements

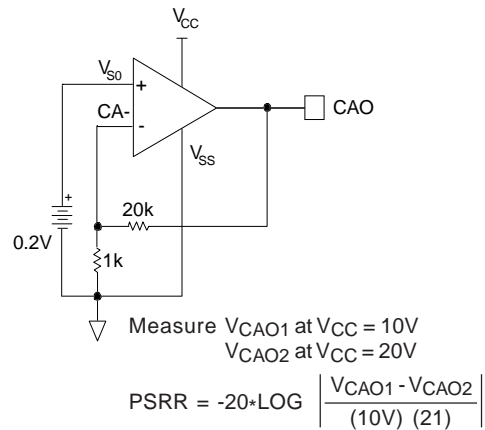


Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

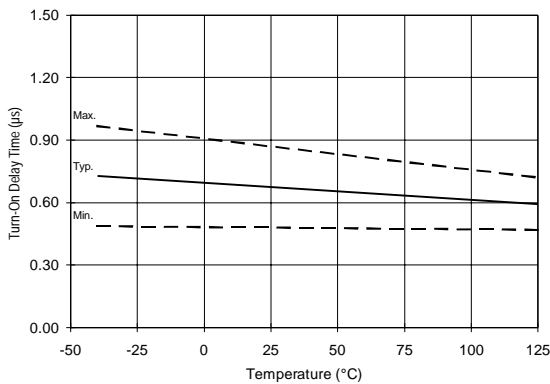


Figure 11A. Turn-On Time vs. Temperature

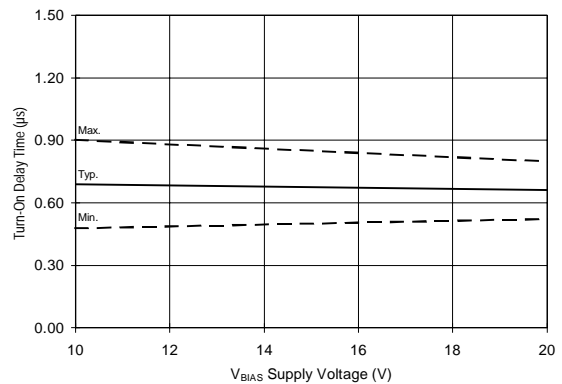


Figure 11B. Turn-On Time vs. Voltage

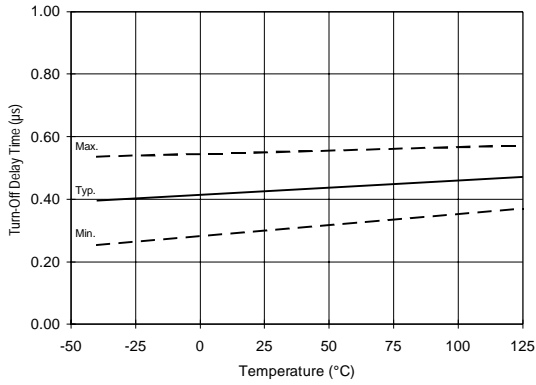


Figure 12A. Turn-Off Time vs. Temperature

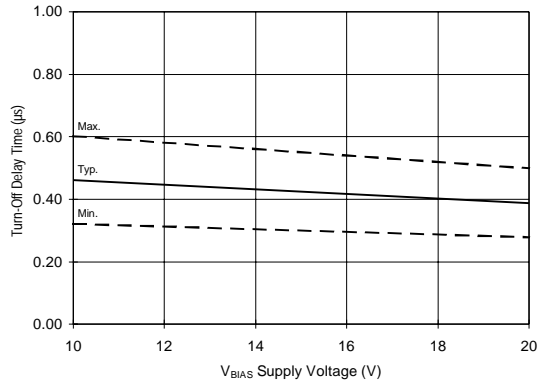


Figure 12B. Turn-Off Time vs. Voltage

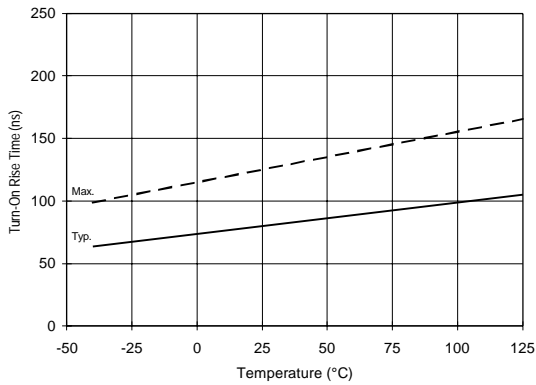


Figure 13A. Turn-On Rise Time vs. Temperature

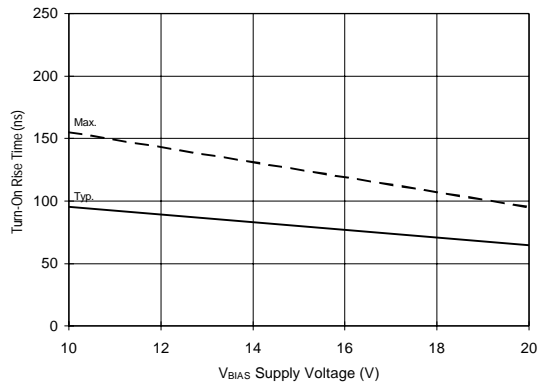


Figure 13B. Turn-On Rise Time vs. Voltage

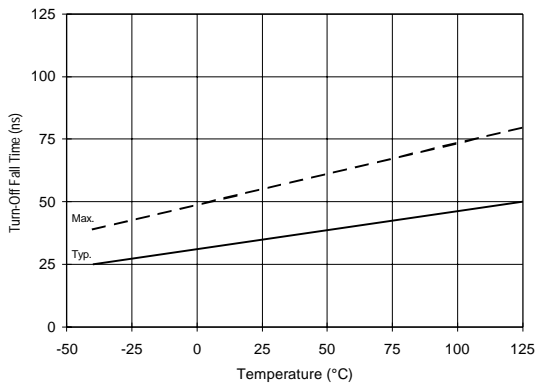


Figure 14A. Turn-Off Fall Time vs. Temperature

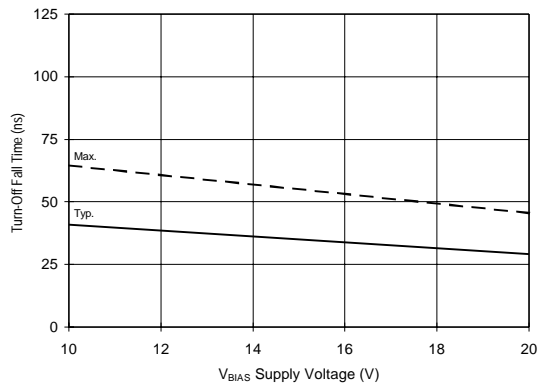


Figure 14B. Turn-Off Fall Time vs. Voltage

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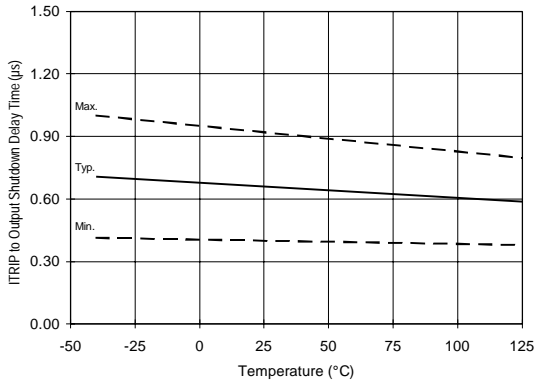


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

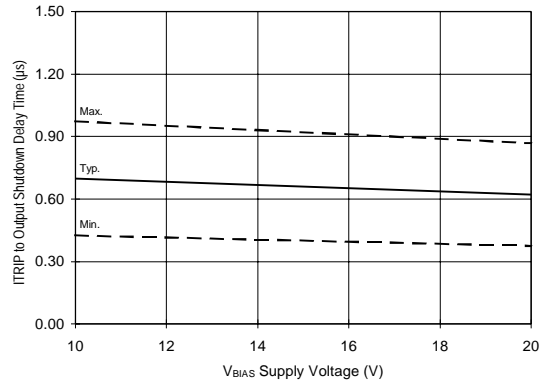


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

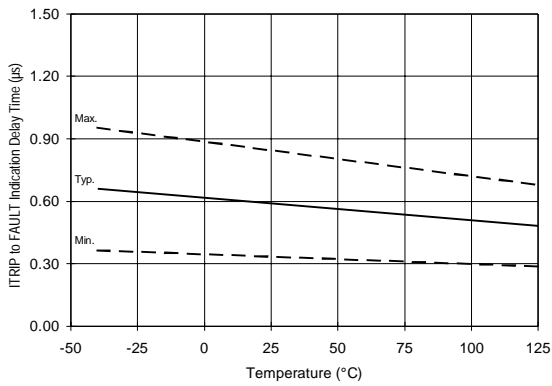


Figure 16A. ITRIP to **FAULT** Indication Time vs. Temperature

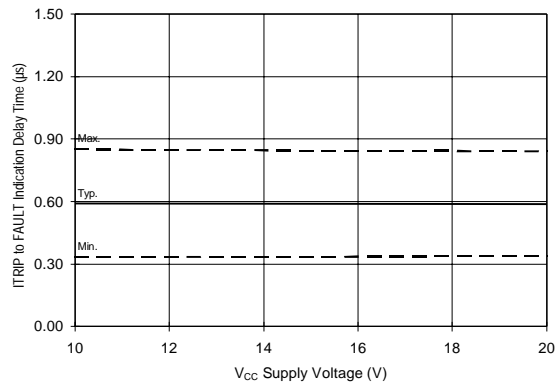


Figure 16B. ITRIP to **FAULT** Indication Time vs. Voltage

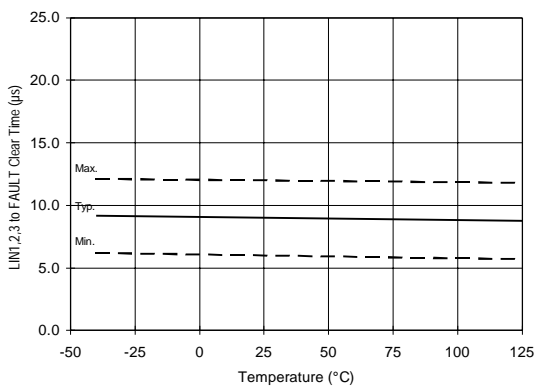


Figure 17A. **LIN1,2,3** to **FAULT** Clear Time vs. Temperature

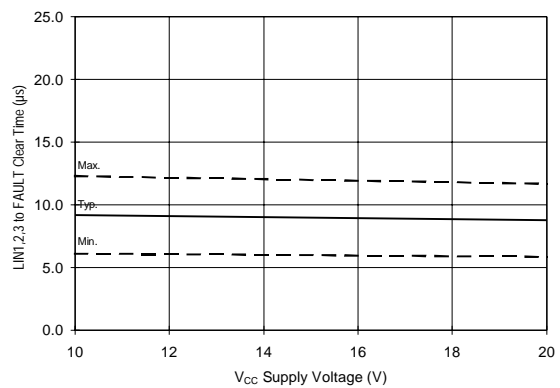


Figure 17B. **LIN1,2,3** to **FAULT** Clear Time vs. Voltage

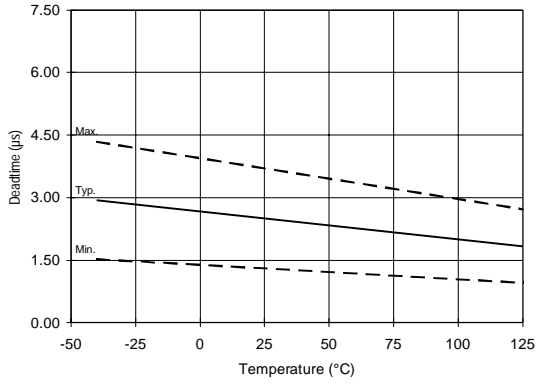


Figure 18A. Deadtime vs. Temperature

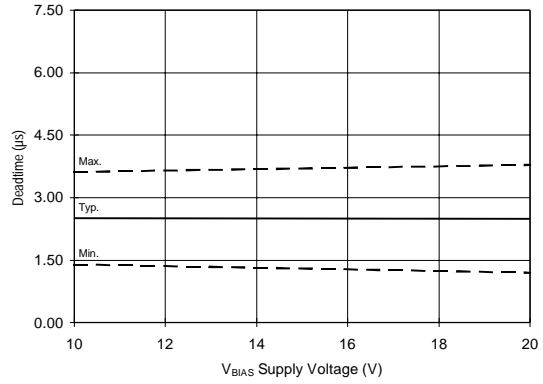


Figure 18B. Deadtime vs. Voltage

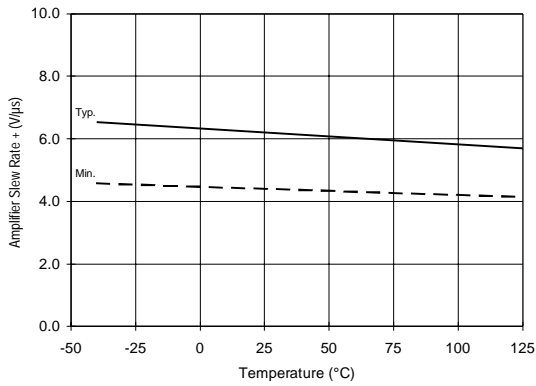


Figure 19A. Amplifier Slew Rate (+) vs. Temperature

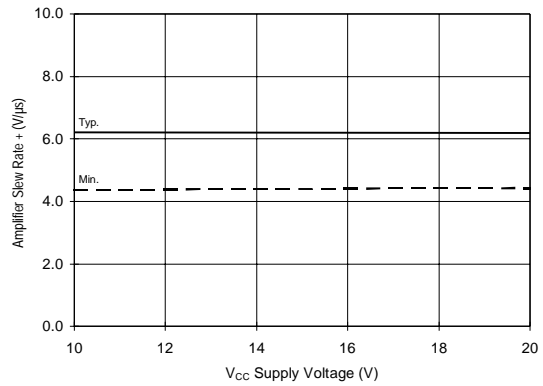


Figure 19B. Amplifier Slew Rate (+) vs. Voltage

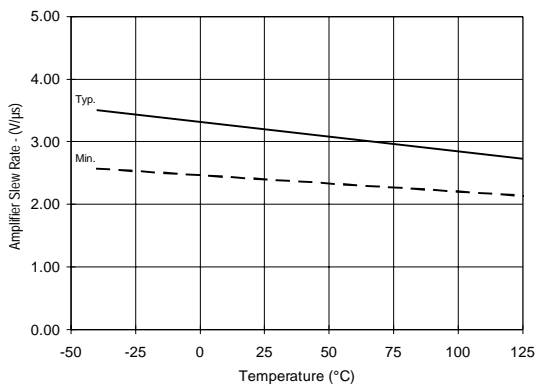


Figure 20A. Amplifier Slew Rate (-) vs. Temperature

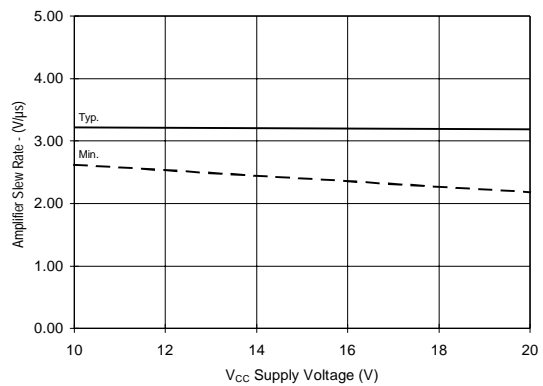


Figure 20B. Amplifier Slew Rate (-) vs. Voltage

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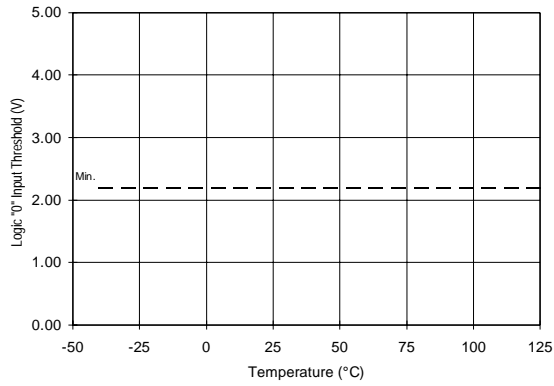


Figure 21A. Logic "0" Input Threshold vs. Temperature

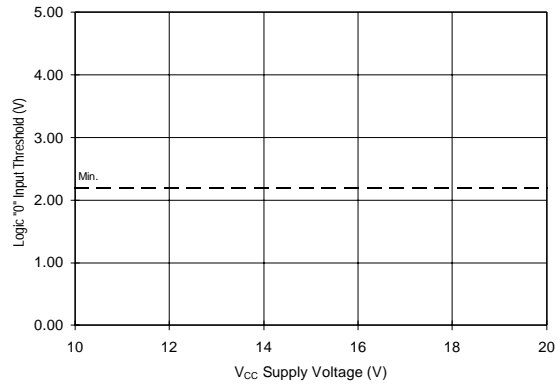


Figure 20B. Logic "0" Input Threshold vs. Voltage

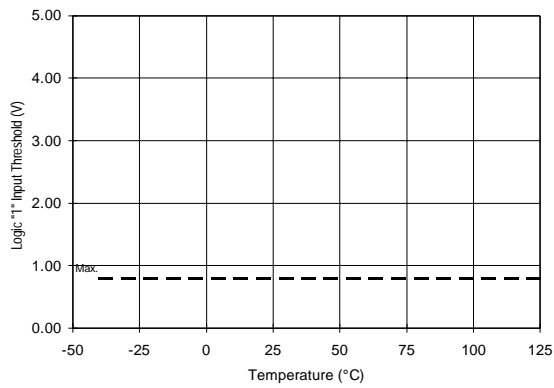


Figure 22A. Logic "1" Input Threshold vs. Temperature

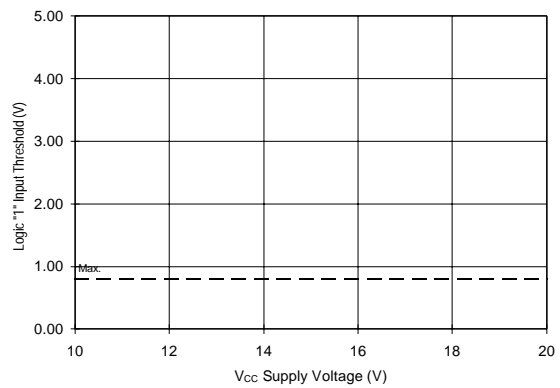


Figure 22B. Logic "1" Input Threshold vs. Voltage

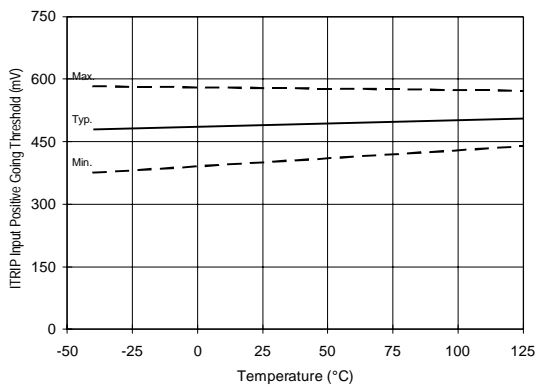


Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

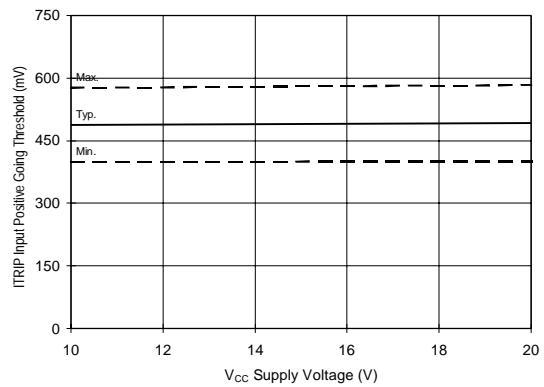


Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

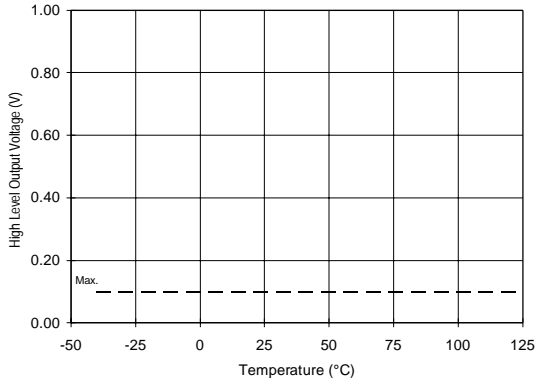


Figure 24A. High Level Output vs. Temperature

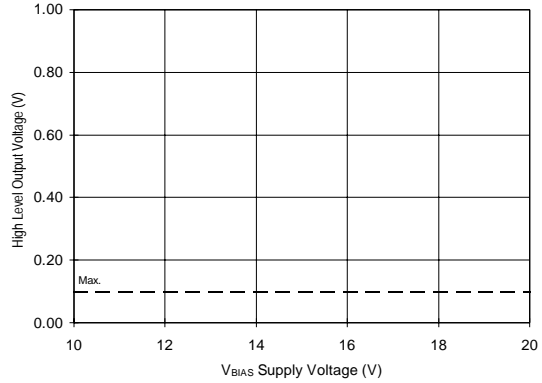


Figure 24B. High Level Output vs. Voltage

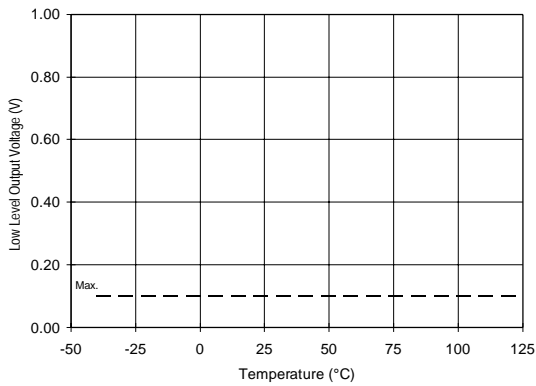


Figure 25A. Low Level Output vs. Temperature

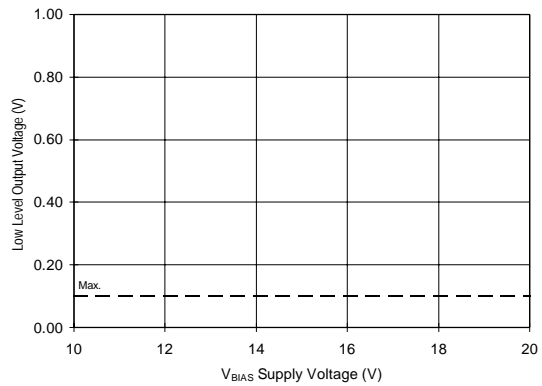


Figure 25B. Low Level Output vs. Voltage

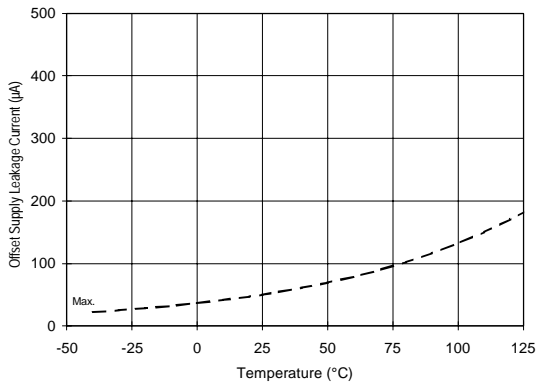


Figure 26A. Offset Supply Leakage Current vs. Temperature

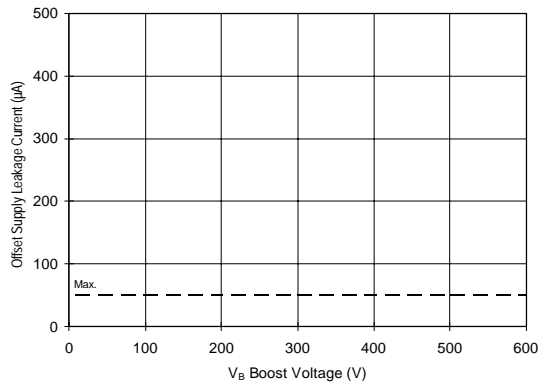


Figure 26B. Offset Supply Leakage Current vs. Voltage

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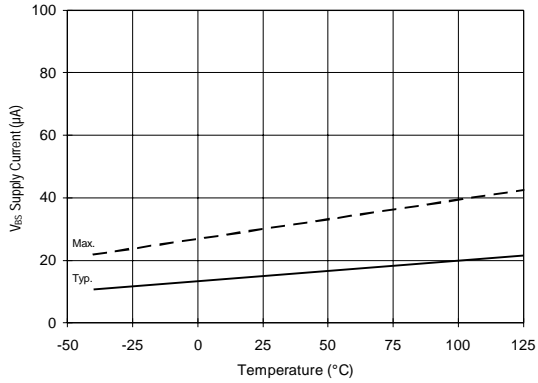


Figure 27A. V_{BS} Supply Current vs. Temperature

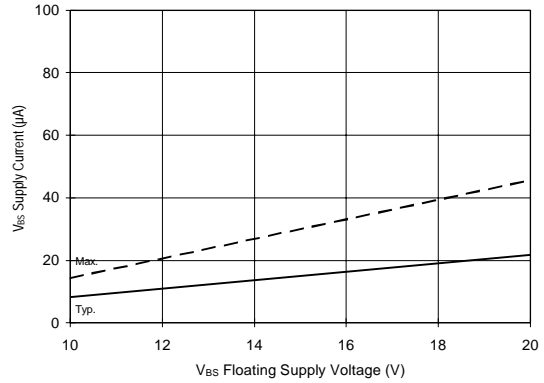


Figure 27B. V_{BS} Supply Current vs. Voltage

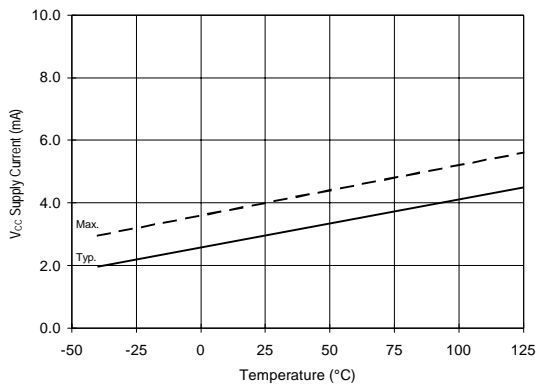


Figure 28A. V_{CC} Supply Current vs. Temperature

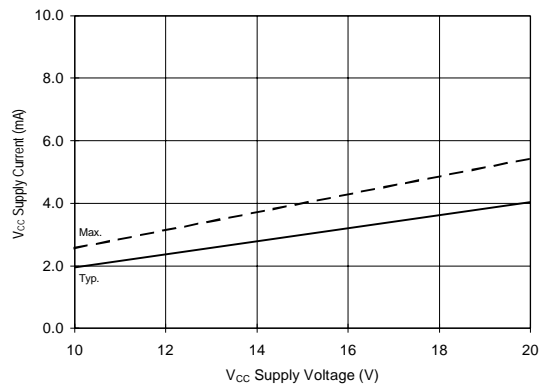


Figure 28B. V_{CC} Supply Current vs. Voltage

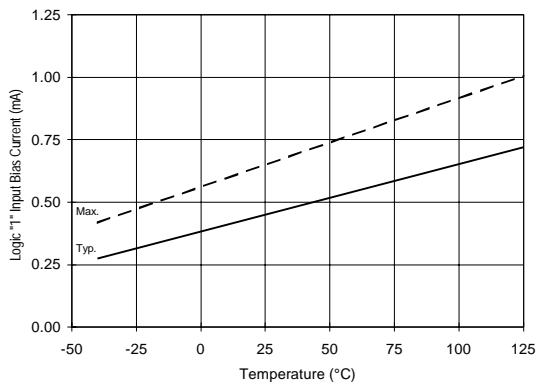


Figure 29A. Logic "1" Input Current vs. Temperature

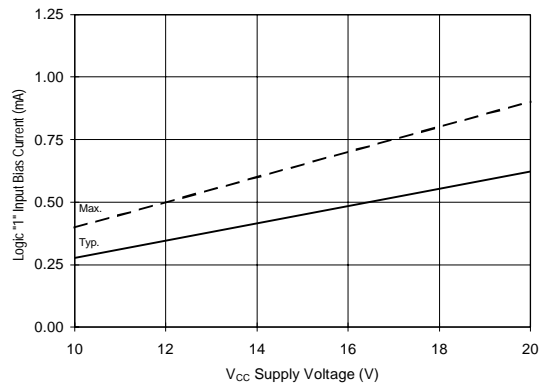


Figure 29B. Logic "1" Input Current vs. Voltage

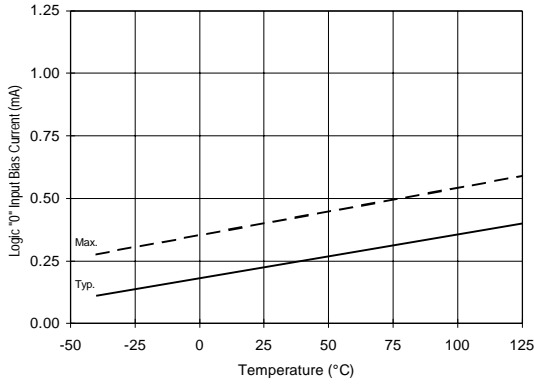


Figure 30A. Logic "0" Input Current vs. Temperature

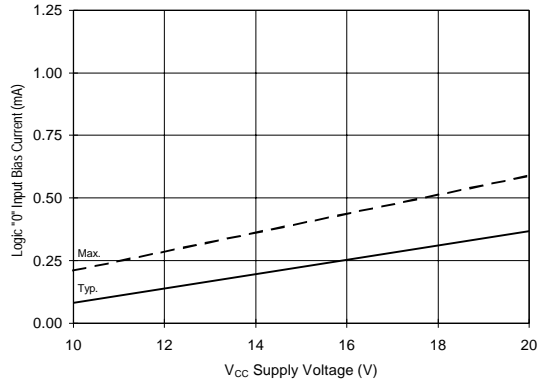


Figure 30B. Logic "0" Input Current vs. Voltage

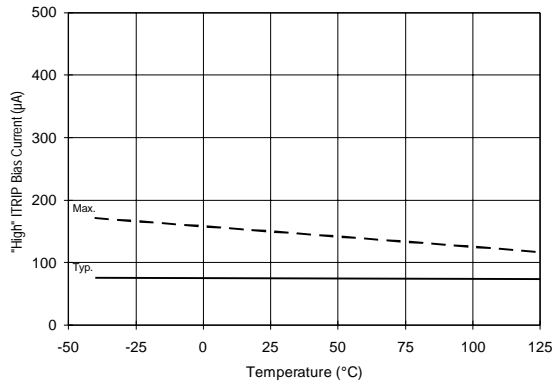


Figure 31A. "High" ITRIP Current vs. Temperature

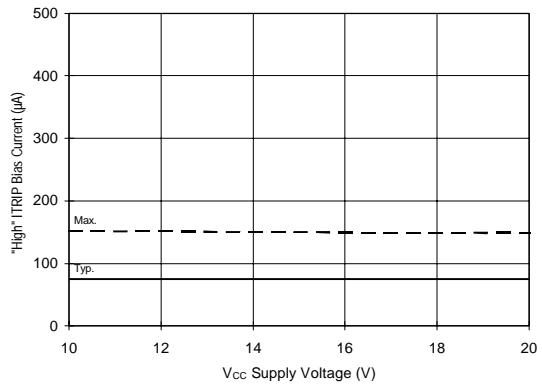


Figure 31B. "High" ITRIP Current vs. Voltage

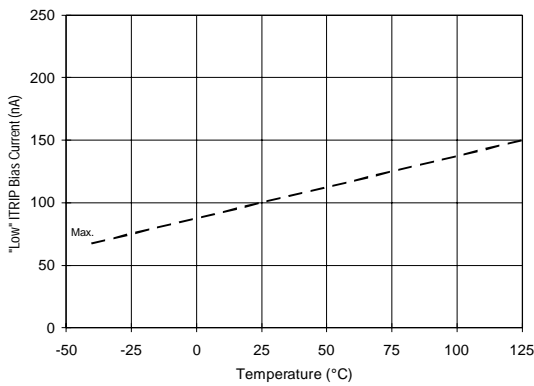


Figure 32A. "Low" ITRIP Current vs. Temperature

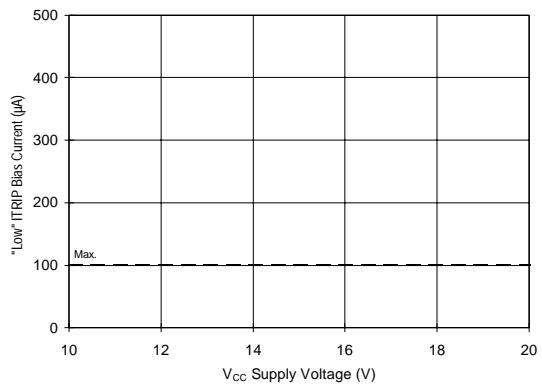


Figure 32B. "Low" ITRIP Current vs. Voltage

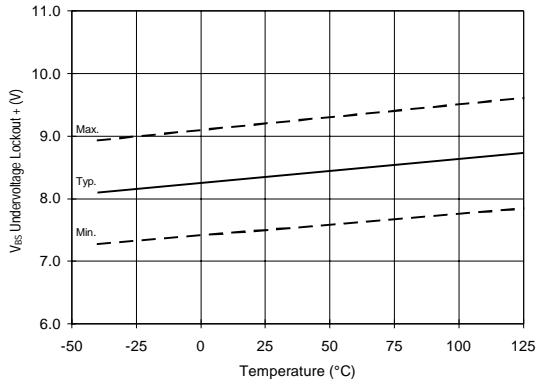


Figure 33. V_{BS} Undervoltage (+) vs. Temperature

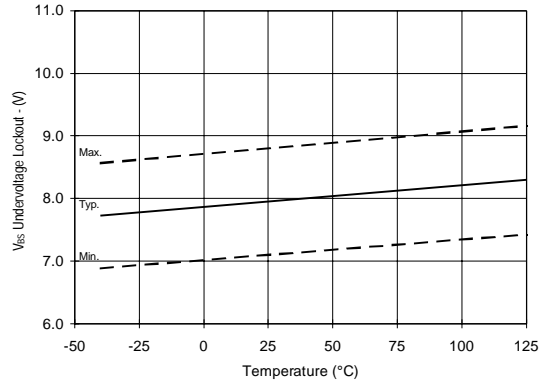


Figure 34. V_{BS} Undervoltage (-) vs. Temperature

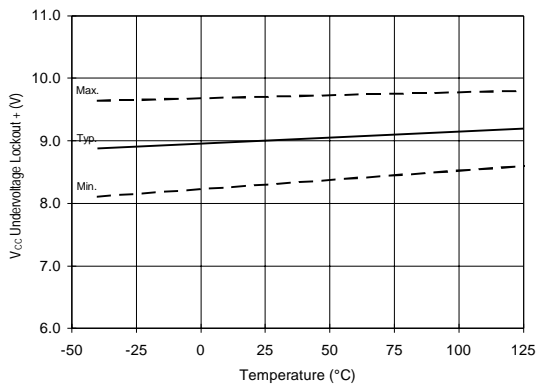


Figure 35. V_{CC} Undervoltage (+) vs. Temperature

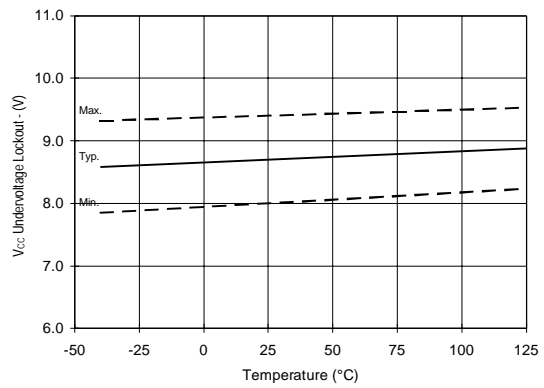


Figure 36. V_{CC} Undervoltage (-) vs. Temperature

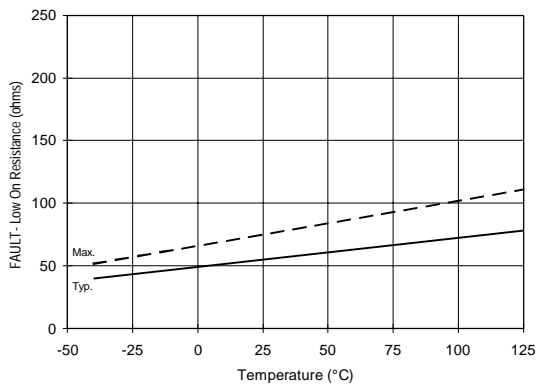


Figure 37A. **FAULT** Low On Resistance vs. Temperature

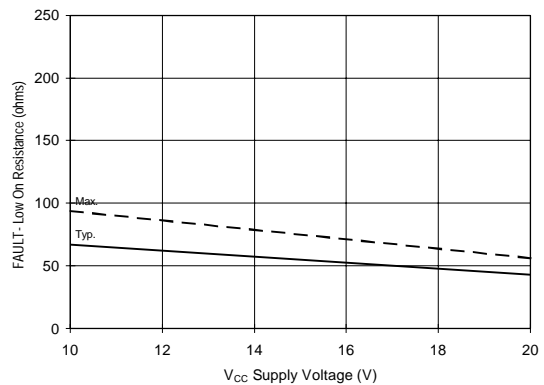


Figure 37B. **FAULT** Low On Resistance vs. Voltage

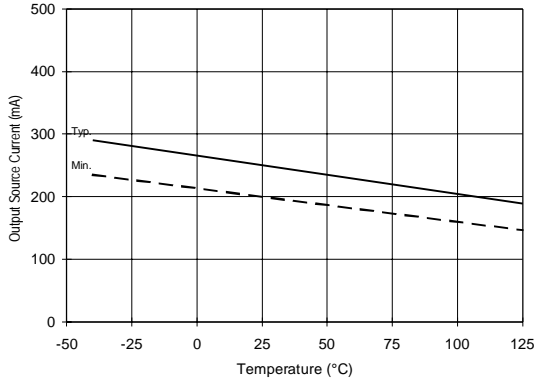


Figure 38A. Output Source Current vs. Temperature

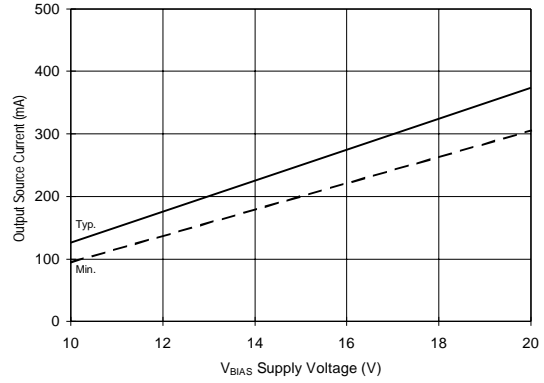


Figure 38B. Output Source Current vs. Voltage

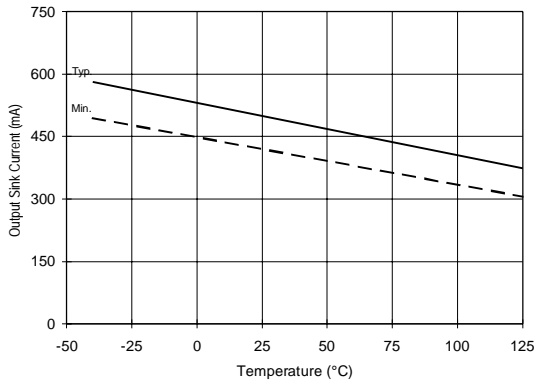


Figure 39A. Output Sink Current vs. Temperature

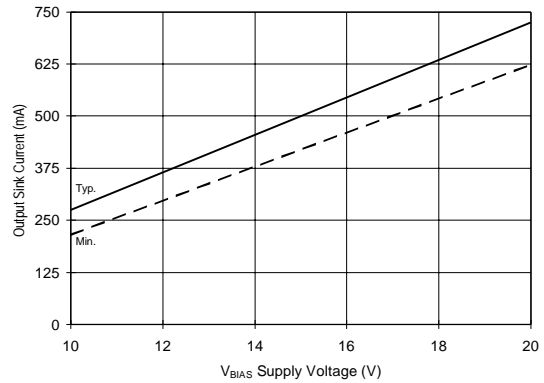


Figure 39B. Output Sink Current vs. Voltage

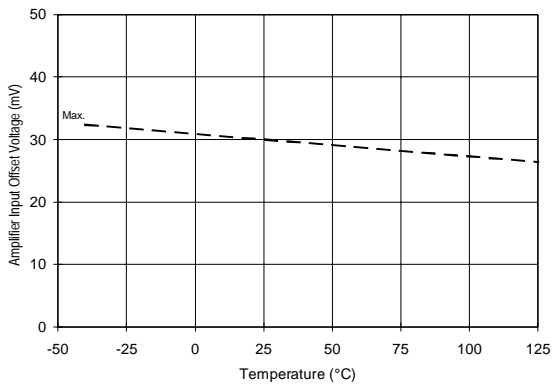


Figure 40A. Amplifier Input Offset vs. Temperature

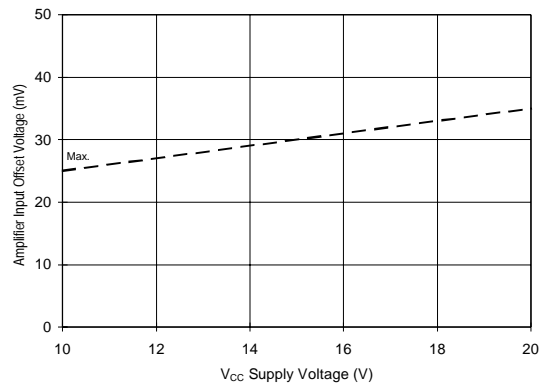


Figure 40B. Amplifier Input Offset vs. Voltage

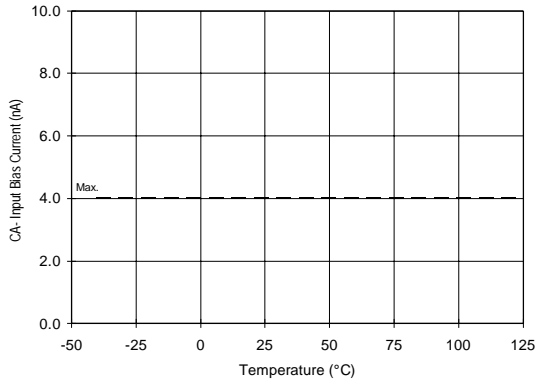


Figure 41A. CA- Input Current vs. Temperature

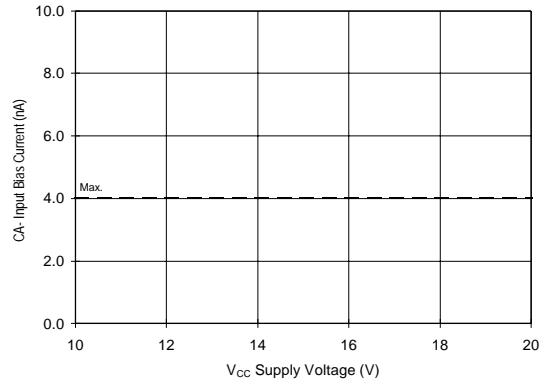


Figure 41B. CA- Input Current vs. Voltage

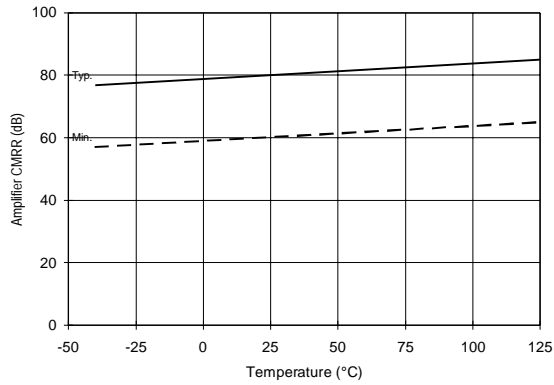


Figure 42A. Amplifier CMRR vs. Temperature

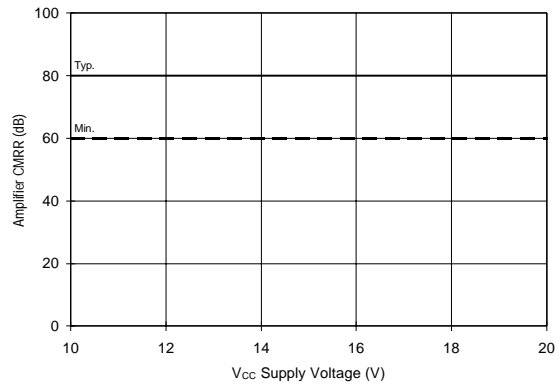


Figure 42B. Amplifier CMRR vs. Voltage

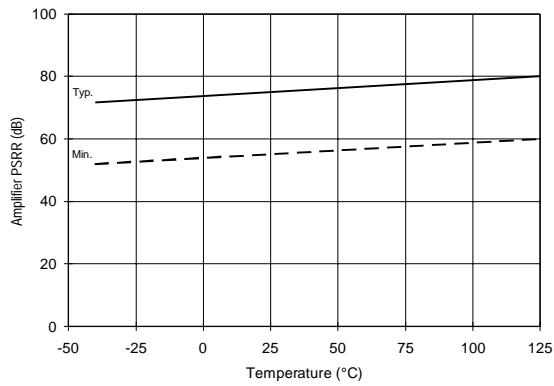


Figure 43A. Amplifier PSRR vs. Temperature

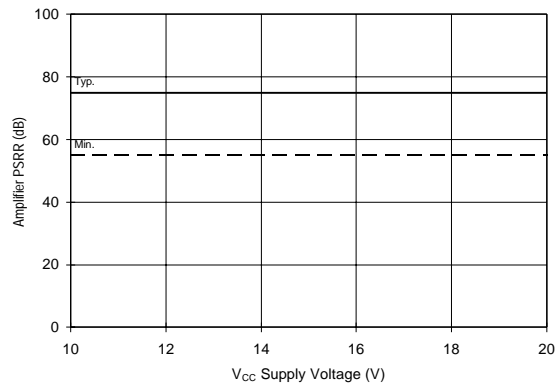


Figure 43B. Amplifier PSRR vs. Voltage

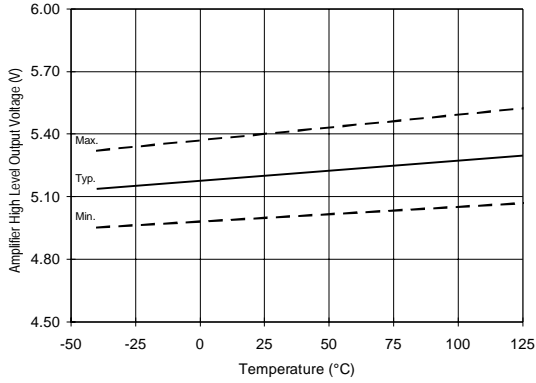


Figure 44A. Amplifier High Level Output vs. Temperature

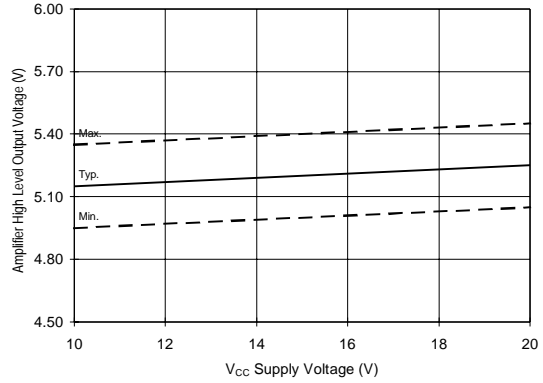


Figure 44B. Amplifier High Level Output vs. Voltage

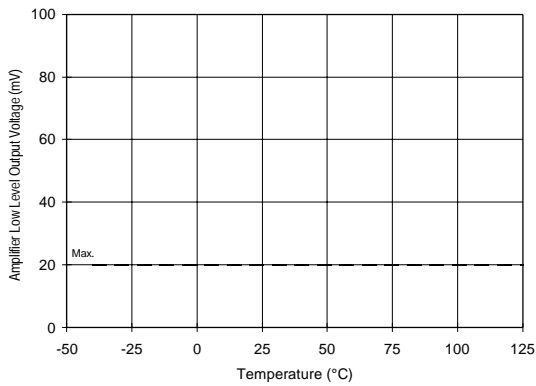


Figure 45A. Amplifier Low Level Output vs. Temperature

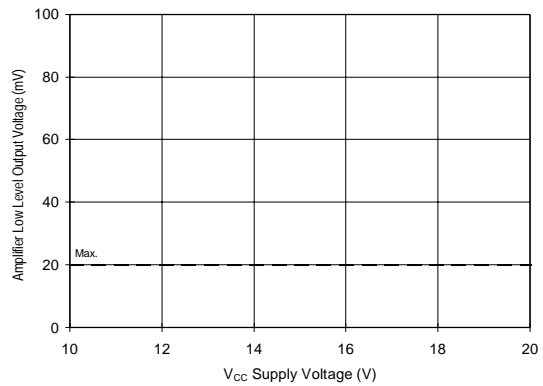


Figure 45B. Amplifier Low Level Output vs. Voltage

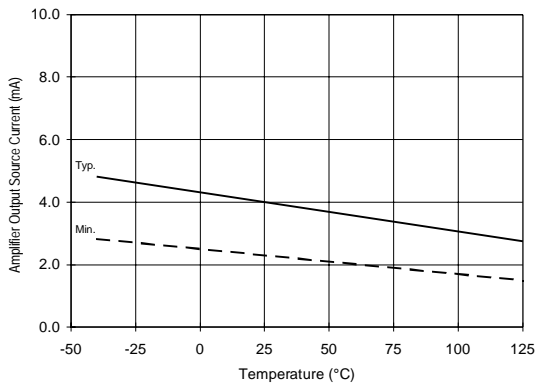


Figure 46A. Amplifier Output Source Current vs. Temperature

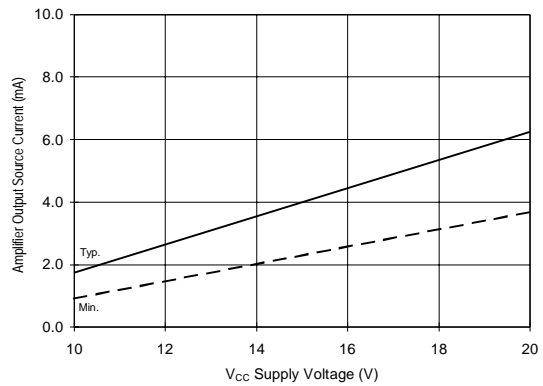


Figure 46B. Amplifier Output Source Current vs. Voltage

IR2130D

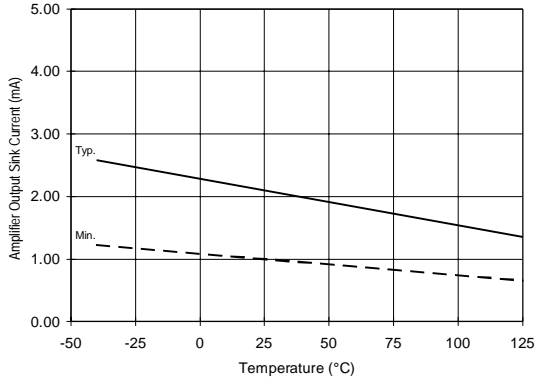


Figure 47A. Amplifier Output Sink Current vs. Temperature

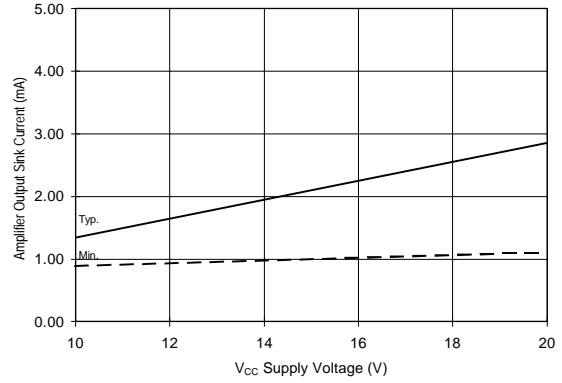


Figure 47B. Amplifier Output Sink Current vs. Voltage

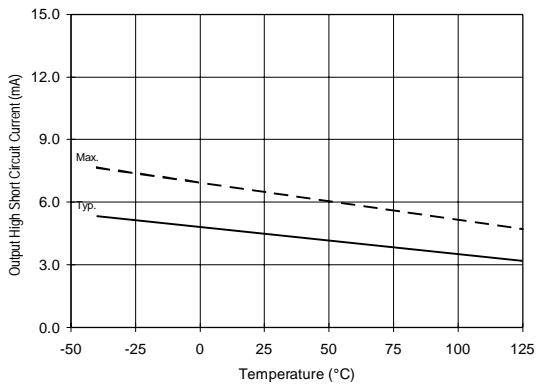


Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

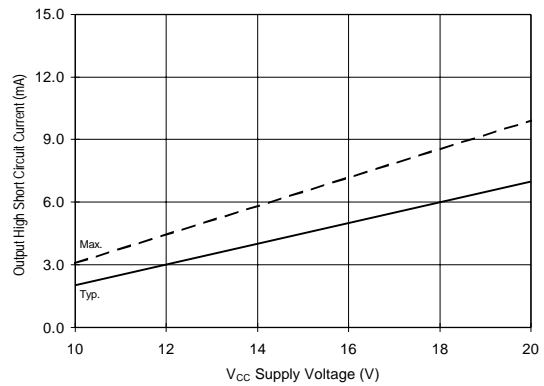


Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

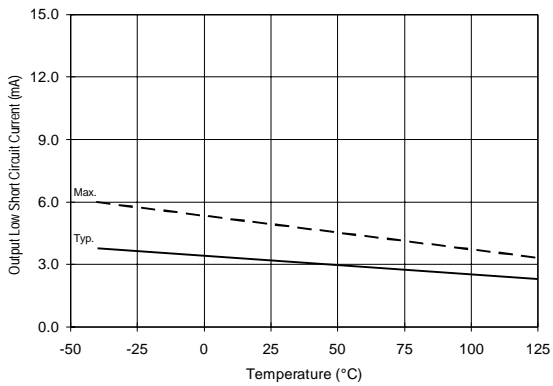


Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

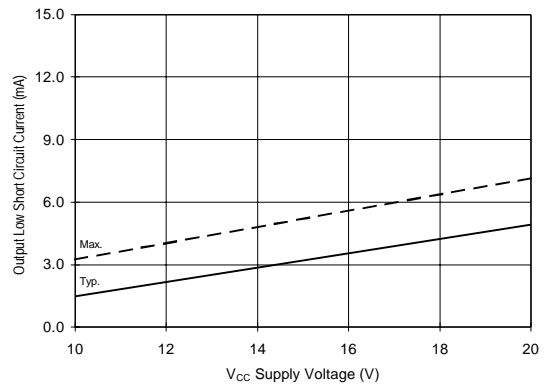


Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

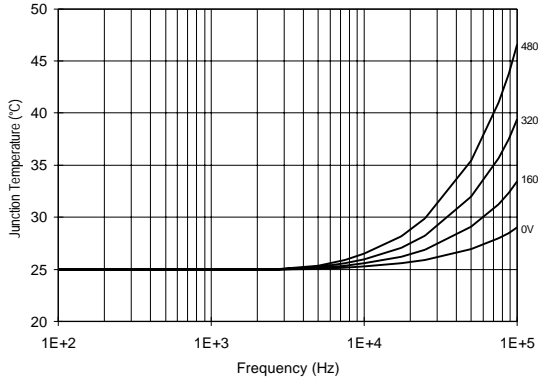


Figure 50. IR2130 T_J vs. Frequency (IRF820)
 $R_{GATE} = 33W, V_{CC} = 15V$

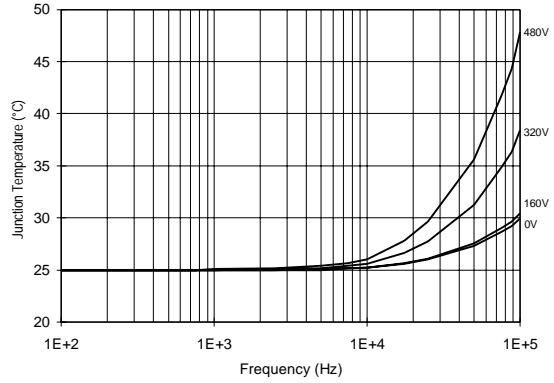


Figure 51. IR2130 T_J vs. Frequency (IRF830)
 $R_{GATE} = 20W, V_{CC} = 15V$

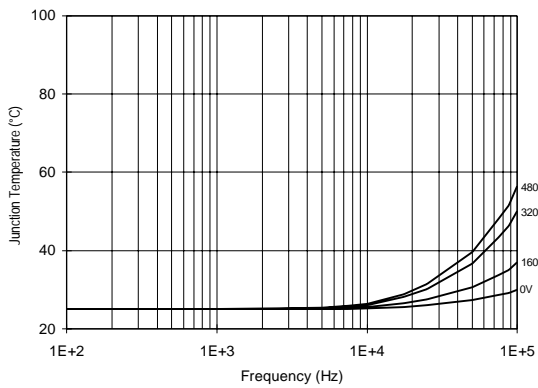


Figure 52. IR2130 T_J vs. Frequency (IRF840)
 $R_{GATE} = 15W, V_{CC} = 15V$

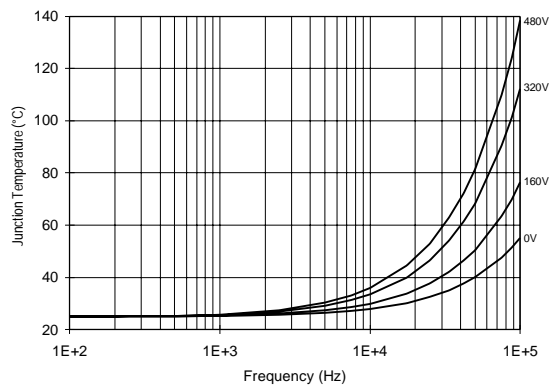


Figure 53. IR2130 T_J vs. Frequency (IRF450)
 $R_{GATE} = 10W, V_{CC} = 15V$

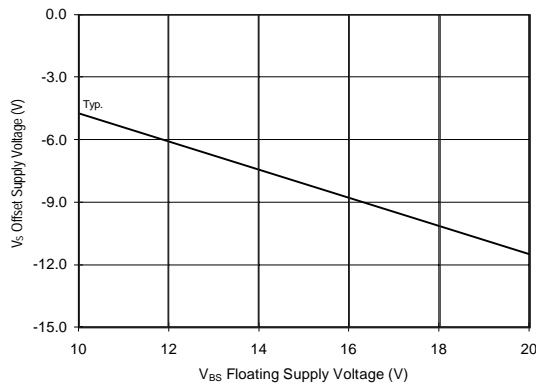
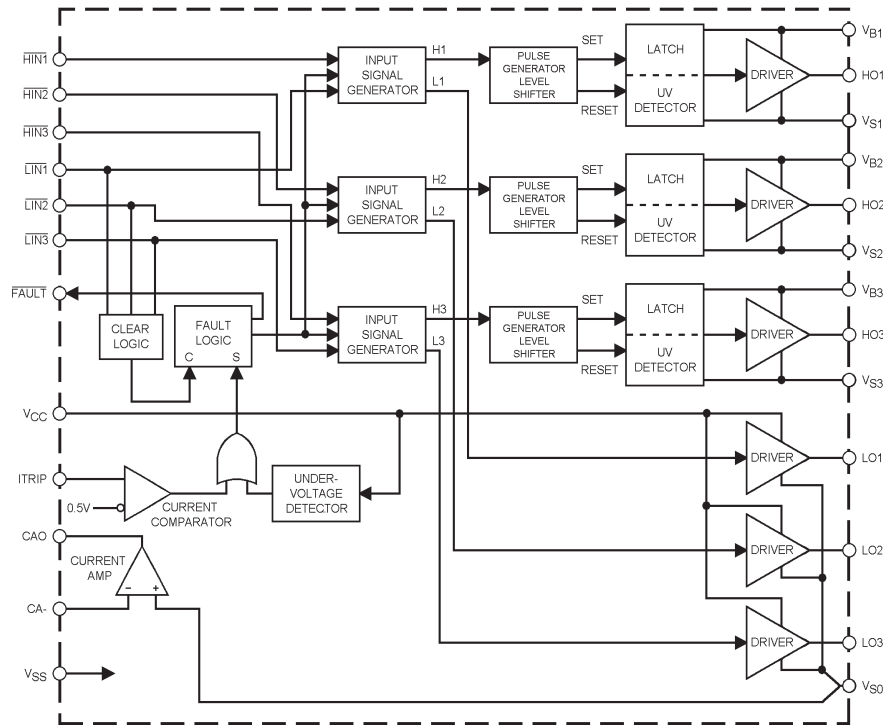


Figure 54. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

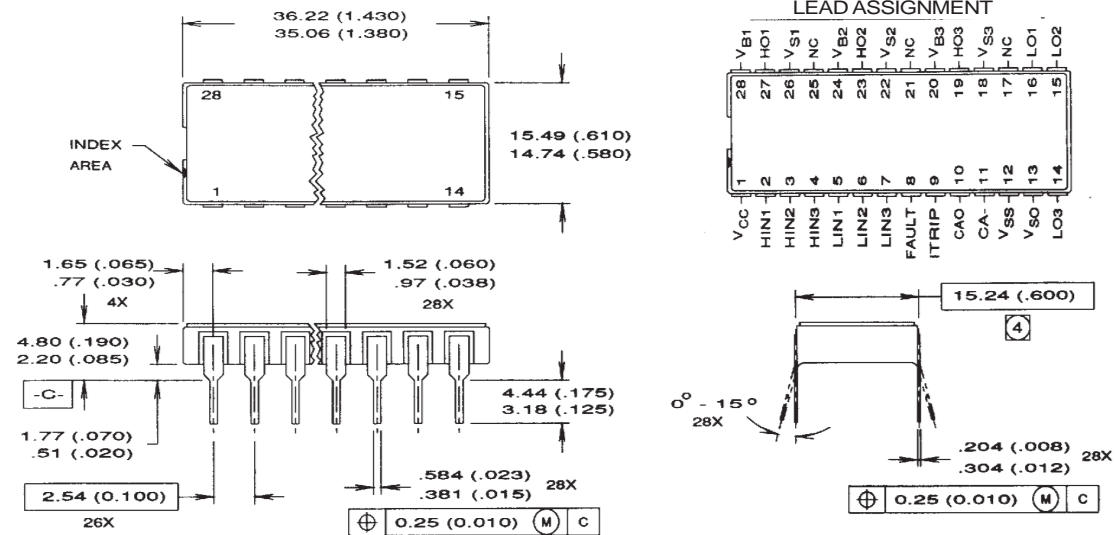
Functional Block Diagram



Lead Definitions

Lead	
Symbol	Description
HIN1,2,3	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
LIN1,2,3	Logic inputs for low side gate driver output (LO1,2,3), out of phase
FAULT	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
VCC	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
VSS	Logic ground
Vb1,2,3	High side floating supplies
HO1,2,3	High side gate drive outputs
Vs1,2,3	High side floating supply returns
LO1,2,3	Low side gate drive outputs
Vs0	Low side return and positive input of current amplifier

Case Outline and dimensions - MO038AB



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH.
 - 3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 - 4 DIMENSION IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - 5 OUTLINE CONFORMS TO JEDEC OUTLINE MO-038AB.

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IR EUROPEAN REGIONAL CENTER: 439/445 Godstone Rd, Whyteleafe, Surrey CR3 0BL, UK Tel: ++ 44 (0)20 8645 8000
IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200
IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590
IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086
IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 (0)838 4630
IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936
Data and specifications subject to change without notice. 3/00