DEIC515

15 Ampere Low-Side Ultrafast RF MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected
- High Peak Output Current: 15A Peak
- Wide Operating Range: 8V to 30V
- Rise And Fall Times of <4ns
- Minimum Pulse Width Of 8ns
- High Capacitive Load Drive Capability: 2nF in <4ns
- Matched Rise And Fall Times
- 18ns Input To Output Delay Time
- Low Output Impedance
- Low Quiescent Supply Current

Applications

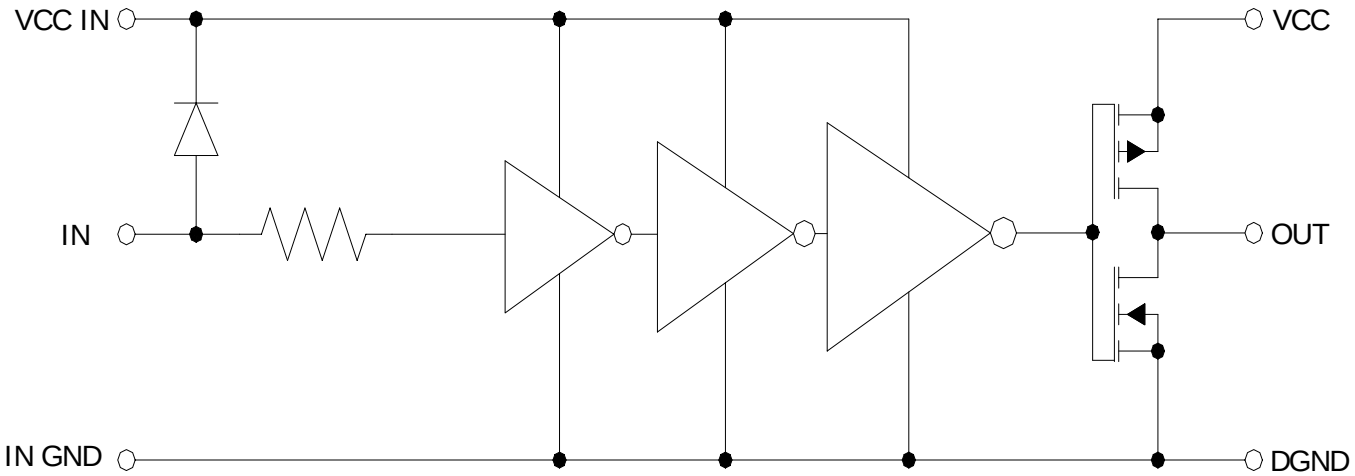
- Driving RF MOSFETs
- Class D or E Switching Amplifier Drivers
- Multi MHz Switch Mode Power Supplies (SMPS)
- Pulse Generators
- Acoustic Transducer Drivers
- Pulsed Laser Diode Drivers
- DC to DC Converters
- Pulse Transformer Driver

Description

TheDEIC515 is a CMOS high speed high current gate driver specifically designed to drive MOSFETs in Class D and E HF RF applications at up to 45MHz, as well as other applications requiring ultrafast rise and fall times or short minimum pulse widths. The DEIC515 can source and sink 15A of peak current while producing voltage rise and fall times of less than 4ns, and minimum pulse widths of 8ns. The input of the driver is fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the DEIC515. Its features and wide safety margin in operating voltage and power make the DEIC515 unmatched in performance and value.

The DEIC515 is packaged in DEI's low inductance RF package incorporating DEI's patented (1) RF layout techniques to minimize stray lead inductances for optimum switching performance. The DEIC515 is a surface-mount device. (1) DEI U.S. Patent #4,891,686

Figure 1 - DEIC515 Functional Diagram



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Absolute Maximum Ratings

Parameter	Value
Supply Voltage	30V
Input	-5V to Vccin+0.3V
All other Pins	-0.3V to (Vcc,Vccin)+0.3V
Power Dissipation $T_{AMBIENT} \leq 25C$ $T_{case} \leq 25C$	 2W 100W
Storage Temperature	-40C to 150C
Soldering Lead Temperature (10 seconds maximum)	300C

Parameter	Value
Maximum Junction Temperature	150^oC
Operating Temperature Range	-40^oC to 85^oC
Thermal Impedance (Junction To Case) θ_{JC}	$0.13^oC/W$

Electrical Characteristics

Unless otherwise noted, $T_A = 25\ ^oC$, $8V < V_{CC}=V_{CCIN} < 30V$.
All voltage measurements with respect to DGND. DEIC515 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		V_{CCIN} -2			V
V_{IL}	Low input voltage				0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	$0V \leq V_{IN} \leq V_{CC},V_{CCIN}$	-10		10	µA
V_{OH}	High output voltage		V_{CC},V_{CCIN} - .025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	I_{OUT} = 10mA, $_{VCC}$ = 15V		0.55	0.85	Ω
R_{OL}	Output resistance @ Output Low	I_{OUT} = 10mA, $_{VCC}$ = 15V		0.35	0.85	Ω
I_{PEAK}	Peak output current	V_{CC},V_{CCIN} = 15V		15		A
I_{DC}	Continuous output current			2.5		A
f_{MAX}	Maximum frequency	C_L=2nF V_{CC},V_{CCIN} =15V			45	MHz
t_R	Rise time (1)	C_L=1nF V_{CC},V_{CCIN} =15V V_{OH}=2V to 12V C_L=2nF V_{CC},V_{CCIN} =15V V_{OH}=2V to 12V		2.5 4.1		ns ns
t_F	Fall time (1)	C_L=1nF V_{CC},V_{CCIN} =15V V_{OH}=12V to 2V C_L=2nF V_{CC},V_{CCIN} =15V V_{OH}=12V to 2V		2.5 3.9		ns ns
t_{ONDLY}	On-time propagation delay (1)	C_L=2nF Vcc=15V		17.4	18.5	ns
t_{OFFDLY}	Off-time propagation delay (1)	C_L=2nF Vcc=15V		14.6	16	ns
P_{Wmin}	Minimum pulse width	FWHM C_L=1nF V_{CC},V_{CCIN} =15V +3V to +3V C_L=1nF V_{CC},V_{CCIN} =15V		6.4 8.2		ns ns
V_{CC},V_{CCIN}	Power supply voltage		8	15	30	V
I_{CC}	Power supply current	V_{IN} = 0V V_{IN} = V_{CCIN}		0	10 10	µA µA

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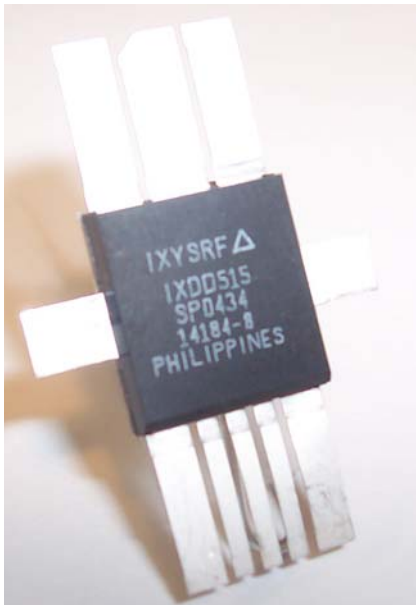
Lead Description - DEIC515

SYMBOL	FUNCTION	DESCRIPTION
VCC	Output Supply Voltage	Input for the positive output section power-supply voltage. These leads provide power to the output section. Both leads must be connected.
VCCIN	Supply Voltage	Input for the positive input section power-supply voltage. This lead provide power to the input section. This lead should not be directly connected to VCC.
IN	Input	Input signal.
OUT	Output	Driver Output.
PGND	Power Ground	The system ground leads. Internally connected to all circuitry, these leads provide ground reference for the entire chip. These leads should be connected to a low noise analog ground plane for optimum performance.
INGND	Input Ground	The input ground lead. This lead is a Kelvin connection internally to PGND. This lead must not be connected to PGND as excessive current can damage this lead.

Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - DEIC515 Package Photo And Outline



Bottom View

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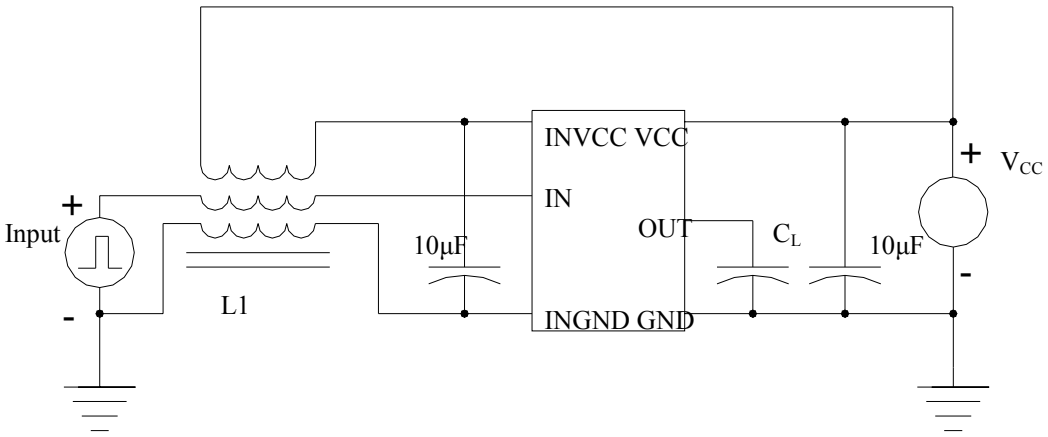
Typical Performance Characteristics

Figure 3a - Characteristics Test Diagram



Application

The very high currents and high speeds inside the DEIC515 create very large transients. To avoid problems with false triggering, the input to the DEIC515 should be supplied via a common mode choke. This is a simple tri-filar winding on a small ferrite core. This prevents high speed transients from effecting the input signals, by allowing the input signals to follow the internal die potential changes without changing the state of the input.

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