SC486
Complete DDR1/2/3 Memory Power Supply

POWER MANAGEMENT

Description

The SC486 is a combination switching regulator and linear source/sink regulator intended for DDR1/2/3 memory systems. The switching regulator is used to generate the supply voltage, VDDQ, for the memory system. It is a pseudo-fixed frequency constant on-time controller designed for high efficiency, superior DC accuracy, and fast transient response. The linear source/sink regulator is used to generate the memory termination voltage, VTT, with the ability to source and sink a 3A peak current.

For the VDDQ regulator, the switching frequency is constant until a step in load or line voltage occurs at which time the pulse density, i.e. frequency, will increase or decrease to counter the transient change in output or input voltage. After the transient, the frequency will return to steady-state operation. At lighter loads, the selectable Power-Save Mode enables the PWM converter to reduce its switching frequency and improve efficiency. The integrated gate drivers feature adaptive shoot-through protection and soft-switching.

For the VTT regulator, the output voltage tracks VREF, which is ½ VDDQ to provide an accurate termination voltage. The VTT output is generated from a 1.2V to VDDQ input by a linear source/sink regulator which is designed for high DC accuracy, fast transient response, and low external component count. Additional features include cycle-by-cycle current limiting, digital soft-start, power good (all VDDQ only) and over-voltage and under-voltage protection (VDDQ and VTT). All 3 outputs (VDDQ, VTT and REF) are actively discharged when VDDQ is disabled, reducing external component count and cost. The SC486 is available in a 24 pin MLPQ 4mmx4mm Lead-free package.

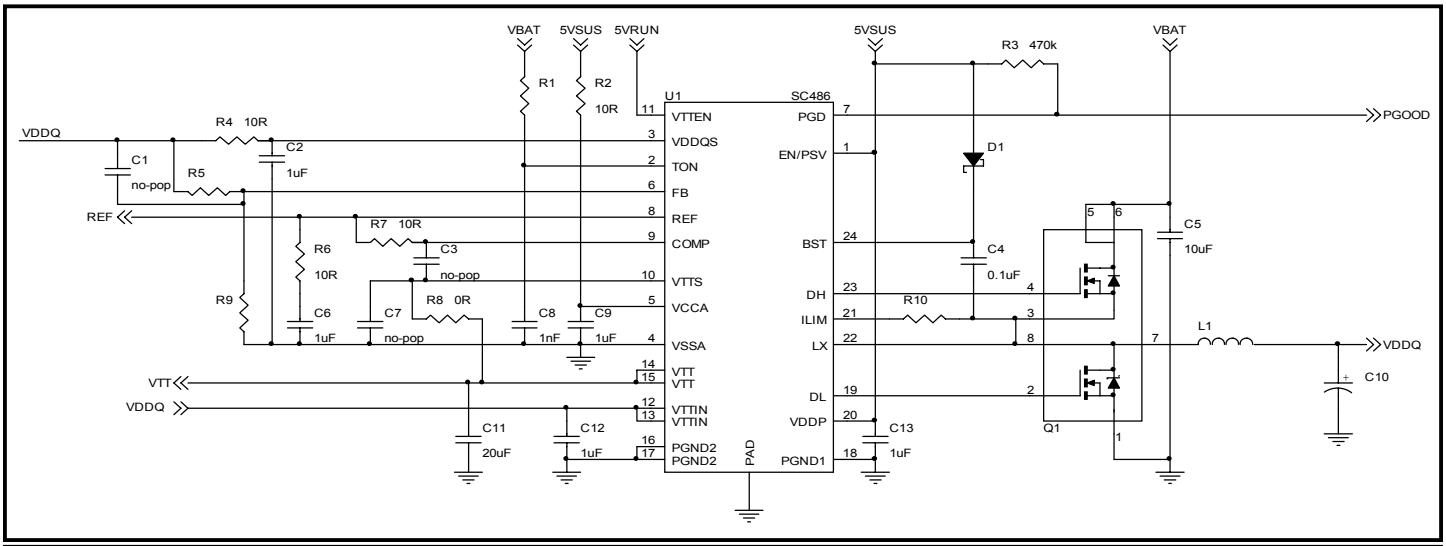
Typical Application Circuit

Features

- DDR1, DDR2 and DDR3 compatible
- Constant on-time controller for fast dynamic response on VDDQ
- Programmable VDDQ range - 1.5V to 3V
- 1% Internal Reference (2% System Accuracy)
- Resistor programmable on time for VDDQ
- VCCA/VDDP range = 4.5V to 5.5V
- VBAT range = 2.5V to 25V
- VDDQ DC current sense using low-side $R_{DS(ON)}$ sensing or external R_{SENSE} in series with low-side FET
- Cycle-by-cycle current limit for VDDQ
- Digital soft-start for VDDQ
- Combined EN and PSAVE pin for VDDQ
- Over-voltage/under-voltage fault protection for both outputs and PGD output (VDDQ only)
- Separate VCCA and VDDP supplies
- VTT/REF range = 0.75V – 1.5V
- VTT source/sink 3A peak
- Internal resistor divider for VTT/REF
- VTT is high impedance in S3
- VDDQ, VTT and REF are actively discharged in S4/S5
- 24-pin MLPQ (4 x 4mm) Lead-free package, fully WEEE and RoHS compliant

Applications

- Notebook computers
- CPU I/O supplies
- Handheld terminals and PDAs
- LCD monitors
- Network power supplies



Absolute Maximum Ratings (10)

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
TON to VSSA		-0.3 to +25.0	V
DH, BST to PGND1		-0.3 to +30.0	V
LX to PGND1		-2.0 to +25.0	V
DL, ILIM, VDDP to PGND1		-0.3 to +6.0	V
VDDP to DL		-0.3 to +6.0	V
VTTIN, VTT to PGND2		-0.3 to +6.0	V
VTTIN to VTT		-0.3 to +6.0	V
COMP, EN/PSV, FB, PGD, REF, VCCA, VDDQS, VTTEN, VTTS TO VSSA		-0.3 to +6.0	V
VCCA to COMP, EN/PSV, FB, REF, VDDQS, VTT, VTTEN, VTTIN, VTTS		-0.3 to +6.0	V
PGND1 to PGND2, PGND1 to VSSA		-0.3 to +0.3	V
BST, DH to LX		-0.3 to +6.0	V
Thermal Resistance Junction to Ambient	θ_{JA}	29	°C/W
Operating Junction Temperature Range	T_J	-40 to +150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature, 10s - 40s	T_{PKG}	260	°C

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, VCCA = VDDP = VTTEN = EN/PSV = 5V, VDDQ = VTTIN = 1.8V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA Operating Current	FB > regulation point, I_{VDDQ} = 0A		1500			2500	µA
VCCA Operating Current, S3	FB > regulation point, I_{VDDQ} = 0A, VTTEN = 0V		1000				µA
VDDP Operating Current	FB > regulation point, I_{VDDQ} = 0A		70			150	µA
TON Operating Current	RTON = 1MΩ		15				µA
VTTIN Operating Current	I_{VTT} = 0A		1			5	µA
VCCA + VDDP + TON Shutdown Current	EN/PSV = VTTEN = 0V		5			11	µA

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, VCCA = VDDP = VTTEN = EN/PSV = 5V, VDDQ = VTTIN = 1.8V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
VDDQ Controller							
FB Error Comparator Threshold(1)	VCCA = 4.5V to 5.5V		1.500		1.485	1.515	V
On-Time	R_{TON} = 1MΩ		460		390	530	ns
	R_{TON} = 500kΩ, -10°C ≤ T_A ≤ 125°C		265		225	305	
	R_{TON} = 500kΩ, -40°C ≤ T_A ≤ 125°C				225	320	
Minimum Off-Time			400			550	ns
VDDQS Input Resistance			150				kΩ
VDDQS Shutdown Discharge Resistance	EN/PSV = GND		22				Ω
FB Leakage Current					-1.0	1.0	µA
VTT Controller							
COMP Leakage Current					-1.0	1.0	µA
REF Source Current					10		mA
REF Output Accuracy	I_{REF} = 0 to 10mA		900		882	918	mV
REF Shutdown Discharge Resistance	EN/PSV = GND		22				Ω
VTT Output Accuracy	-2A < I_{VTT} < 2A		REF		-20	+20	mV
VTT Shutdown Discharge Resistance	EN/PSV = GND		22				Ω
VTTS Leakage Current					-1.0	1.0	µA
Current Sensing							
ILIM Current			10		9	11	µA
Current Comparator Offset	PGND1 - ILIM				-10	10	mV
Zero-Crossing Threshold	PGND1 - LX, EN/PSV = 5V		5				mV
VDDQ Fault Protection							
Current Limit (Positive)(2)	PGND1 - LX, R_{ILIM} = 5kΩ		50		35	65	mV
	PGND1 - LX, R_{ILIM} = 10kΩ		100		80	120	
	PGND1 - LX, R_{ILIM} = 20kΩ		200		170	230	
Current Limit (Negative)	PGND1 - LX		-125		-160	-90	mV
Output Under Voltage Fault	With respect to internal reference		-30		-35	-25	%
Under Voltage Fault Delay	FB forced below UV Vth		8				clks(3)

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, VCCA = VDDP = VTTEN = EN/PSV = 5V, VDDQ = VTTIN = 1.8V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
VDDQ Fault Protection (Cont.)							
Under Voltage Blank Time	From EN high		440				clks(3)
Output Over Voltage Fault	With respect to internal reference		+16		+12	+20	%
Over Voltage Fault Delay	FB forced above OV Vth		5				µs
PGD Low Output Voltage	Sink 1mA					0.4	V
PGD Leakage Current	FB in regulation, PGD = 5V					1	µA
PGD UV Threshold	With respect to internal reference		-10		-12	-8	%
PGD Fault Delay	FB forced outside PGD window		5				µs
VCCA Under Voltage	Falling edge, hysteresis 100mV		4.0		3.7	4.3	V
VTT Fault Protection							
Output Under Voltage Fault	VTT w/rt REF		-12		-16	-8	%
Output Over Voltage Fault	VTT w/rt REF		+12		+8	+16	%
Fault Shutdown Delay	VTT outside UV/OV window		50				µs
Thermal Shutdown (4)(5)			160		150	170	°C
Inputs/Outputs							
Logic Input Low Voltage	EN & PSV low					1.2	V
	VTTEN low					0.6	
Logic Input High Voltage	EN high, PSV low		2.0				V
	VTTEN high				2.4		
Logic Input High Voltage	EN high, PSV high				3.1		V
EN/PSV Input Resistance	Sourcing		1.5				MΩ
	Sinking		1.0				
Soft Start							
VDDQ Soft Start Ramp Time	EN/PSV high to PGD high		440				clks(3)
VTT Soft Start Ramp Rate (6)			6				mV/µs
Gate Drives							
Shoot-thru Protection Delay (4)(7)	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Sink Current	V_{DL} = 2.5V		3.1				A

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, VCCA = VDDP = VTTEN = EN/PSV = 5V, VDDQ = VTTIN = 1.8V, R_{TON} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Gate Drives (Cont.)							
DL Pull-Up Resistance	DL high		2			4	Ω
DL Source Current	V_{DL} = 2.5V		1.3				A
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance(8)	DH high, BST - LX = 5V		2			4	Ω
DH Sink/Source Current	V_{DH} = 2.5V		1.3				A
VTT Pull-Up Resistance	VTTS < REF		0.25			0.45	Ω
VTT Pull-Down Resistance	VTTS > REF		0.25			0.45	Ω
VTT Peak Sink/Source Current (9)			3.6		2.0		A

Notes:

(1) The output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

(2) Using a current sense resistor, this measurement relates to PGND1 minus the voltage of the source on the low-side MOSFET.

(3) clks = switching cycles, consisting of one high side and one low side gate pulse.

(4) Guaranteed by design.

(5) Thermal shutdown latches both outputs (VTT and VDDQ) off, requiring VCCA or EN/PSV cycling to reset.

(6) VTT soft start ramp rate is 6mV/µs typical unless VDDQ/2 ramp rate is slower. If this is true, VTT soft start ramps at 6mV/µs (typ.) until it reaches VDDQ/2, and then tracks it.

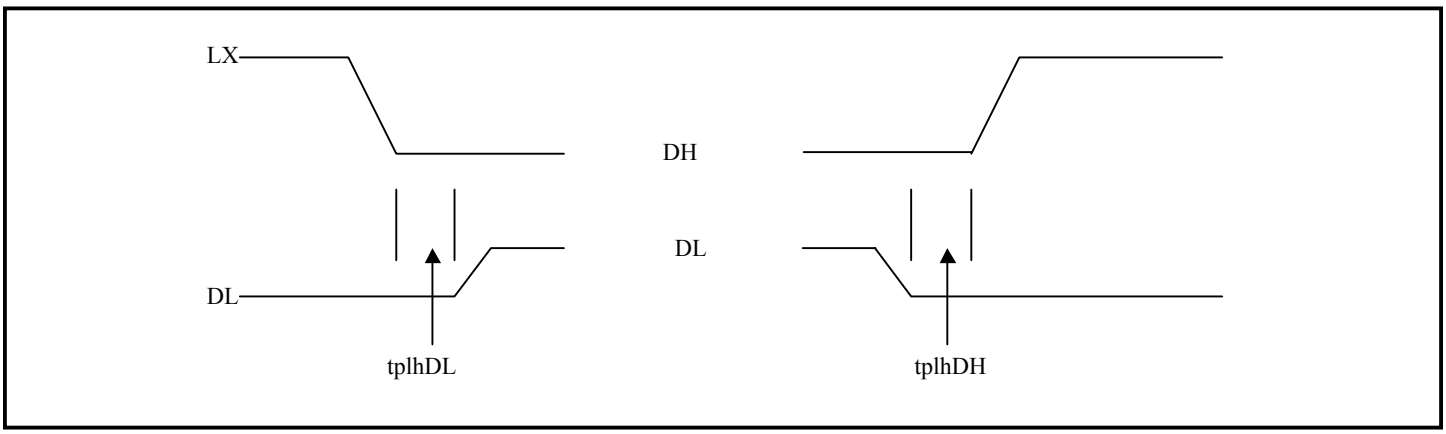
(7) See Shoot-Through Delay Timing Diagram below.

(8) Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typ.). This negates the need for an external gate or boost resistor.

(9) Provided operation below $T_{J(MAX)}$ is maintained.

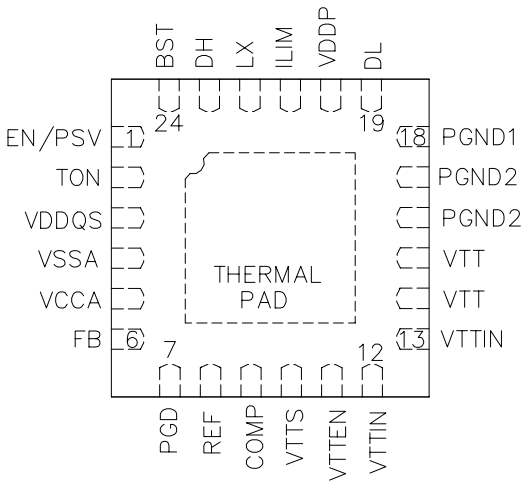
(10) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Shoot-Through Delay Timing Diagram



Pin Configuration

Top View



(MLPQ-24)

Ordering Information

DEVICE	PACKAGE(1)
SC486IMLTRT(2)	MLPQ-24
SC486EVB	Evaluation Board

Note:
(1) Only available in tape and reel packaging. A reel contains 3000 devices.
(2) Lead-free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

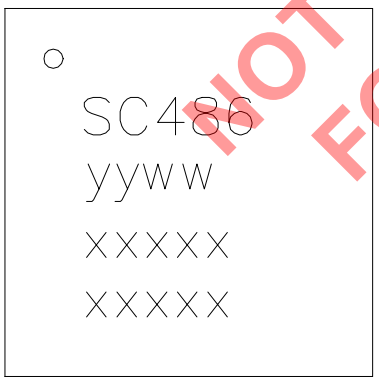
Pin #	Pin Name	Pin Function
1	EN/PSV	Enable/Power Save input pin. Tie to ground to disable VDDQ. Tie to +5V to enable VDDQ and activate PSAVE mode. Float to enable VDDQ and activate continous conduction mode. If floated, bypass to VSSA with a 10nF capacitor.
2	TON	This pin is used to sense VBAT through a pullup resistor, RTON, and set the top MOSFET on-time. Bypass this pin with a 1nF capacitor to VSSA.
3	VDDQS	Sense pin for VDDQ. Used to set the on-time for the top MOSFET and also to set VREF/VTT. Use a 10Ω/1µF RC filter from VDDQ to VSSA.
4	VSSA	Ground reference for analog circuitry. Connect directly to R9, C6, C7, C8, and C9 (see Page 1) on same side of PCB as I.C. Connect to thermal pad.
5	VCCA	Supply voltage input for the analog supply. Use a 10Ω/1µF RC filter from 5VSUS to VSSA.
6	FB	Feedback input for VDDQ. Connect to a resistor divider from the output to VSSA to set the output voltage between 1.5V and VCCA.
7	PGD	Power good output for VDDQ. PGD is low if VDDQ is outside the power good thresholds. This pin is an open drain NMOS output and requires an external pull-up resistor.
8	REF	Reference output. An internal resistor divider from VDDQS sets this voltage to 50% VDDQ (nominal). Bypass this pin with a series 10Ω/1µF to VSSA. The connection to R6 (see Page 1) should be made close to pin 8.
9	COMP	Error amplifier compensation for VTT output.
10	VTTS	Sense pin for VTT. Connect to VTT at the load.
11	VTTEN	Enable pin for VTT. Pull this pin low to disable VTT (VREF remains present as long as VDDQ is present).
12,13	VTTIN	Input supply for the high side switch for VTT regulator. Decouple this pin with a 1µF capacitor to PGND2.

Pin Descriptions (Cont)

14,15	VTT	Output of the linear regulator. Decouple with two (minimum) 10µF ceramic capacitors to PGND2, locating them directly across pins 14, 15, 16, and 17.
16,17	PGND2	Power ground for VTT output. Connect to thermal pad and ground plane.
18	PGND1	Power ground for VDDQ output. Connect to thermal pad and ground plane.
19	DL	Gate drive output for the low side MOSFET switch.
20	VDDP	+5V supply voltage input for the VDDQ gate drivers.
21	ILIM	Current limit input pin. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor.
22	LX	Phase node - the junction between the top and bottom FETs and the output inductor.
23	DH	Gate drive output for the high side MOSFET switch.
24	BST	Boost capacitor connection for the high side gate drive.
-	THERMAL PAD	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Marking Information

Top View



Part Number
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: E9010
xxx 1-1)

Block Diagram

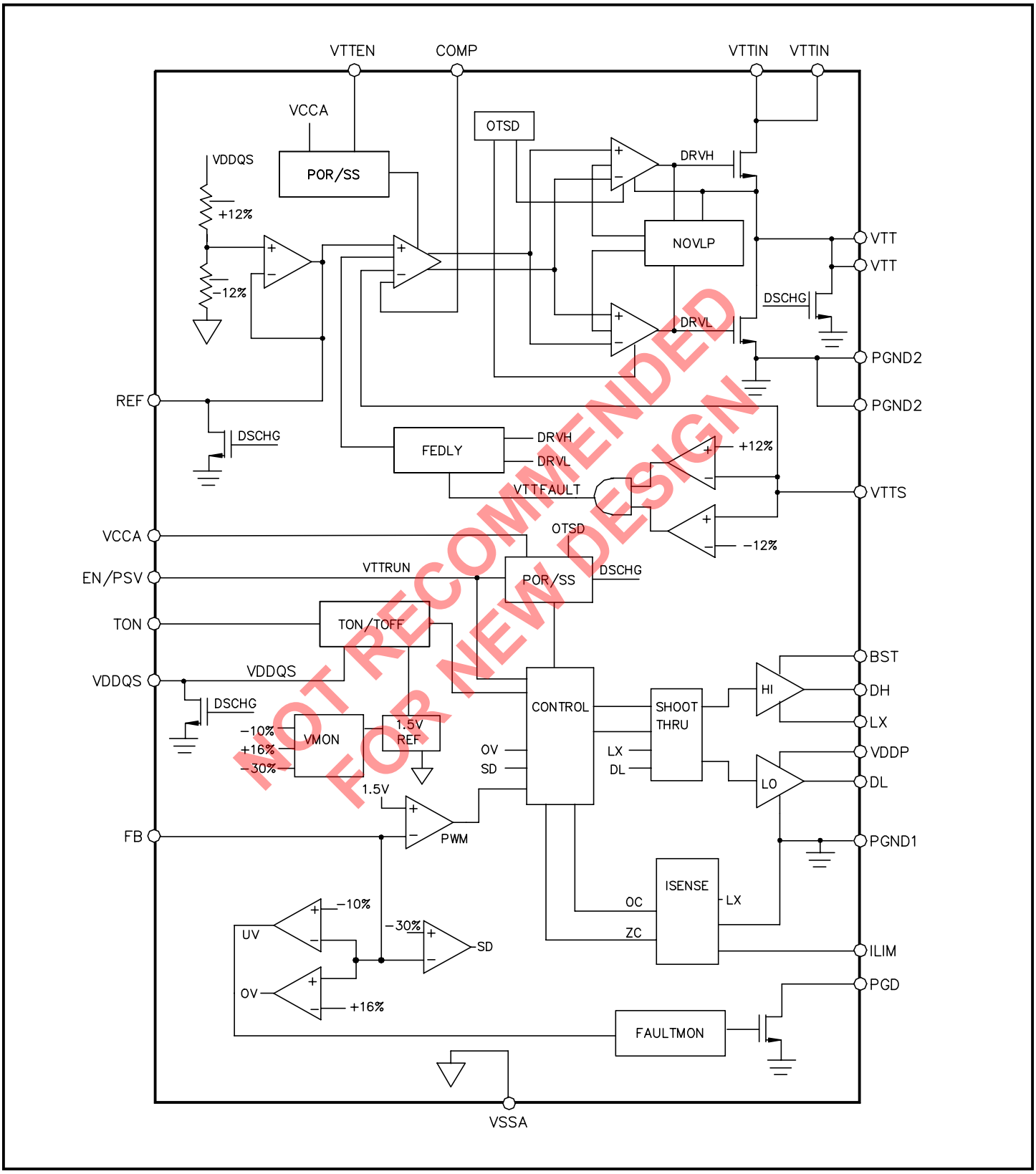


Figure 1 - SC486 Block Diagram

POWER MANAGEMENT

Enable Control Logic

Enable Pin Status		Output Status		
EN/PSV (1)	VTTEN	VDDQ	VTT	REF
0	0	OFF, Discharged (2)(3)	OFF, Discharged (2)	OFF, Discharged (2)
0	1	OFF, Discharged (2)(3)	OFF, Discharged (2)	OFF, Discharged (2)
1	0	ON	OFF, High Impedance	ON
1	1	ON	ON	ON

Notes:
(1) EN/PSV = 1 = EN/PSV high or floating.
(2) Discharge resistance = 22Ω typ.
(3) VDDQ is discharged via R4 (see Page 1) so this resistance must be added when calculating discharge times.

Application Information

+5V Bias Supply

The SC486 requires an external +5V bias supply in addition to the battery. This is connected to VDDP for the VDDQ switching drive power and via an RC filter to VCCA for the chip supply. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator.

VTTIN Supply

The VTTIN pins provide the input power for the high side (sourcing) section of the VTT LDO. These pins should be decoupled to PGND2. If the output capacitors for the input supply for VTTIN (whether it is VDDQ or a different supply) are not close to the chip, additional local bulk capacitance may be required.

Grounding

The SC486 has three ground connections, VSSA, PGND1 and PGND2 (2 pins). These should all be starred together at the thermal pad under the device, which in turn will be connected to the ground plane using multiple vias. VSSA is the controller ground reference, to avoid interference between the power and reference sections. PGND1 is the power ground connection for the switching controller for VDDQ. PGND2 is the power ground connection for the sink-source LDO for VTT. All external components referenced to VSSA in the schematic should be connected directly to the VSSA trace. The supply decoupling capacitor should be tied between VCCA and VSSA. A 10Ω resistor should be used to decouple the VCCA supply from the main VDDP supply. The VDDP input provides power to the upper and lower gate drivers of the switching supply. A decoupling capacitor with no series resistor between VDDP and 5V is required. See layout guidelines for more details.

Pseudo-fixed Frequency Constant On-Time PWM Controller (VDDQ)

The PWM control architecture consists of a constant on-time, pseudo fixed frequency PWM controller (see Figure 1, SC486 Block Diagram). The output ripple voltage developed across the output filter capacitor's ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time which is typically 400ns.

On-Time One-Shot (t_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage-proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need for a clock generator.

$$t_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50ns$$

R_{TON} is a resistor connected from the input supply to the TON pin. Due to the high impedance of this resistor, the TON pin should always be bypassed to VSSA using a 1nF ceramic capacitor.

EN/PSV: Enable, PSAVE and Soft Discharge

The EN/PSV pin enables the VDDQ (2.5V or 1.8V) output and the REF output. VTTEN enables the VTT (1.25V or 0.9V) output provided that VDDQ is present. See Enable Control Logic on Page 9.

When EN/PSV is pulled high the VDDQ controller is enabled and power save will also be enabled. When the EN/PSV pin is tri-stated (allowed to float, a 10nF capacitor is required in this instance), an internal pull-up will activate the VDDQ controller and power save will be disabled. If PSAVE is enabled, the SC486 PSAVE comparator will look for the inductor current to cross zero on eight consecutive switching cycles by comparing the phase node (LX) to PGND1. Once observed, the controller will enter power save and turn off the low side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteresis, the on-time is increased by 50% in power save. The efficiency improvement at light-loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller will immediately exit power save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when psave is enabled.

EN/PSV: Enable, PSAVE and Soft Discharge (Cont.)

If the EN/PSV pin is pulled low, all three outputs will be shut down and discharged using switches with a nominal resistance of 22 Ohms, regardless of the state of the VTTEN pin. This will ensure that the outputs will be in a defined state next time they are enabled and also ensure, since this is a soft discharge, that there are no dangerous negative voltage excursions to be concerned about. In order for the soft discharge circuitry to function correctly, the chip supply must be present.

VTTEN

The VTTEN pin is used to enable the VTT regulator only. Pulling it high enables the regulator as long as VDDQ/REF are present. Pulling VTTEN low while EN/PSV is floating or high will turn off the VTT regulator and leave it in a high-impedance state for S3 mode (VDDQ and REF present, VTT high-Z).

VDDQ Output Voltage Selection and Output Sense

The output voltage is set by the feedback resistors R5 & R9 of Figure 2 below. The internal reference is 1.5V, so the voltage at the feedback pin will match the 1.5V reference. Therefore the output can be set to a minimum of 1.5V. The equation for setting the output voltage is:

$$VOUT = \left(1 + \frac{R5}{R8}\right) \bullet 1.5$$

VDDQS is used to sense the output voltages for the on-time one-shot, t_{ON}, and also to generate REF, which is 1/2 of VDDQ. An RC filter consisting of 10Ω and 1µF from VDDQ to VSSA is required (R4 and C2 in Figure 2) to filter switching frequency ripple.

VDDQ Current Limit Circuit

Current limiting of the SC486 can be accomplished in two ways. The on-state resistance of the low-side MOSFETs can be used as the current sensing element or sense resistors in series with the low-side sources can be used if greater accuracy is desired. $R_{DS(ON)}$ sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistors between the ILIM pin and LX pin set the over current threshold. This resistor R_{ILIM} is connected to a 10µA current source within the SC486 which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low side MOSFET equals the voltage across the RILIM resistor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output undervoltage (see Output Undervoltage Protection).

The current sensing circuit actually regulates the inductor valley current (see Figure 3). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown overleaf.

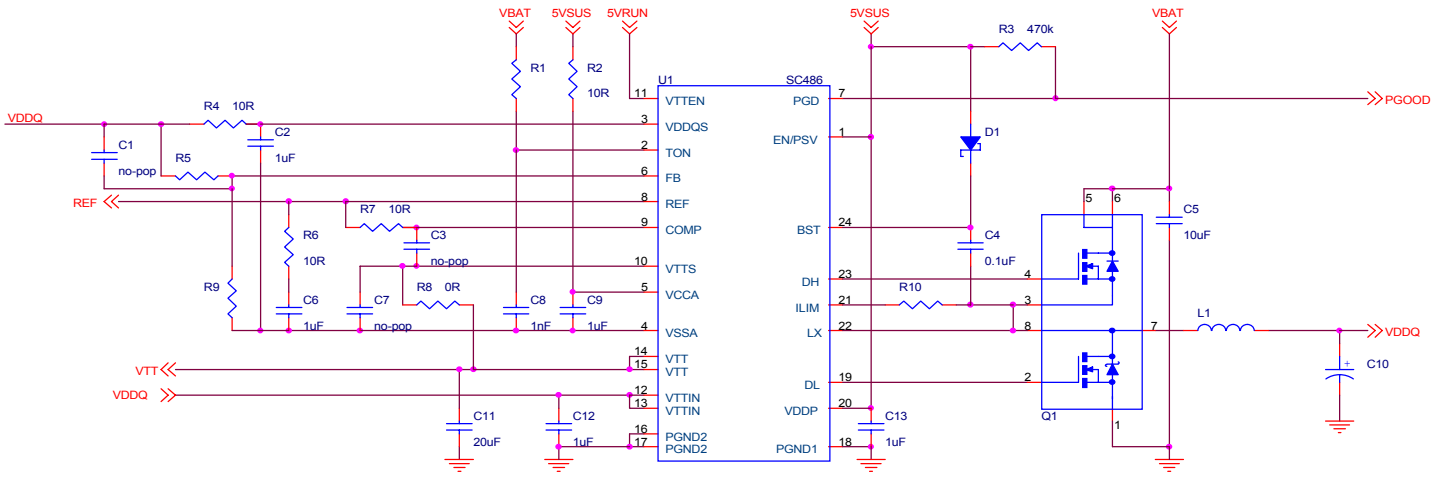


Figure 2

VDDQ Current Limit Circuit (Cont.)

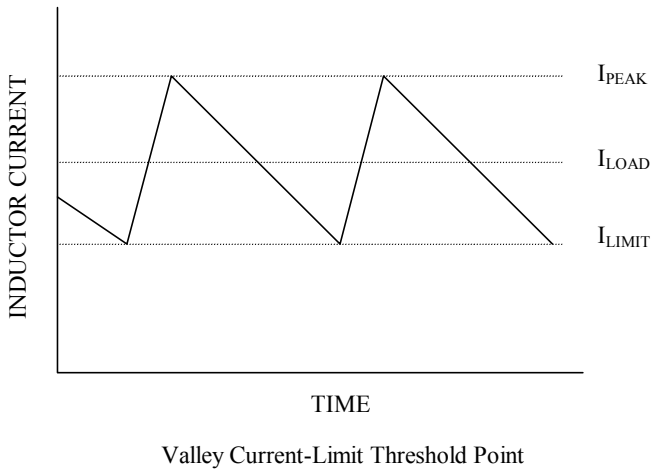


Figure 3: Valley Current Limiting

The equation for the current limit threshold is as follows:

$$I_{LIMIT} = 10e^{-6} \bullet \frac{R_{ILIM}}{R_{SENSE}} A$$

Where (referring to Figure 2) R_{ILIM} is R10 and R_{SENSE} is the $R_{DS(ON)}$ of the bottom of Q1.

For resistor sensing, a sense resistor is placed between the source of Q1 and PGND1. The current through the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches the voltage drop across R_{ILIM}, a positive over-current exists and the high side MOSFET will not be allowed to turn on. When using an external sense resistor R_{SENSE} is the resistance of the sense resistor.

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND1 through the inductor and bottom MOSFET). In this case, when the bottom MOSFET is turned on, the phase node, LX, will be higher than PGND initially. The SC486 monitors the voltage at LX, and if it is greater than a set threshold voltage of 125mV (nom.) the bottom MOSFET is turned off. The device then waits for approximately 2.5µs and then DL goes high for 300ns (typ.) once more to sense the current. This repeats until either the over-current condition goes away or the part latches off due to output overvoltage (see Output Overvoltage Protection).

Power Good Output

The VDDQ output has its own power good output. Power good is an open-drain output and requires a pull-up resistor. When VDDQ is 16% above or 10% below its set voltage, PGD gets pulled low. It is held low until the output voltage returns to within these thresholds. PGD is also held low during start-up and will not be allowed to transition high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5µs delay built into the PGD circuitry to prevent false transitions.

Output Overvoltage Protection

VDDQ: when the output exceeds 16% of its set voltage the low-side MOSFET is latched on. It stays latched on and the controller is latched off until reset (see below). There is a 5µs delay built into the OV protection circuit to prevent false transitions. An OV fault in VDDQ will cause REF and VTT to turn off (high-Z) also when VDDQ drops below 0.5V. Note: to reset from any fault, VCCA or EN/PSV must be toggled.

VTT: when the output exceeds 12% of its set voltage the output is latched in a tri-stated condition (high-Z). The controller stays latched off until reset (see below). There is a 50µs delay built into the OV protection circuit to prevent false transitions. An OV fault in VTT will not affect VDDQ or REF. To reset VTT from a fault, VCCA or VTTEN or EN/PSV must be toggled.

Output Undervoltage Protection

VDDQ: when the output is 30% below its set voltage the output is latched in a tri-stated condition. It stays latched and the controller is latched off until reset (see below). There is a 5µs delay built into the UV protection circuit to prevent false transitions. An UV fault in VDDQ will cause REF and VTT to turn off (high-Z) also when VDDQ drops below 0.5V.

VTT: when the output is 12% below its set voltage the output is latched in a tri-stated condition (high-Z). The controller stays latched off until reset (see below). There is a 50µs delay built into the UV protection circuit to prevent false transitions. An UV fault in VTT will not affect VDDQ or REF. To reset VTT from a fault, VCCA or VTTEN or EN/PSV must be toggled.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA exceeds 3V, starting up the internal biasing. VCCA undervoltage lockout (UVLO) circuitry inhibits the whole controller until VCCA rises above 4.2V. At this time the UVLO circuitry enables the REF buffer, resets the fault latch and soft start timer, and allows switching to occur, if enabled. Switching always starts with DL to charge up the BST capacitor. With the softstart circuit (automatically) enabled, it will progressively limit the output current (by limiting the current out of the ILIM pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:
1) 110 cycles at 25% ILIM with double minimum off-time (for purposes of the on-time one-shot, there is an internal positive offset of 120mV to VOUT during this period to aid in startup)
2) 110 cycles at 50% ILIM with normal minimum off-time
3) 110 cycles at 75% ILIM with normal minimum off-time
4) 110 cycles at 100% ILIM with normal minimum off-time. At this point the output undervoltage and power good circuitry is enabled.

When VDDQ reaches 0.5V, the REF output is enabled and rises to VDDQS/2. VTT attempts to track REF but its own soft start circuitry will limit its rise rate to 6mV/µs. If VDDQ is rising slow enough, VTT will rise at 6mV/µs until it reaches VDDQ/2 and then track VDDQ.

There is 100mV of hysteresis built into the UVLO circuit and when VCCA falls to 4.1V (nom.) the output drivers are shut down and tri-stated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off (below ~1V). Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typ.). This negates the need for an external gate or boost resistor. The adaptive dead-time circuit also monitors the phase node, LX, to determine the state of the high side MOSFET, and prevents the low-side MOSFET from turning on until DH is fully off (LX below ~1V). Be sure to have low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

DDR Reference Buffer

The reference buffer is capable of driving 10mA and sinking 25µA. Since the output is class A, if additional sinking is required an external pulldown resistor can be added. Make sure that the ground side of this pulldown is tied to VSSA. As with most opamps, a small resistor is required when driving a capacitive load. To ensure stability use either a 10Ω resistor in series with a 1µF capacitor or a 100Ω resistor in series with a 0.1µF capacitor from REF to VSSA.

VTT Sink/Source Output

The VTT regulator is a sink/source LDO capable of supplying peak currents up to 3.6A. It has been designed to operate with output capacitances as low as 20µF (two 10µF 1210 ceramic capacitors). These capacitors need to be placed directly across the VTT and PGND2 pins to minimize parasitic resistance and inductance. Additional ceramic capacitors may be used to improve transient response further if desired. The VTT input requires a 1µF ceramic capacitor for bypass purposes located right at the pin. If the output capacitors for the power rail being used for VTTIN are far from the part then additional bulk capacitance of two 10µF ceramic capacitors should be added.

COMP Pin

The VTT COMP pin is provided to permit the addition of a zero into the VTT control loop by adding a resistor (less than 100Ω) between COMP and REF and a capacitor from COMP to VTTS (R7 and C3 in Figure 2). The zero frequency should be set to approximately 10 times the unity gain bandwidth, which is ~1MHz, therefore f_z should be ~10MHz. f_z is given by the following equation:

$$f_z = \frac{1}{2 \bullet \pi \bullet R \bullet C}$$

Typically this compensation will not be required, so C3 should be no-pop and R7 should be 0Ω or 10Ω.

VTTS Pin

The VTTS pin is used to kelvin sense the VTT output. An RC filter (with R from VTT to VTTS less than 100Ω and C from VTTS to VSSA, R8 and C7 in Figure 2) may be used to compensate any zeroes created by less than optimal ESR at the output. With the recommended output capacitors they are not necessary so R should be 0Ω and C should be no-pop.

Dropout Performance

VDDQ: the output voltage adjust range for continuous-conduction operation is limited by the fixed 550ns (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200kHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

VTT: the minimum input voltage allowed to be applied to VTTIN (if a supply other than VDDQ is being used) should be determined using the required maximum output current and the maximum VTT pull-up resistance, 0.45Ω. The minimum VTTIN for a given VTT and ITT can be calculated as follows:

$$VTTIN(MIN) = VTT + ITT \bullet R_{PULLUP(MAX)}$$

For example: for VTT = 0.9V out and ITT = 1.25A, VTTIN can go as low as 1.463V.

SC486 System DC Accuracy (VDDQ Controller)

Two IC parameters affect system DC accuracy, the error comparator threshold voltage variation and the switching frequency variation with line and load.

The error comparator threshold does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy. Board components and layout also influence DC accuracy. The use of 1% feedback resistors contribute 1%. If tighter DC accuracy is required use 0.1% feedback resistors.

The on-pulse in the SC486 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on-time regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the feedback resistors are chosen to divide down the output by a factor of five, the valley of the output ripple will be 2.5V. If the ripple is 50mV with VBAT = 6V, then the measured DC output will be 2.525V. If the ripple increases to 80mV with VBAT = 25V, then the measured DC output will be 2.540V.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. It will not change the frequency. Switching frequency variation with load can be minimized by choosing MOSFETs with lower $R_{DS(ON)}$. High $R_{DS(ON)}$ MOSFETs will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage.

SC486 System DC Accuracy (VTT Sink/Source LDO)

The VTT LDO is designed to track the voltage at REF, with a guaranteed DC accuracy of REF +/-20mV for -2A to +2A. Thus the DDR/DDR2 absolute requirement of +/-40mV including transients is an easy goal to achieve provided that careful attention is paid during board layout to reduce parasitic ESR/ESL.

DDR Supply Selection

The SC486 can be configured so that the VTT supply can be generated from the VDDQ supply, or from an alternate supply (usually lower to minimize power dissipation). If the VTT LDO is going to be powered from the VDDQ output, the electrical design of the VDDQ output needs to be for IDDQ(MAX) + ITT(MAX).

Design Procedure - VDDQ Controller

Prior to designing an output and making component selections, it is necessary to determine the input voltage range and the output voltage specifications. For purposes of demonstrating the procedure an 8A VDDQ output being used to power VTT at +/-2A for a total IDDQ of 10A will be designed.

The maximum input voltage ($V_{BAT(MAX)}$) is determined by the highest AC adaptor voltage. The minimum input voltage ($V_{BAT(MIN)}$) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches. For the purposes of this design example we will use a V_{BAT} range of 9V to 19.2V.

Four parameters are needed for the output:
1) nominal output voltage, V_{OUT} (for DDR2 this is 1.8V)
2) static (or DC) tolerance, TOL_{ST} (we will use +/-4% for this design)
3) transient tolerance, TOL_{TR} and size of transient (we will use +/-100mV for this design).
4) maximum output current, I_{OUT} (we are designing for 10A)

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up. The default R_{tON} value of 715kΩ is suggested as a starting point, but it is not set in stone. The first thing to do is to calculate the on-time, t_{ON}, at $V_{BAT(MIN)}$ and $V_{BAT(MAX)}$, since this depends only upon V_{BAT}, V_{OUT} and R_{tON}.

$$t_{ON\_VBAT(MIN)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{BAT(MIN)}}\right] + 50 \bullet 10^{-9} s$$

and

$$t_{ON\_VBAT(MAX)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{BAT(MAX)}}\right] + 50 \bullet 10^{-9} s$$

From these values of t_{ON} we can calculate the nominal switching frequency as follows:

$$f_{SW\_VBAT(MIN)} = \frac{V_{OUT}}{\left(V_{BAT(MIN)} \bullet t_{ON\_VBAT(MIN)}\right)} Hz$$

and

$$f_{SW\_VBAT(MAX)} = \frac{V_{OUT}}{\left(V_{BAT(MAX)} \bullet t_{ON\_VBAT(MAX)}\right)} Hz$$

t_{ON} is generated by a one-shot comparator that samples V_{BAT} via R_{tON}, converting this to a current. This current is used to charge an internal 3.3pF capacitor to V_{OUT}. The equations above reflect this along with any internal components or delays that influence t_{ON}. For our DDR2 VDDQ example we select R_{tON} = 715kΩ:

$t_{ON\_VBAT(MIN)}$ = 546ns and $t_{ON\_VBAT(MAX)}$ = 283ns

$f_{SW\_VBAT(MIN)}$ = 366kHz and $f_{SW\_VBAT(MAX)}$ = 332kHz

Now that we know t_{ON} we can calculate suitable values for the inductor. To do this we select an acceptable inductor ripple current. The calculations below assume 50% of I_{OUT} which will give us a starting place.

$$L_{VBAT(MIN)} = \left(V_{BAT(MIN)} - V_{OUT}\right) \bullet \frac{t_{ON\_VBAT(MIN)}}{\left(0.5 \bullet I_{OUT}\right)} H$$

and

$$L_{VBAT(MAX)} = \left(V_{BAT(MAX)} - V_{OUT}\right) \bullet \frac{t_{ON\_VBAT(MAX)}}{\left(0.5 \bullet I_{OUT}\right)} H$$

For our DDR2 VDDQ example:

$L_{VBAT(MIN)}$ = 0.8µH and $L_{VBAT(MAX)}$ = 1.0µH

We will select an inductor value of 1.5µH to reduce the ripple current, which can be calculated as follows:

$$I_{RIPPLE\_VBAT(MIN)} = \left(V_{BAT(MIN)} - V_{OUT}\right) \bullet \frac{t_{ON\_VBAT(MIN)}}{L} A_{P-P}$$

and

$$I_{RIPPLE\_VBAT(MAX)} = \left(V_{BAT(MAX)} - V_{OUT}\right) \bullet \frac{t_{ON\_VBAT(MAX)}}{L} A_{P-P}$$

Design Procedure (Cont.)

For our DDR2 VDDQ example:

$I_{RIPPLE\_VBAT(MIN)}$ = 2.62A_{P-P} and $I_{RIPPLE\_VBAT(MAX)}$ = 3.28A_{P-P}

From this we can calculate the minimum inductor current rating for normal operation:

$$I_{INDUCTOR(MIN)} = I_{OUT(MAX)} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2} A_{(MIN)}$$

For our DDR2 VDDQ example:

$I_{INDUCTOR(MIN)}$ = 11.6$A_{(MIN)}$

Next we will calculate the maximum output capacitor equivalent series resistance (ESR). This is determined by calculating the remaining static and transient tolerance allowances. Then the maximum ESR is the smaller of the calculated static ESR ($R_{ESR\_ST(MAX)}$) and transient ESR ($R_{ESR\_TR(MAX)}$):

$$R_{ESR\_ST(MAX)} = \frac{(ERR_{ST} - ERR_{DC}) \bullet 2}{I_{RIPPLE\_VBAT(MAX)}} Ohms$$

Where ERR_{ST} is the static output tolerance and ERR_{DC} is the DC error. The DC error will be 1% plus the tolerance of the feedback resistors, thus 2% total for 1% feedback resistors.

For our DDR2 VDDQ example:

ERR_{ST} = 72mV and ERR_{DC} = 36mV, therefore

$R_{ESR\_ST(MAX)}$ = 22mΩ

$$R_{ESR\_TR(MAX)} = \frac{(ERR_{TR} - ERR_{DC})}{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)} Ohms$$

Where ERR_{TR} is the transient output tolerance. Note that this calculation assumes that the worst case load transient is full load. For half of full load, divide the I_{OUT} term by 2.

For our DDR2 VDDQ example:

ERR_{TR} = 100mV and ERR_{DC} = 36mV, therefore

$R_{ESR\_TR(MAX)}$ = 5.5mΩ for a full 10A load transient

We will select a value of 7.5mΩ maximum for our design, which would be achieved by using two 15mΩ output capacitors in parallel.

Note that for constant-on converters there is a minimum ESR requirement for stability which can be calculated as follows:

$$R_{ESR(MIN)} = \frac{3}{2 \bullet \pi \bullet C_{OUT} \bullet f_{SW}}$$

This criteria should be checked once the output capacitance has been determined.

Now that we know the output ESR we can calculate the output ripple voltage:

$$V_{RIPPLE\_VBAT(MAX)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MAX)} V_{P-P}$$

and

$$V_{RIPPLE\_VBAT(MIN)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MIN)} V_{P-P}$$

For our DDR2 VDDQ example:

$V_{RIPPLE\_VBAT(MAX)}$ = 25mV_{P-P} and $V_{RIPPLE\_VBAT(MIN)}$ = 20mV_{P-P}

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{FB}, should be approximately 15mV_{P-P} at minimum V_{BAT}, and worst case no smaller than 10mV_{P-P}. If $V_{RIPPLE\_VBAT(MIN)}$ is less than 15mV_{P-P} the above component values should be revisited in order to improve this. A small capacitor, C_{TOP}, may be required in parallel with the top feedback resistor, R_{TOP}, in order to ensure that V_{FB} is large enough. C_{TOP} should not be greater than 100pF. The value of C_{TOP} can be calculated as follows, where R_{BOT} is the bottom feedback resistor. Firstly calculating the value of Z_{TOP} required:

$$Z_{TOP} = \frac{R_{BOT}}{0.015} \bullet (V_{RIPPLE\_VBAT(MIN)} - 0.015) Ohms$$

Design Procedure (Cont.)

Secondly calculating the value of C_{TOP} required to achieve this:

$$C_{TOP} = \frac{\left(\frac{1}{Z_{TOP}} - \frac{1}{R_{TOP}}\right)}{2 \bullet \pi \bullet f_{SW\_VBAT(MIN)}} F$$

For our DDR2 VDDQ example we will use R_{TOP} = 4.64kΩ and R_{BOT} = 23.2kΩ, therefore

$V_{FB\_VBAT(MIN)}$ = 16.7mV_{P-P} - good

No additional capacitance is required, however a no-pop space is recommended to allow for adjustment once the design is complete, laid out and built.

Next we need to calculate the minimum output capacitance required to ensure that the output voltage does not exceed the transient maximum limit, $POSLIM_{TR}$, starting from the actual static maximum, $V_{OUT\_ST\_POS}$, when a load release occurs:

$$V_{OUT\_ST\_POS} = V_{OUT} + ERR_{DC}\ V$$

For our DDR2 VDDQ example:

$V_{OUT\_ST\_POS}$ = 1.836V

$$POSLIM_{TR} = V_{OUT} \bullet TOL_{TR}\ V$$

Where TOL_{TR} is the transient tolerance. For our DDR2 VDDQ example:

$POSLIM_{TR}$ = 1.900V

The minimum output capacitance is calculated as follows:

$$C_{OUT(MIN)} = L \bullet \frac{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)^2}{\left(POSLIM_{TR}^{\ 2} - V_{OUT\_ST\_POS}^{\ 2}\right)} F$$

This calculation assumes the absolute worst case condition of a full-load to no load step transient occurring when the inductor current is at its highest. The capacitance required for smaller transient steps my be calculated by substituting the desired current for the I_{OUT} term.

For our DDR2 VDDQ example:

$C_{OUT(MIN)}$ = 839µF.

We will select 440µF, using two 220µF, 15mΩ capacitors in parallel, which will be good for load release steps of up to 6.7A.

Next we calculate the RMS input ripple current, which is largest at the minimum battery voltage:

$$I_{IN(RMS)} = \sqrt{V_{OUT} \bullet (V_{BAT(MIN)} - V_{OUT})} \bullet \frac{I_{OUT}}{V_{BAT\_MIN}} A_{RMS}$$

For our DDR2 VDDQ example:

$I_{IN(RMS)}$ = 4A_{RMS}

Input capacitors should be selected with sufficient ripple current rating for this RMS current, for example a 10µF, 1210 size, 25V ceramic capacitor can handle approximately 3A_{RMS}. Refer to manufacturer's data sheets.

Finally, we calculate the current limit resistor value. As described in the current limit section, the current limit looks at the "valley current", which is the average output current minus half the ripple current. We use the maximum room temperature specification for MOSFET $R_{DS(ON)}$ at V_{GS} = 4.5V for purposes of this calculation:

$$I_{VALLEY} = I_{OUT} - \frac{I_{RIPPLE\_VBAT(MIN)}}{2} A$$

The ripple at low battery voltage is used because we want to make sure that current limit does not occur under normal operating conditions.

$$R_{ILIM} = (I_{VALLEY} \bullet 1.2) \bullet \frac{R_{DS(ON)} \bullet 1.4}{10 \bullet 10^{-6}} Ohms$$

For our DDR2 VDDQ example $R_{DS(ON)}$ = 9mΩ:

I_{VALLEY} = 8.69A and R_{ILIM} = 13.1kΩ

We select the next lowest 1% resistor value: 13.0kΩ

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad °C$$

Where:
T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows, assuming that VTT spends 50% of its time sourcing current and 50% sinking:

$$P_D = VCCA \bullet I_{VCCA} + VDDP \bullet I_{VDDP} + V_g \bullet Q_g \bullet f + VBST \bullet 1mA \bullet D + (VTTIN - VTT) \bullet ITT \quad W$$

Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
VDDP = gate drive supply voltage (V)
I_{VDDP} = gate drive operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_g = FET gate charge, from the FET datasheet (C)
f = switching frequency (Hz)
VBST = boost pin voltage during t_{ON} (V)
D = duty cycle
VTTIN = input voltage for VTT LDO (V)
ITT = maximum VTT current (A)

Inserting the following values for $VBAT_{(MIN)}$ condition (since this is the worst case condition for power dissipation in the controller) as an example):

T_A = 85°C
θ_{JA} = 29°C/W
VCCA = VDDP = 5V
I_{VCCA} = 2500µA (data sheet maximum)
I_{VDDP} = 150µA (data sheet maximum)
V_g = 5V
Q_g = 60nC
f = 366kHz
$VBAT_{(MIN)}$ = 8V
$VBST_{(MIN)}$ = $VBAT_{(MIN)}$ +VDDP = 13V
$D_{1(MIN)}$ = 1.8/8 = 0.225
VDDQ = VTTIN = 1.8V
VTT = 0.9V
ITT = 1.2A

gives us:

$$P_D = 5 \bullet 2500e^{-6} + 5 \bullet 150e^{-6} + 5 \bullet 60e^{-9} \bullet 366e^{3} + 13 \bullet 1mA \bullet 0.225 + (1.8 - 0.9) \bullet 1.2 = 1.206 \quad W$$

and therefore:

$$T_J = 85 + 1.206 \bullet 29 = 120°C$$

As can be seen, the heating effects due to internal power dissipation are dominated by the VTT LDO, but they can be managed comfortably by the MLPQ-24 package which is heatsunk to the ground plane using 4 vias from its thermal pad.

Layout Guidelines

One (or more) ground planes is/are recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation. The IC ground reference, VSSA, should be connected to PGND1 and PGND2 as a star connection at the thermal pad, which in turn is connected using 4 vias to the ground plane. All components that are referenced to VSSA should connect to it directly on the chip side, and not through the ground plane.

VDDQ: the feedback trace must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route the feedback trace in a quiet layer if possible from the output capacitor back to the chip.
Chip supply decoupling capacitors (VCCA, VDDP) should be located next to the pins (VCCA and VSSA, VDDP and PGND1) and connected directly to them on the same side.
VTT: output capacitors should be located right across the VTT output pins (VTT and PGND2) as close as possible to the part to minimize parasitics.

The switcher power section should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the connections on one side of the PCB using wide copper filled areas if possible. Do not use “minimum” land patterns for power components. Minimize trace lengths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses), the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitics) if routed on more than one layer. Current sense connections must always be made using Kelvin connections to ensure an accurate signal.

We will examine the SC486 DDR2 reference design used in the Design Procedure section while explaining the layout guidelines in more detail.

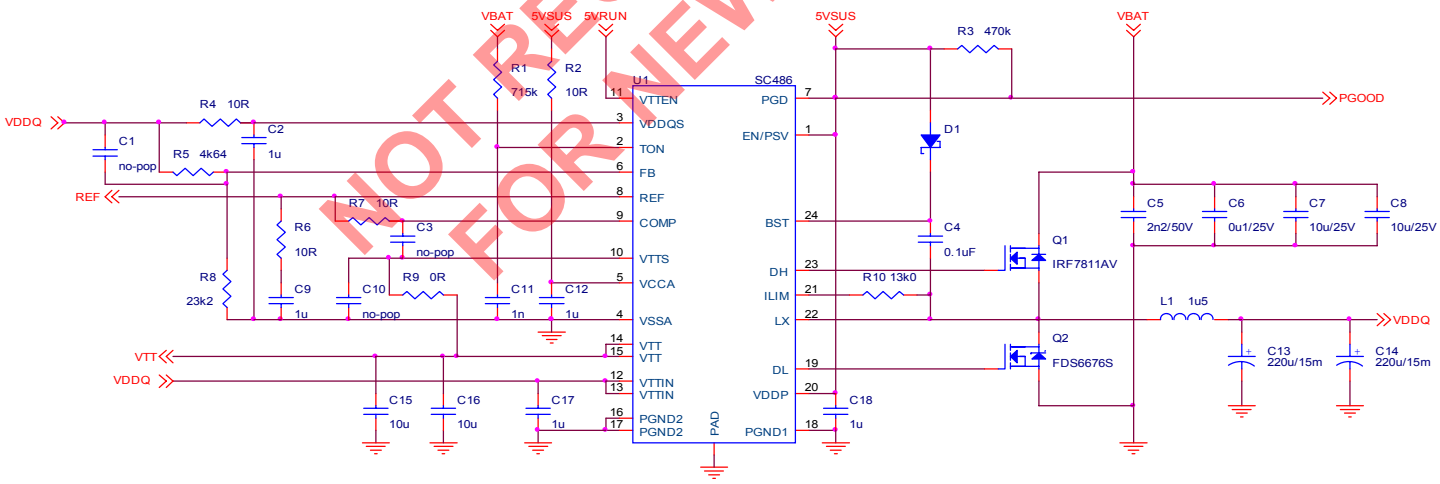


Figure 4: DDR2 Reference Design and Layout Example

Sample DDR2 Design Using SC486
VBAT = 9V to 19.2V
VDDQ = 1.8V @ (8+2)A
VTT = 0.9V @ 2A

Layout Guidelines (Cont.)

The layout can be considered in three parts, the control section referenced to VSSA, the VTT output, and the switcher power section. Looking at the control section first, locate all components referenced to VSSA1 on the schematic and place these components at the chip. Connect VSSA using a wide (>0.020") trace. Very little current flows in the chip ground therefore large areas of copper are not needed. Connect the VSSA pin directly to the thermal pad under the device as the only connection to PGND from VSSA.

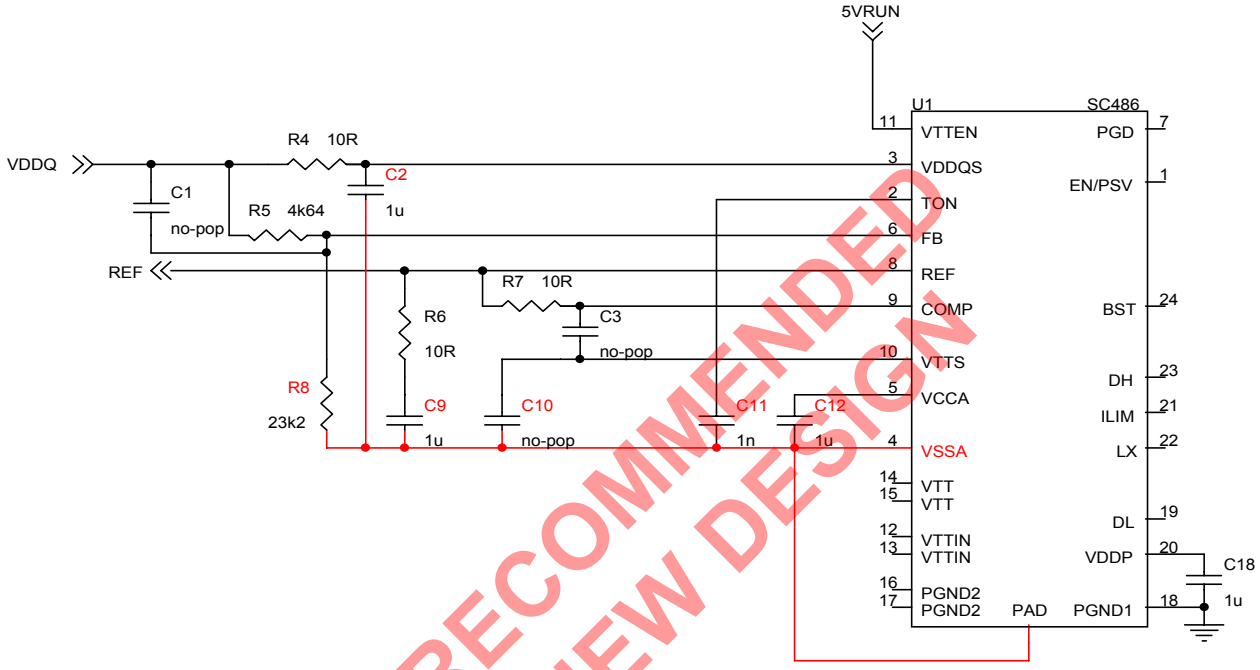


Figure 7: Components Connected to VSSA

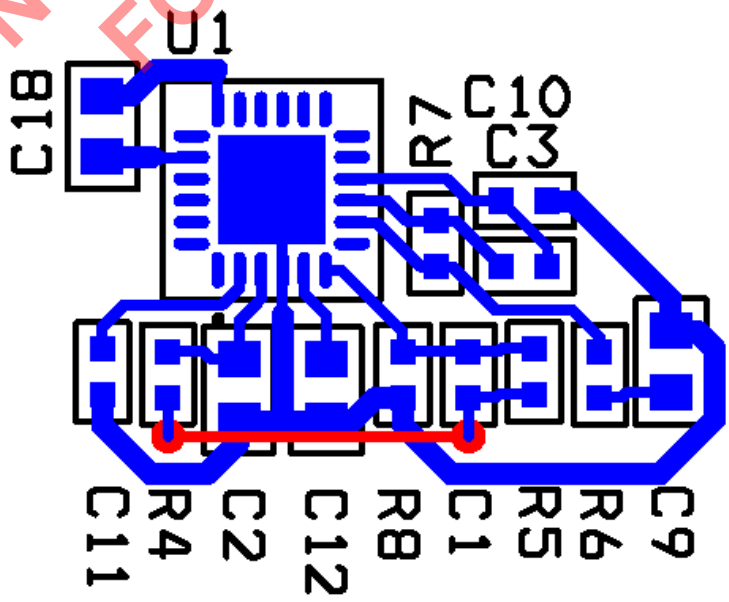


Figure 8: Example VSSA 0.020" Trace

Layout Guidelines (Cont.)

In Figure 8, all components referenced to VSSA have been placed and have been connected using a 0.020" trace. Decoupling capacitor C12 is as close as possible to VCCA and VSSA and the VDDP decoupling capacitor C18 is as close as possible to VDDP and PGND1. The feedback components R5, R8 and C1 along with the VDDQ sense components, R4 and C2 are also located at the chip and the feedback trace from the VDDQ output should route from the top of the output capacitors (C13 and C14) in a quiet layer back to these components. In Figure 8, the VDDQ feedback trace would connect to the red trace.

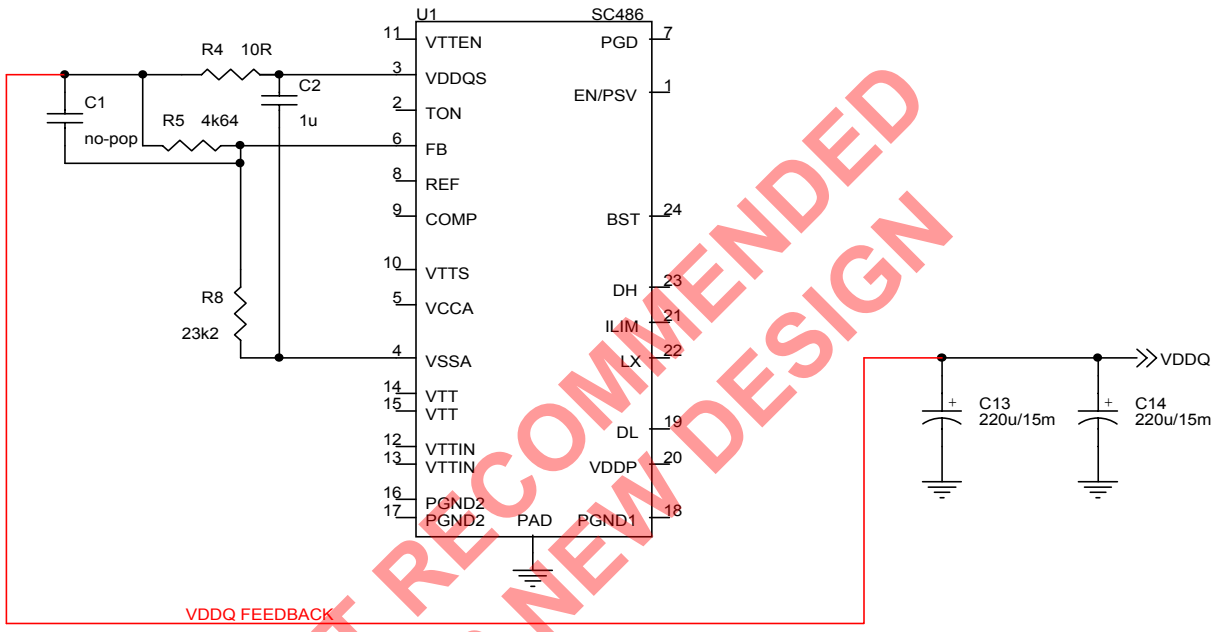


Figure 9: VDDQ Feedback and Sense Components and Feedback Trace

Layout Guidelines (Cont.)

Next, looking at the switcher power section, the schematic in Figure 10 below shows the power section for VDDQ:

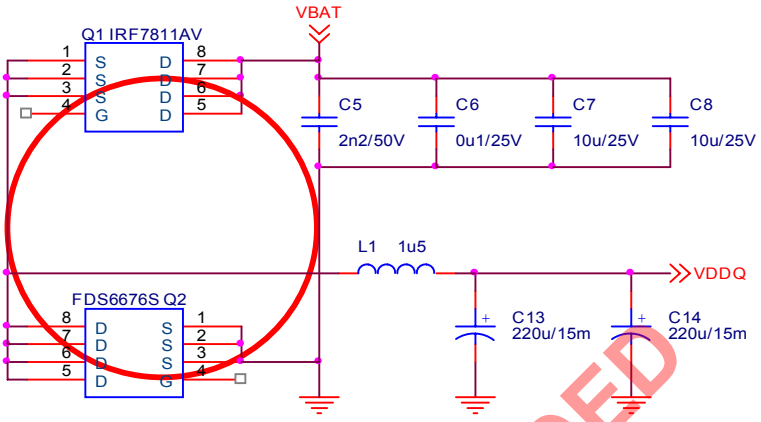


Figure 10: VDDQ Power Section and Input Loop

The highest di/dts occur in the input loop (highlighted in red) and thus this should be kept as small as possible. The input capacitors should be placed with the highest frequency capacitors closest to the loop to reduce EMI. Use large copper pours to minimize losses and parasitics. See Figure 11 below for an example.

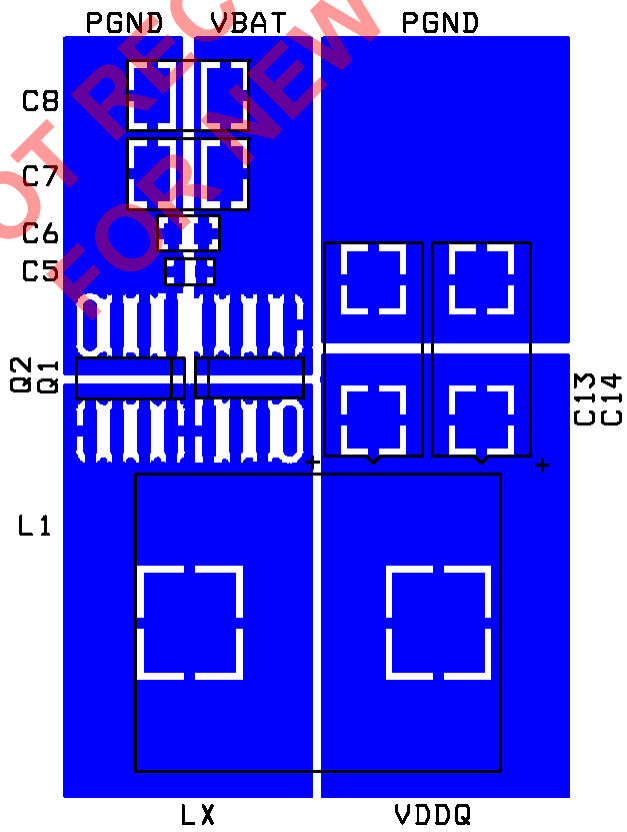


Figure 11: Example VDDQ Power Section Layout

Layout Guidelines (Cont.)

Key points for the switcher power section:

1) there should be a very small input loop, well decoupled.
2) the phase node should be a large copper pour, but compact since this is the noisiest node.
3) input power ground and output power ground should not connect directly, but through the ground planes instead.

Connecting the control and switcher power sections should be accomplished as follows (see Figure 12 below):

1) Route VDDQ feedback trace in a “quiet” layer away from noise sources.
2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to chip using wide traces with multiple vias if using more than one layer. These connections are to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power ground as its return path. LX is the noisiest node in the circuit, switching between VBAT and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path.
3) BST is also a noisy node and should be kept as short as possible.
4) Connect PGND pins on the chip directly to the VDDP decoupling capacitor and then drop vias directly to the ground plane.

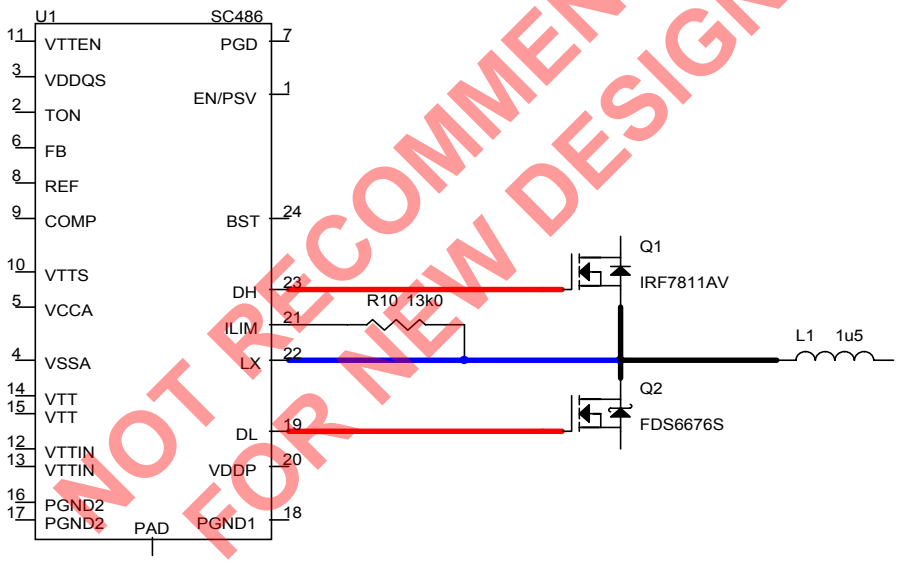


Figure 12: Connecting Control and Switcher Power Sections

Phase nodes (black) to be copper islands (preferred) or wide copper traces. Gate drive traces (red) and phase node traces (blue) to be wide copper traces (L:W < 20:1) and as short as possible, with DL the most critical. Use multiple vias when switching between layers. Locate the current limit resistor (R10) at the chip with a kelvin connection to the phase node.

Layout Guidelines (Cont.)

Next looking at the VTT output:

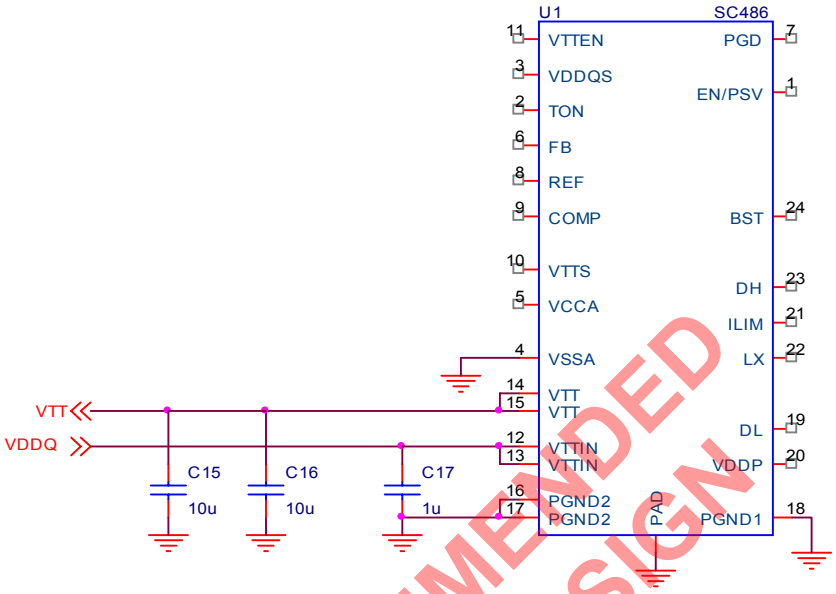


Figure 13: VTT Output

The output capacitors should be connected right at the chip, on the same side as the chip and right across the pins. The input capacitor may be placed on the opposite side, if desired. See Figure 14 below:

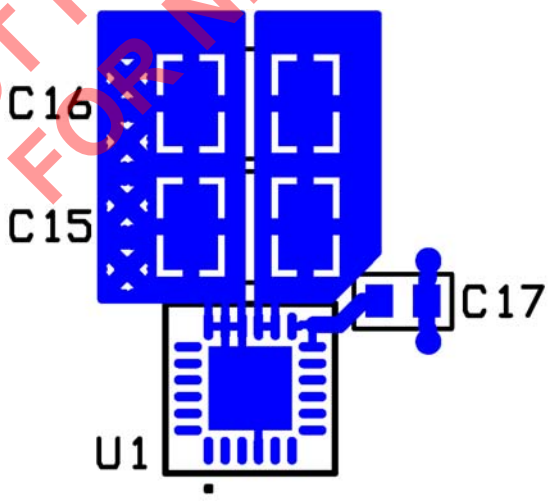
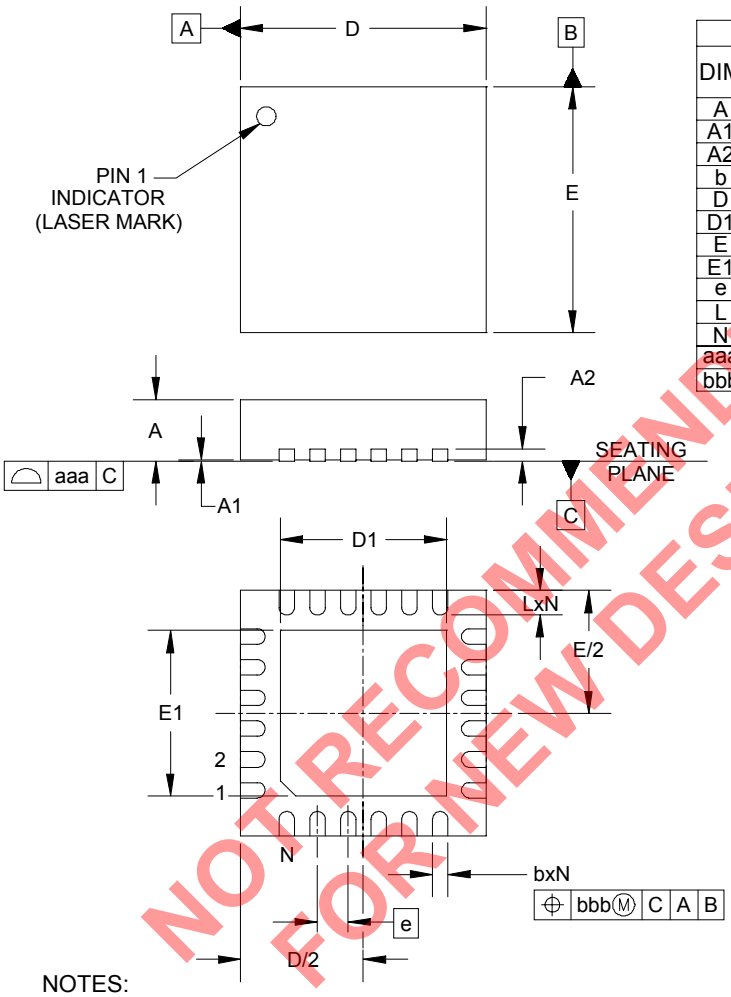


Figure 14: Example VTT Output Component Placement and Starred Ground

Output capacitors C15 and C16 are placed across the device pins, and connect to the ground plane using multiple vias. Input capacitor C17 connects directly to the device pins and connects to the ground plane using two vias. Note that PGND1, PGND2 and VSSA all connect to the pad under the device, which should also connect to the ground plane using multiple vias.

Outline Drawing - MLPQ-24 (4 x 4mm)

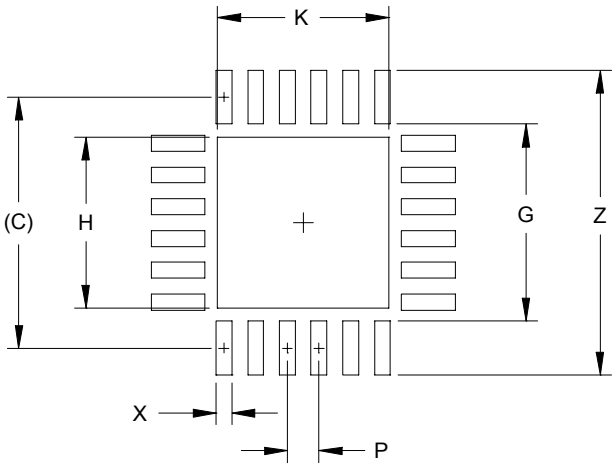


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.039	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.152	.157	.163	3.85	4.00	4.15
D1	.100	.106	.110	2.55	2.70	2.80
E	.152	.157	.163	3.85	4.00	4.15
E1	.100	.106	.110	2.55	2.70	2.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	24			24		
aaa	.004			0.10		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPQ-24 (4 x 4mm)



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.156)	(3.95)
G	.122	3.10
H	.106	2.70
K	.106	2.70
P	.020	0.50
X	.010	0.25
Y	.033	0.85
Z	.189	4.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804