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NTE3881
Integrated Circuit
NMOS, Parallel I/O Interface (PIO), 4MHz

Description:

The NTE3881 Parallel I/O Circuit (PIO) is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the NTE3880. The Central Processing Unit (CPU) can configure the NTE3881 to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the NTE3881 include most keyboard, paper tape readers and punches, printers, PROM programmers, etc. The NTE3881 utilizes N channel silicon gate depletion load technology and is packaged in a 40–Lead DIP type package.

Features:

- Two Independent 8–Bit Bidirectional Peripheral Interface Ports with “Handshake” Data Transfer Control
- Interrupt Driven “Handshake” for Fast Response
- Any One of Four Distinct Modes of Operation may be Selected for a Port, including:
  - Byte Output
  - Byte Input
  - Byte Bidirectional Bus (Available on Port A Only)
  - Bit Control Mode
- All with Interrupt Controlled Handshake
- Daisy Chain Priority Interrupt Logic Included to Provide for Automatic Interrupt Vectoring without External Logic
- Eight Outputs are Capable of Driving Darlington Transistors
- All Inputs and Outputs Fully TTL Compatible
- Single 5 Volt Supply and Single Phase Clock Required

Absolute Maximum Ratings:

Temperature Under Bias . . . . . 0° to +70°C
Storage Temperature Range . . . . . –65° to +150°C
Voltage On Any Pin With Respect to GND . . . . . –0.3V to +7V
Power Dissipation 6W

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics: (T_A = 0° to 70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Input Low Voltage	V_{ILC}		–0.3	–	0.80	V
Clock Input High Voltage	V_{IHC}		V_{CC}–0.6	–	V_{CC}+3	V
Input Low Voltage	V_{IL}		–0.3	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –250µA	2.4	–	–	V
Power Supply Current	I_{CC}		–	–	70	mA
Input Leakage Current	I_{L1}	V_{IN} = 0 to V_{CC}	–	–	±10	µA
Tri–State Output Leakage Current in Float	I_{LOH}	V_{OUT} = 2.4 to V_{CC}	–	–	10	µA
Tri–State Output Leakage Current in Float	I_{LOL}	V_{OUT} = 0.4V	–	–	–10	µA
Data Bus Leakage Current in Input Mode	I_{LD}	$0 \le V_{IN} \le V_{CC}$	–	–	±10	µA
Darlington Drive Current	I_{OHD}	V_{OH} = 1.5V Port B Only	–1.5	–	–	mA

Capacitance: (T_A = +25°C, f = 1MHz unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Capacitance	C_ϕ	Unmeasured Pins	–	–	10	pF
Input Capacitance	C_{IN}	Input Capacitance	–	–	5	pF
Output Capacitance	C_{OUT}		–	–	10	pF

AC Characteristics: (T_A = 0° to 70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Cycle Time	TcC	Note 1	250	–	–	ns
Clock Width (High)	TcCH		105	–	2000	ns
Clock Width (Low)	TcCL		105	–	2000	ns
Clock Fall Time	TfC		–	–	30	ns
Clock Rise Time	TrC		–	–	30	ns
$\overline{CE}$, B/$\overline{A}$, C/E, to $\overline{RD}$, $\overline{IORQ}$ ↓ Setup Time	TsCS(RI)	Note 2	50	–	–	ns
Any Hold Time for Specified Setup Time	Th		0	–	–	ns
$\overline{RD}$, $\overline{IORQ}$ to Clock ↑ Setup Time	TsRI(C)		115	–	–	ns
$\overline{RD}$, $\overline{IORQ}$ ↓ to Data Out Delay	TdRI(DO)	Note 3	–	–	380	ns
$\overline{RD}$, $\overline{IORQ}$ ↑ to Data Out Float Delay	TdRI(DOr)		–	–	110	ns
Data In to Clock ↑ Setup Time	TsDI(C)	C_L = 50pF	50	–	–	ns
$\overline{IORQ}$ ↓ to Data Out Delay (INTA Cycle)	TdIO(DOI)	Note 4	250	–	–	ns
$\overline{M1}$ ↓ to Clock ↑ Setup Time	TsM1(Cr)		90	–	–	ns
$\overline{M1}$ ↑ to Clock ↓ Setup Time ($\overline{M1}$ Cycle)	TsM1(Cf)		0	–	–	ns

Note 1 TcC = TwCh + TwCl + TrC + TfC.

Note 2. TsCS(RI) may be reduced. However, the time subtracted from TsCS(RI) will be added to TdR(DO).

Note 3. Increase TdRI(DO) by 10ns for each 50pF increase in loading up to 200pF max.

Note 4. Increase TdIO(DOT) by 10ns for each 60pF increase in loading up to 200pF max.

AC Characteristics (Cont'd): (T_A = 0° to 70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{M1}$ ↓ to IEO ↓ Delay (Interrupt Immediately Preceding $\overline{M1}$)	TdM1(IEO)	Note 5, Note 6	–	–	190	ns
IEI to $\overline{IORQ}$ ↓ Setup Time (INTA Cycle)	TsIE(IO)	Note 6	140	–	–	ns
IEI ↓ to IEO ↓ Delay	TdIEI(IEO)	C_L = 50pF, Note 5	–	–	130	ns
IEI ↑ to IEO ↑ Delay (after ED Decode)	TdIE(IIOr)	Note 5	–	–	160	ns
$\overline{IORQ}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	TsIO(C)		220	–	–	ns
Clock ↓ to Ready ↑ Delay	TdC(RDYr)	C_L = 50pF, Note 5	200	–	–	ns
Clock ↓ to Ready ↓ Delay	TdC(RDYf)	Note 5	150	–	–	ns
$\overline{STROBE}$ Pulse Width	TwSTB	Note 4	150	–	–	ns
$\overline{STROBE}$ ↑ to Clock ↓ Setup Time (To Activate READY on Next Clock Cycle)	TsSTB(C)		200	–	–	ns
$\overline{IORQ}$ ↑ to PORT Data Stable Delay (Mode 0)	TdIO(PD)	Note 5	–	–	180	ns
PORT DATA to $\overline{STROBE}$ ↑ Setup Time (Mode 1)	TsPD(STB)		230	–	–	ns
$\overline{STROBE}$ ↓ to PORT DATA Stable (Mode 2)	TdSTB(PD)	Note 5	–	–	210	ns
$\overline{STROBE}$ ↑ to PORT DATA Float Delay (Mode 2)	TdSTB(PDz)	C_L = 50pF	–	–	180	ns
PORT DATA Match to $\overline{INT}$ ↓ Delay (Mode 3)	TdPD(INT)		–	–	490	ns
$\overline{STROBE}$ ↑ to $\overline{INT}$ ↓ Delay	TdSTB(INT)		–	–	440	ns

Note 4 For Mode 2: $t_{W(ST)} > t_{S(PD)}$

Note 5 Increase these values by 2nsec for each 10pF increase in loading up to 100pF max.

Note 6. 2.5 TcC > (N–2) TdIEI (IEOG) + Td$\overline{M1}$(IEO) + TsIE(IO) + TTL Buffer Delay, if any.

Pin Connection Diagram