National Semiconductor

February 1995

MM5452/MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 ½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram

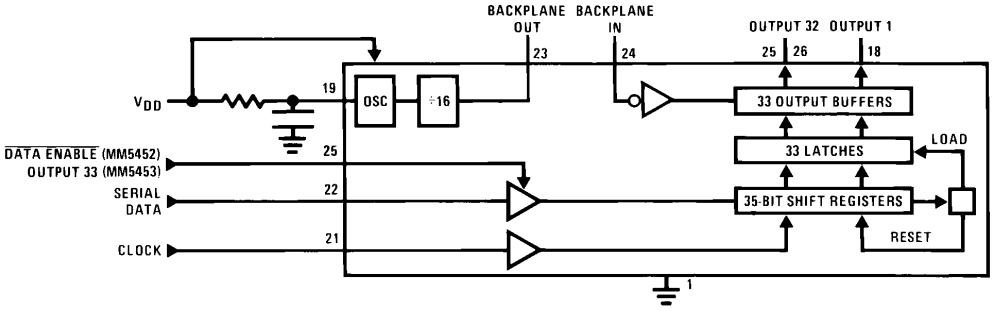

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FIGURE 1

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  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	V_{SS} to V_{SS} + 10V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	300 mW at +70°C 350 mW at +25°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

T_A within operating range, V_{DD} = 3.0V to 10V, V_{SS} = 0V, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs				
	OSC = V_{SS}, BP IN @ 32 Hz			40	μA
	V_{DD} = 5V, Open Outputs, No Clock			10	μA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	V_{DD} < 4.75	−0.3		0.1 V_{DD}	V
	V_{DD} ≥ 4.75	−0.3		0.8	V
Logical '1' Level	V_{DD} > 5.25	0.8 V_{DD}		V_{DD}	V
	V_{DD} ≤ 5.25	2.0		V_{DD}	V
Output Current Levels					
Segments					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−20	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	20			μA
Backplane					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			−320	μA
Source	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.3V	320			μA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF (Note 1)			±50	mV
Clock Input Frequency, f_C	(Notes 2 and 3)			500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input		100			ns
Set-Up Time, t_{DES}					

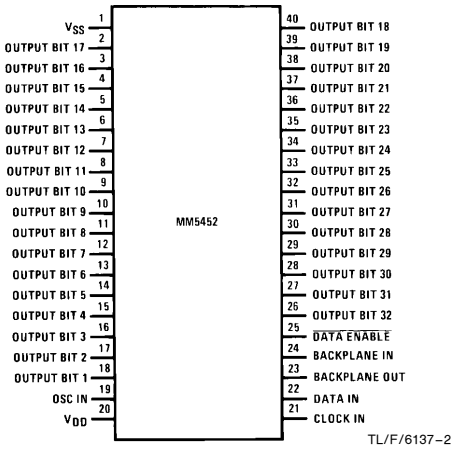
Note 1: This parameter is guaranteed (not 100% production tested) over operating temperature and supply voltage ranges. Not to be used in Q.A. testing.

Note 2: AC input waveform for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ±10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 300 ns.

Connection Diagrams

Dual-In-Line Package



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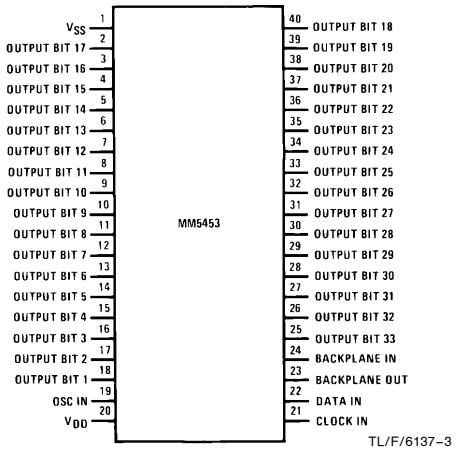
Top View
FIGURE 2a

Dual-In-Line Package



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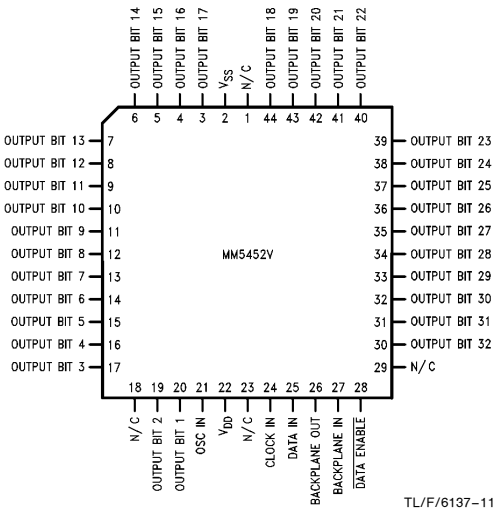
Top View
FIGURE 2b

Plastic Chip Carrier



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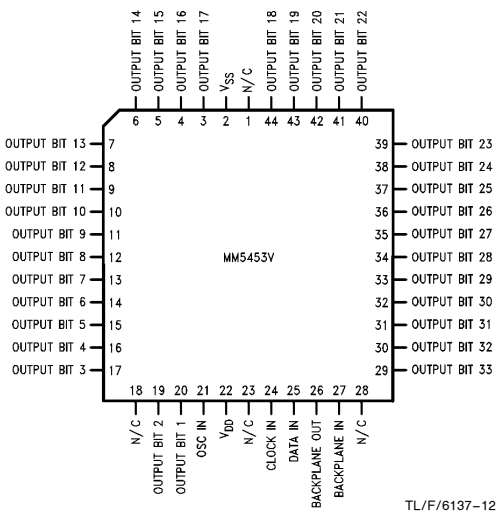
Top View

Plastic Chip Carrier



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Top View

Order Number MM5452N, MM5453N,
MM5452V or MM5453V
See NS Package Number N40A or V44A

Functional Description

The MM5452 is specifically designed to operate 4 ½-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading ''1'' followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1.* For the MM5452 a $\overline{\text{DATA ENABLE}}$ is used instead of the 33rd output. If the $\overline{\text{DATA ENABLE}}$ signal is not required, the 33rd output can be brought out. This is the MM5453 device.

Functional Description (Continued)

Figure 4 shows the input data format. A start bit of logical ''1'' precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$.

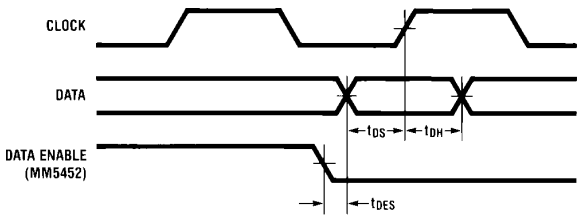

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FIGURE 3

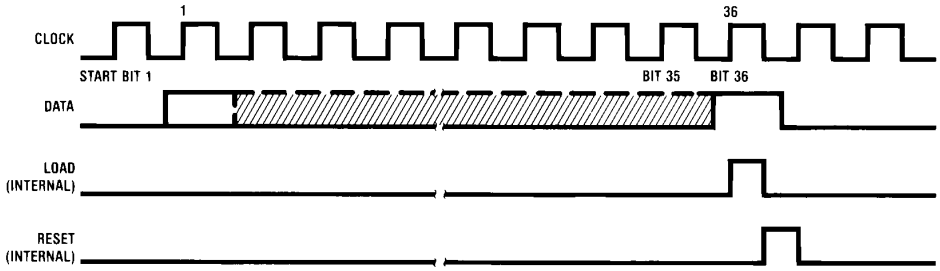

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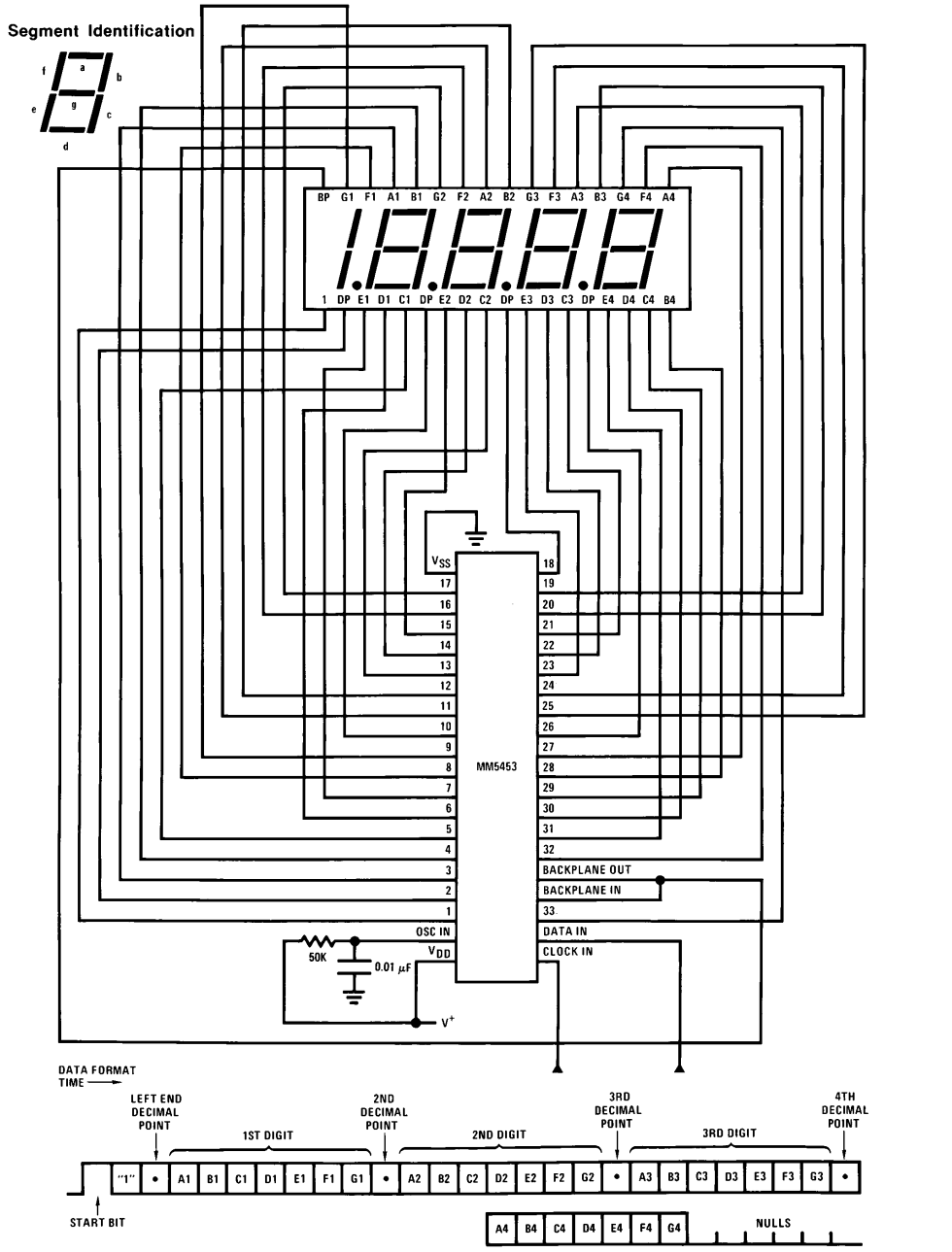
FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.



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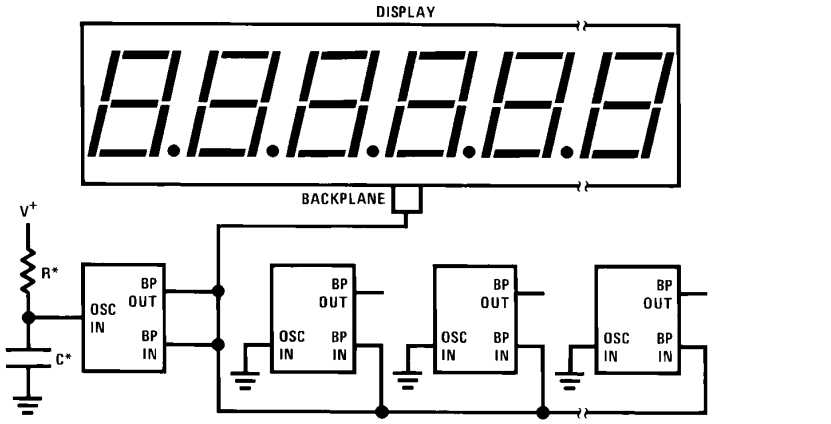
Consult LCD manufacturer's data sheet for specific pinouts.

FIGURE 5. Typical 4½-Digit Display Application

Functional Description (Continued)



*The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs

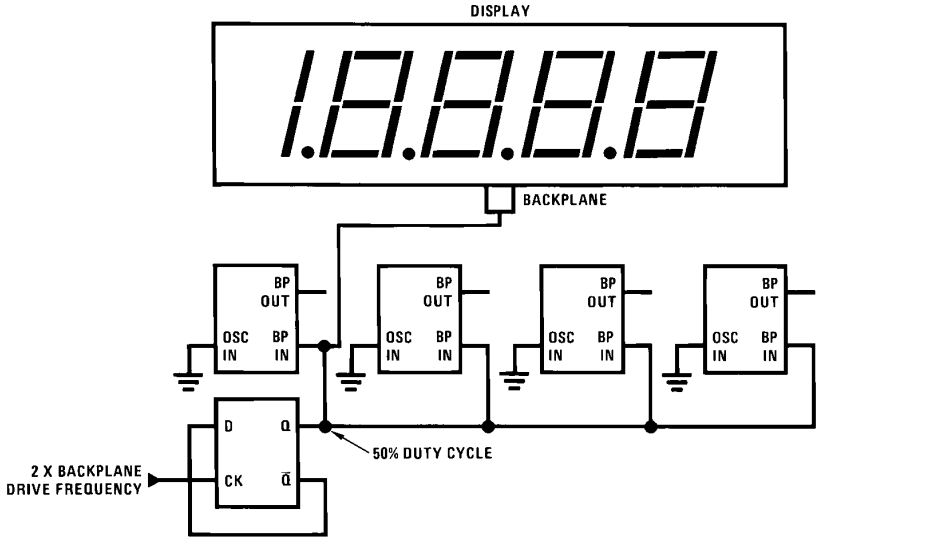


FIGURE 7. External Backplane Clock

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

USING AN EXTERNAL CLOCK

The MM5452/MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7,* a flip-flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumptions in the chips. The oscillator is not used.

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

Functional Description (Continued)

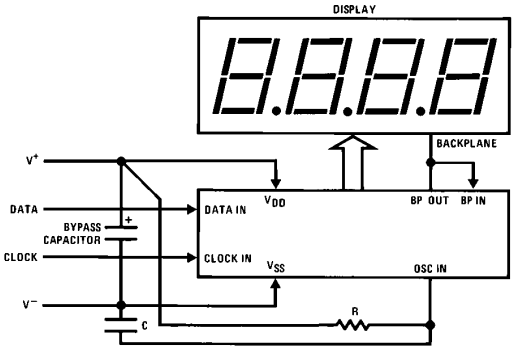


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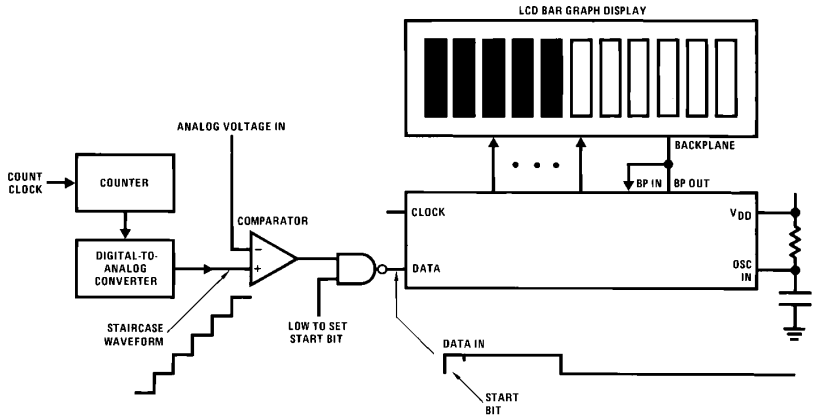
FIGURE 8. Four Wire Remote Display



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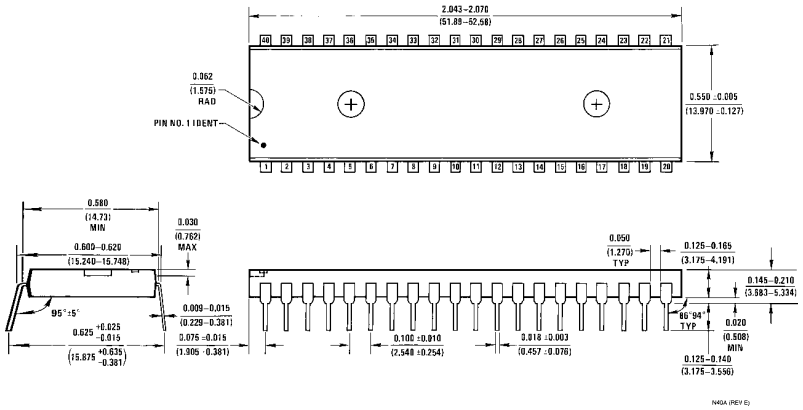
Data is high until staircase > input

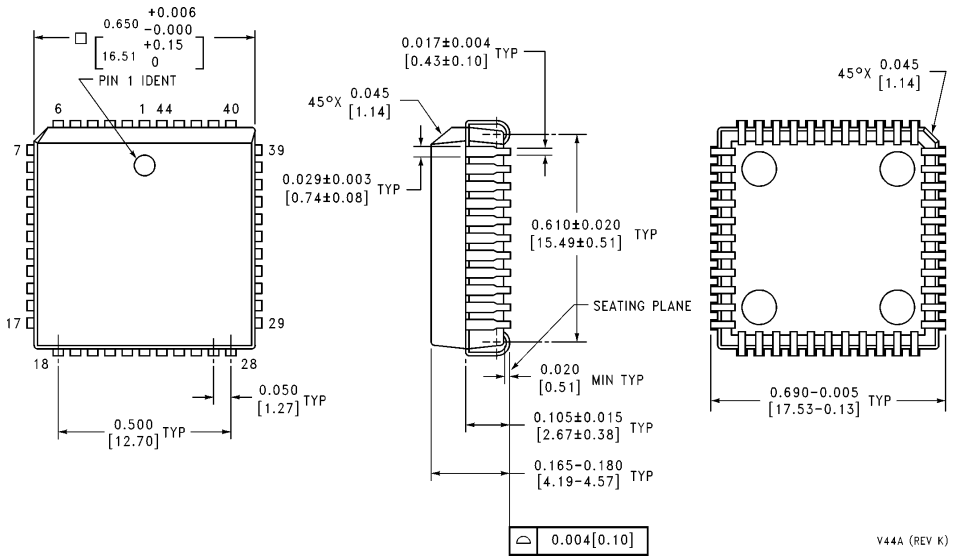
FIGURE 9. Analog Display

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number MM5452N or MM5453N
NS Package Number N40A

Physical Dimensions inches (millimeters) (Continued)



Plastic Chip Carrier (V)
Order Number MM5452V or MM5453V
NS Package Number V44A

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