14-Bit, 125 MSPS Dual TxDAC+® Digital-to-Analog Converter

AD9767

FEATURES

14-bit dual transmit DAC
125 MSPS update rate
SFDR and IMD: 82 dBc
Gain and offset matching: 0.1%
Fully independent or single resistor gain control
Dual-port or interleaved data
On-chip 1.2 V reference
5 V or 3.3 V operation
Power dissipation: 380 mW @ 5 V
Power-down mode: 50 mW @ 5 V
48-lead LQFP

APPLICATIONS

Communications
Base stations
Digital synthesis
Quadrature modulation

GENERAL DESCRIPTION

The AD9767 is a dual-port, high speed, 2-channel, 14-bit CMOS DAC. It integrates two high quality, 14-bit TxDAC+ cores, a voltage reference and digital interface circuitry into a small, 48-lead LQFP. The AD9767 offers exceptional ac and dc performance while supporting update rates up to 125 MSPS.

The AD9767 has been optimized for processing I and Q data in communications applications. The digital interface consists of two double-buffered latches as well as control logic. Separate write inputs allow data to be written to the two DAC ports independent of one another. Separate clocks control the update rate of the DACs.

A mode control pin allows the AD9767 to interface to two separate data ports, or to a single interleaved high speed data port. In interleaving mode, the input data stream is demuxed into its original I and Q data and then latched. The I and Q data is then converted by the two DACs and updated at half the input data rate.

The GAINCTRL pin allows two modes for setting the full-scale current (I_{OUTFS}) of the two DACs. I_{OUTFS} for each DAC can be set independently using two external resistors, or I_{OUTFS} for both DACs can be set by using a single external resistor. See the Gain Control Mode section for important date code information on this feature.

FUNCTIONAL BLOCK DIAGRAM

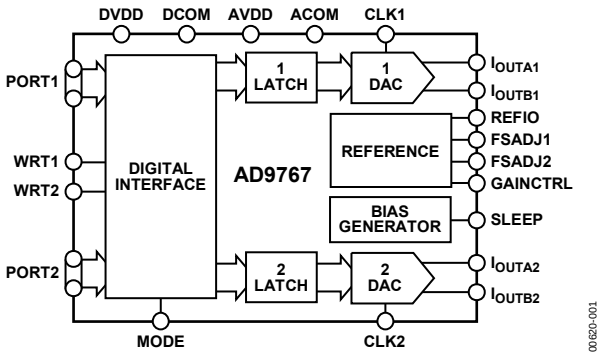

Figure 1.

The DACs utilize a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and maximize dynamic accuracy. Each DAC provides differential current output, thus supporting single-ended or differential applications. Both DACs can be simultaneously updated and can provide a nominal full-scale current of 20 mA. The full-scale currents between each DAC are matched to within 0.1%.

The AD9767 is manufactured on an advanced, low cost CMOS process. It operates from a single supply of 3.3 V to 5.0 V and consumes 380 mW of power.

PRODUCT HIGHLIGHTS

1. The AD9767 is a member of a pin-compatible family of dual TxDACs providing 8-bit, 10-bit, 12-bit, and 14-bit resolution.
2. Dual 14-Bit, 125 MSPS DACs. A pair of high performance DACs optimized for low distortion performance provide for flexible transmission of I and Q information.
3. Matching. Gain matching is typically 0.1% of full scale, and offset error is better than 0.02%.
4. Low Power. Complete CMOS dual DAC function operates on 380 mW from a 3.3 V to 5.0 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.
5. On-Chip Voltage Reference. The AD9767 includes a 1.20 V temperature-compensated band gap voltage reference.
6. Dual 14-Bit Inputs. The AD9767 features a flexible dual-port interface, allowing dual or interleaved input data.

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/06—Rev. B to Rev. C

Updated Format ... Universal
Changes to Figure 2 ... 5
Changes to Figure 3 ... 7
Changes to Functional Description Section ... 12
Changes to Figure 25 and Figure 26 ... 15
Changes to Figure 28 and Figure 29 ... 16
Changes to Power Dissipation Section ... 18
Changes to Figure 39 ... 19
Changes to Power and Grounding Considerations Section ... 19
Changes to Figure 45 ... 22
Changes to Figure 47 ... 24
Updated Outline Dimensions ... 28
Changes to Ordering Guide ... 28

2/00—Rev. A to Rev. B

12/99—Rev. 0 to Rev. A

8/99—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)				
T_A = 25°C	−3.5	±1.5	+3.5	LSB
T_{MIN} to T_{MAX}	−4.0		+4.0	LSB
Differential Nonlinearity (DNL)				
T_A = 25°C	−2.5	±1.0	+2.5	LSB
T_{MIN} to T_{MAX}	−3.0		+3.0	LSB
ANALOG OUTPUT				
Offset Error	−0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	−2	±0.25	+2	% of FSR
Gain Error (With Internal Reference)	−5	±1	+5	% of FSR
Gain Match	−1.6	±0.1	+1.6	% of FSR
	−0.14		+0.14	dB
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	−1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		± 100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3	5	5.5	V
DVDD	2.7	5	5.5	V
Analog Supply Current (I_{AVDD})		71	75	mA
Digital Supply Current (I_{DVDD})[4]		5	7	mA
Digital Supply Current (I_{DVDD})[5]			15	mA
Supply Current Sleep Mode (I_{AVDD})		8	12	mA
Power Dissipation[4] (5 V, I_{OUTFS} = 20 mA)		380	410	mW
Power Dissipation[5] (5 V, I_{OUTFS} = 20 mA)		420	450	mW
Power Dissipation[6] (5 V, I_{OUTFS} = 20 mA)		450		mW
Power Supply Rejection Ratio[7]—AVDD	−0.4		+0.4	% of FSR/V
Power Supply Rejection Ratio[7]—DVDD	−0.025		+0.025	% of FSR/V
OPERATING RANGE	−40		+85	°C

[1] Measured at I_{OUTA}, driving a virtual ground.
[2] Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[3] An external buffer amplifier with input bias current use of <100 nA should drive any external load.
[4] Measured at f_{CLK} = 25 MSPS and f_{OUT} = 1.0 MHz.
[5] Measured at f_{CLK} = 100 MSPS and f_{OUT} = 1 MHz.
[6] Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at I_{OUTA} and I_{OUTB}, f_{CLK} = 100 MSPS and f_{OUT} = 40 MHz.
[7] ±10% power-supply variation.

DYNAMIC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, differential transformer coupled output, 50 Ω doubly terminated, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLK})	125			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		35		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (90% to 10%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)		50		pA/√Hz
Output Noise (I_{OUTFS} = 2 mA)		30		pA/√Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLK} = 100 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	71	82		dBc
−6 dBFS Output		77		dBc
−12 dBFS Output		73		dBc
−18 dBFS Output		70		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 1.00 MHz		82		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 2.51 MHz		80		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 5.02 MHz		79		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 14.02 MHz		70		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 25 MHz		55		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 25 MHz		67		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 40 MHz		70		dBc
Spurious-Free Dynamic Range Within a Window				
f_{CLK} = 100 MSPS; f_{OUT} = 1.00 MHz; 2 MHz Span	82	91		dBc
f_{CLK} = 50 MSPS; f_{OUT} = 5.02 MHz; 10 MHz Span		88		dBc
f_{CLK} = 65 MSPS; f_{OUT} = 5.03 MHz; 10 MHz Span		88		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 5.04 MHz; 10 MHz Span		88		dBc
Total Harmonic Distortion				
f_{CLK} = 100 MSPS; f_{OUT} = 1.00 MHz		−81	−71	dBc
f_{CLK} = 50 MSPS; f_{OUT} = 2.00 MHz		−79		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 4.00 MHz		−83		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 10.00 MHz		−80		dBc
Multitone Power Ratio (Eight Tones at 110 kHz Spacing)				
f_{CLK} = 65 MSPS; f_{OUT} = 2.00 MHz to 2.99 MHz				
0 dBFS Output		80		dBc
−6 dBFS Output		79		dBc
−12 dBFS Output		78		dBc
−18 dBFS Output		76		dBc
Channel Isolation				
f_{CLK} = 125 MSPS; f_{OUT} = 10 MHz		85		dBc
f_{CLK} = 125 MSPS; f_{OUT} = 40 MHz		77		dBc

[1] Measured single-ended into 50 Ω load.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic 1 Voltage @ DVDD = 5 V	3.5	5		V
Logic 1 @ DVDD = 3.3 V	2.1	3		V
Logic 0 Voltage @ DVDD = 5 V		0	1.3	V
Logic 0 @ DVDD = 3.3 V	0		0.9	V
Logic 1 Current	−10		+10	µA
Logic 0 Current	−10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulse Width (t_{LPW}, t_{CPW})	3.5			ns

Timing Diagram

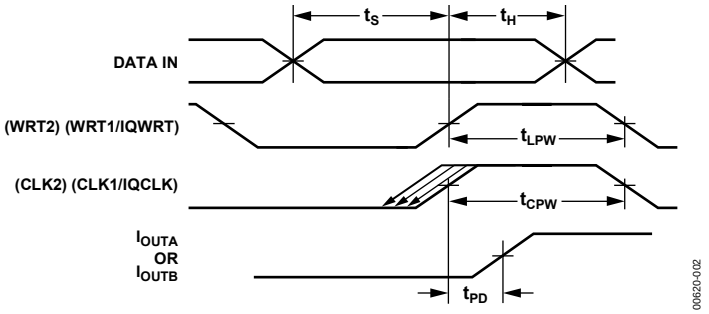

Figure 2. Timing Diagram for Dual and Interleaved Modes

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect to	Rating
AVDD	ACOM	−0.3 V to +6.5 V
DVDD	DCOM	−0.3 V to +6.5 V
ACOM	DCOM	−0.3 V to +3 V
AVDD	DVDD	−6.5 V to +6.5 V
MODE, CLK1, CLK2, WRT1, WRT2	DCOM	−0.3 V to DVDD + 0.3 V
Digital Inputs	DCOM	−0.3 V to DVDD + 0.3 V
I_{OUTA1}/I_{OUTA2}, I_{OUTB1}/I_{OUTB2}	ACOM	−1.0 V to AVDD + 0.3 V
REFIO, FSADJ1, FSADJ2	ACOM	−0.3 V to AVDD + 0.3 V
GAINCTRL, SLEEP	ACOM	−0.3 V to AVDD + 0.3 V
Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (10 sec)		300°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
48-lead LQFP	91	°C/W

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

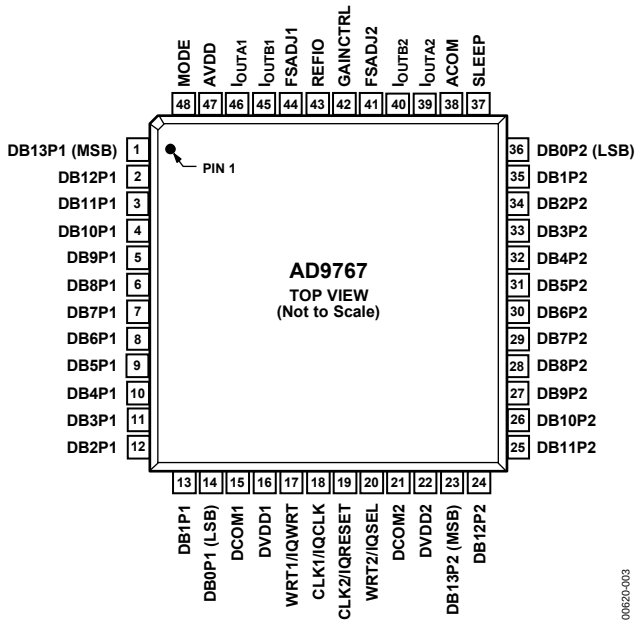

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Name	Description
1 to 14	PORT1	Data Bit DB13P1 to Data Bit DB0P1.
15, 21	DCOM1, DCOM2	Digital Common.
16, 22	DVDD1, DVDD2	Digital Supply Voltage.
17	WRT1/IQWRT	Input Write Signal for PORT 1. IQWRT in interleaving mode.
18	CLK1/IQCLK	Clock Input for DAC1. IQCLK in interleaving mode.
19	CLK2/IQRESET	Clock Input for DAC2. IQRESET in interleaving mode.
20	WRT2/IQSEL	Input Write Signal for PORT 2. IQSEL in Interleaving Mode.
23 to 36	PORT2	Data Bit DB13P2 to Data Bit DB0P2.
37	SLEEP	Power-Down Control Input.
38	ACOM	Analog Common.
39, 40	I_{OUTA2}, I_{OUTB2}	PORT 2 Differential DAC Current Outputs.
41	FSADJ2	Full-Scale Current Output Adjust for DAC2.
42	GAINCTRL	Gain Control Mode. 0 = 2 resistor, 1 = 1 resistor.
43	REFIO	Reference Input/Output.
44	FSADJ1	Full-Scale Current Output Adjust for DAC1.
45, 46	I_{OUTB1}, I_{OUTA1}	PORT 1 Differential DAC Current Outputs.
47	AVDD	Analog Supply Voltage.
48	MODE	Mode Select. 1 = dual port, 0 = interleaved.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.3 V or 5 V, DVDD = 3.3 V or 5 V, I_{OUTFS} = 20 mA, 50 Ω doubly terminated load, differential output, T_A = 25°C, SFDR up to Nyquist, unless otherwise noted.

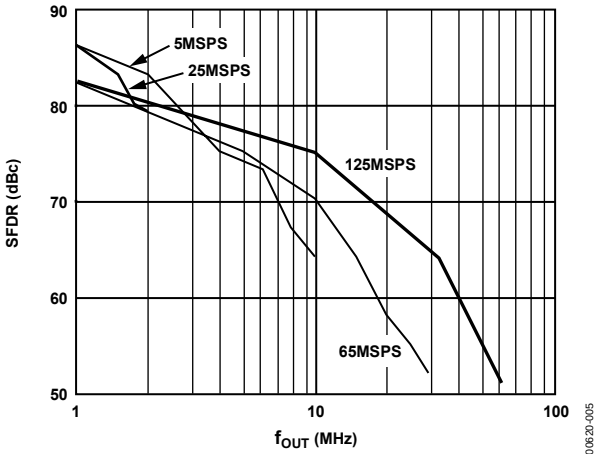

Figure 4. SFDR vs. f_{OUT} @ 0 dBFS

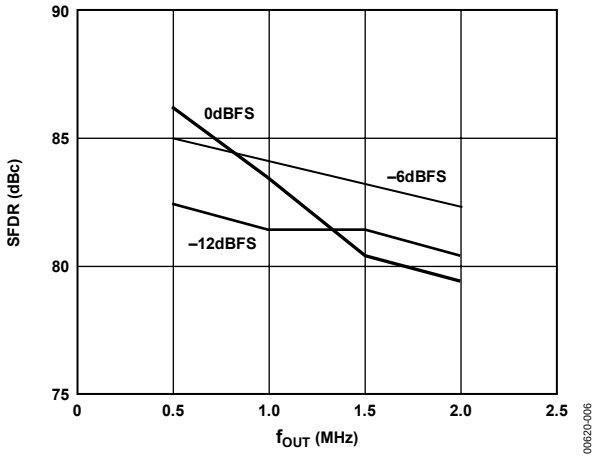

Figure 5. SFDR vs. f_{OUT} @ 5 MSPS

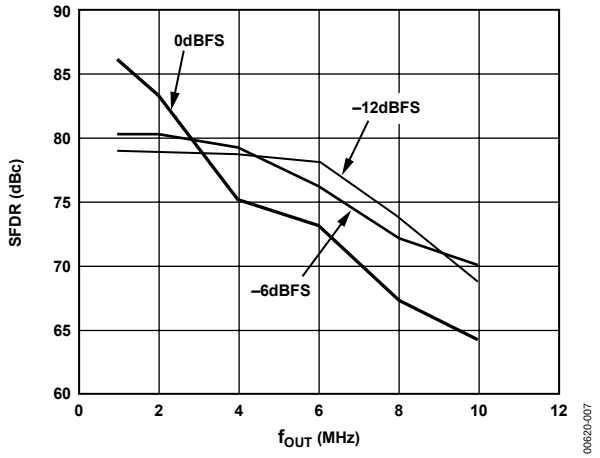

Figure 6. SFDR vs. f_{OUT} @ 25 MSPS

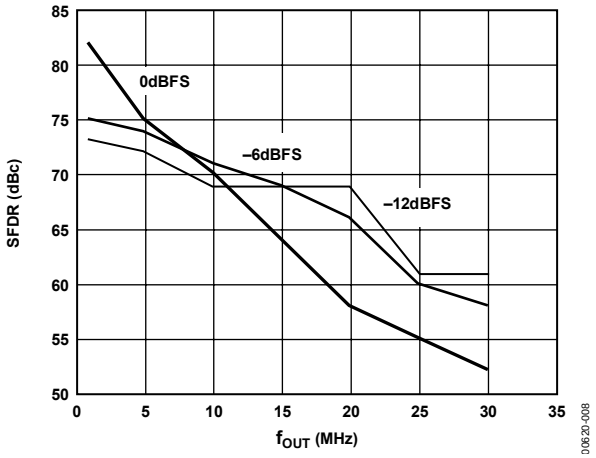

Figure 7. SFDR vs. f_{OUT} @ 65 MSPS

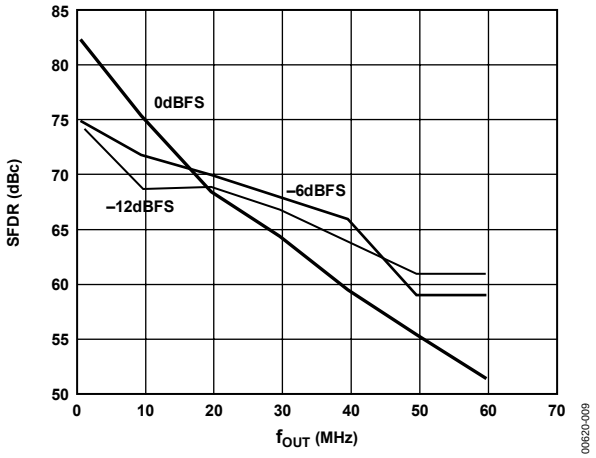

Figure 8. SFDR vs. f_{OUT} @ 125 MSPS

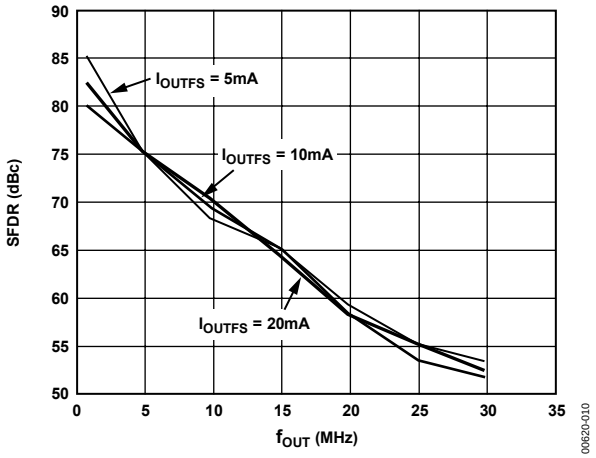

Figure 9. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

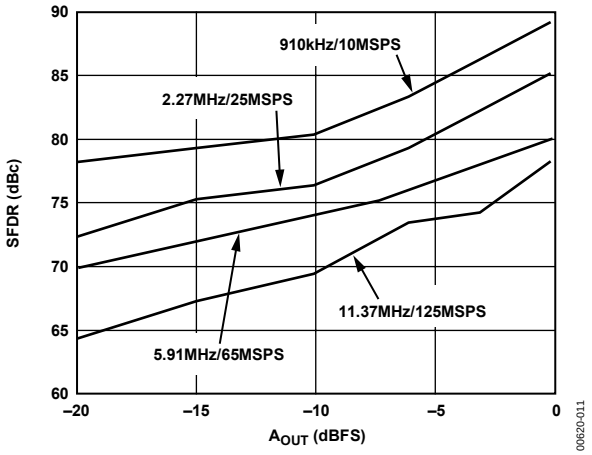

Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/11$

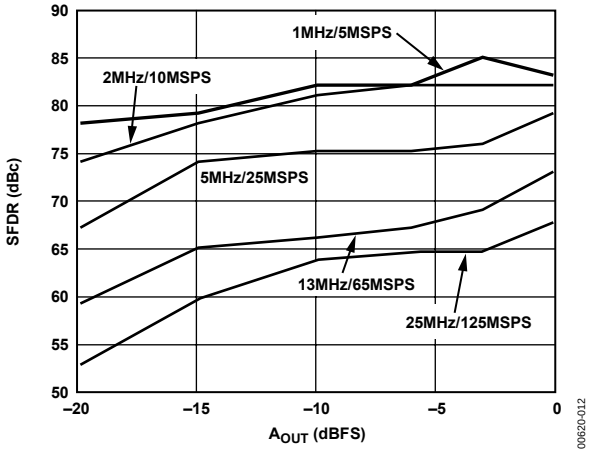

Figure 11. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/5$

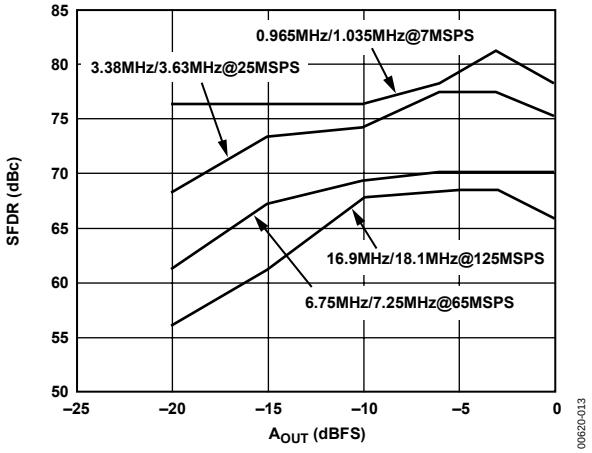

Figure 12. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLK}/7$

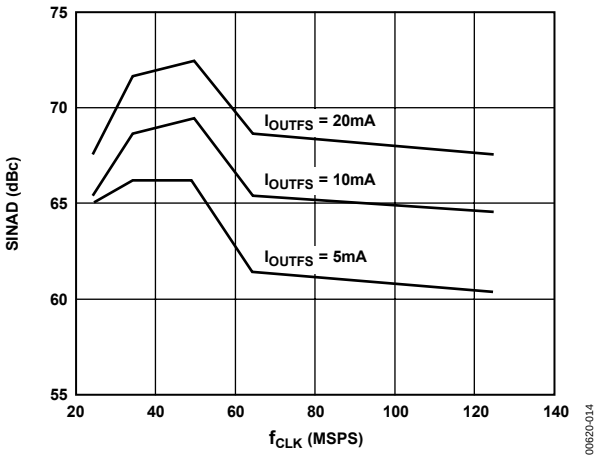

Figure 13. SINAD vs. f_{CLK} and I_{OUTFS} @ f_{OUT} = 5 MHz and 0 dBFS

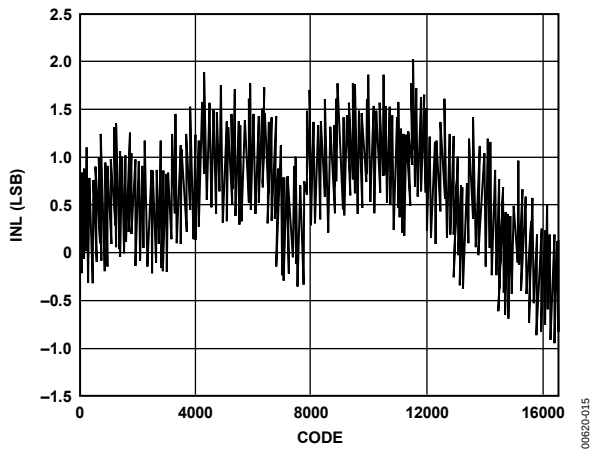

Figure 14. Typical INL

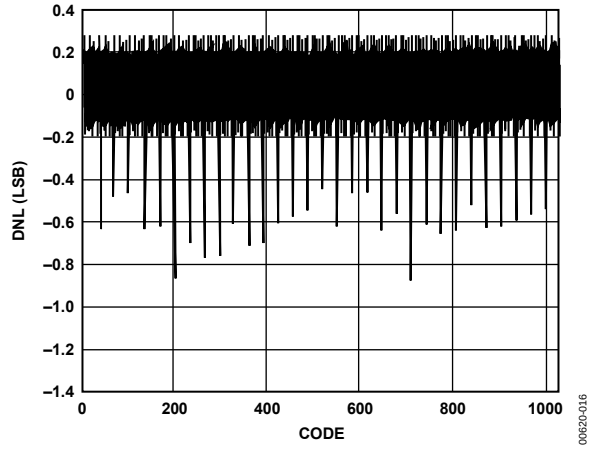

Figure 15. Typical DNL

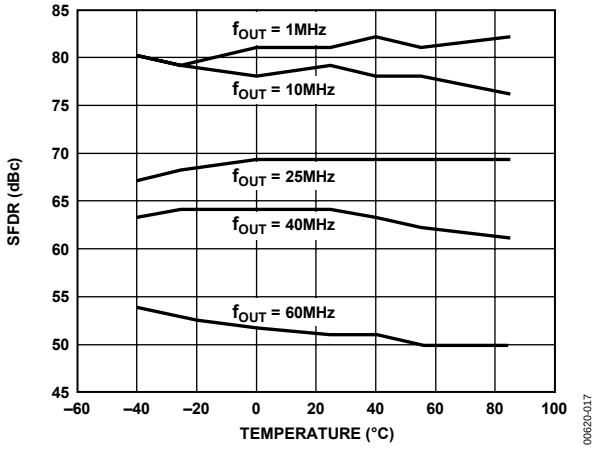

Figure 16. SFDR vs. Temperature @ 125 MSPS, 0 dBFS

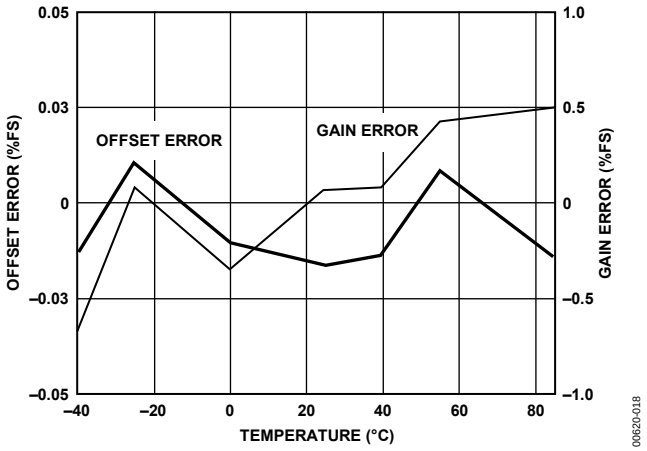

Figure 17. Reference Voltage Drift vs. Temperature

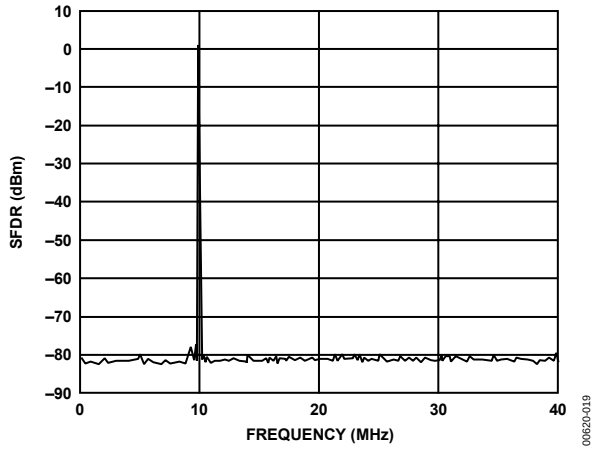

Figure 18. Single-Tone SFDR @ f_{CLK} = 125 MSPS

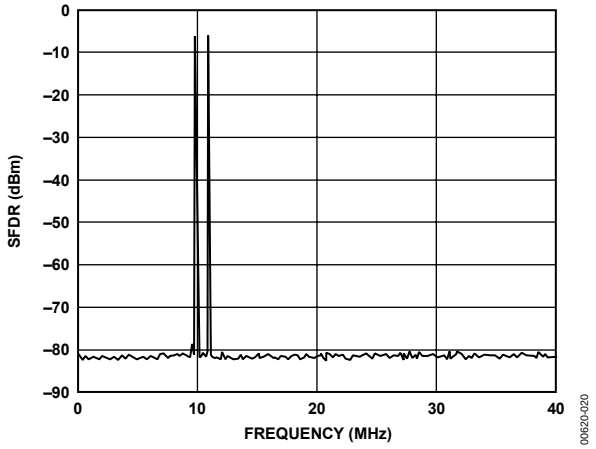

Figure 19. Dual-Tone SFDR @ f_{CLK} = 125 MSPS

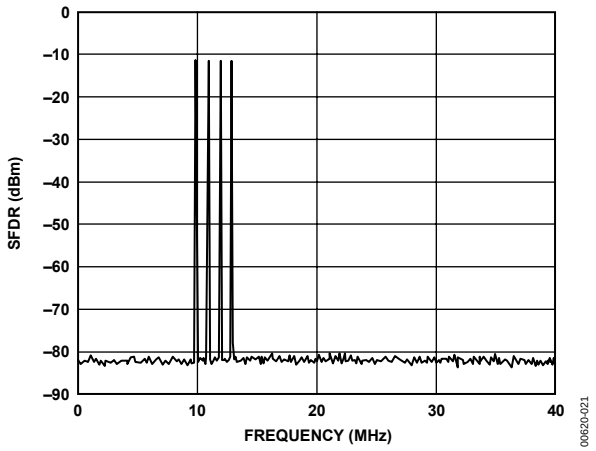

Figure 20. Four-Tone SFDR @ f_{CLK} = 125 MSPS

TERMINOLOGY

Linearity Error or Integral Nonlinearity (INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, and associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C (ppm/°C).

Power Supply Rejection (PSR)
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse, which is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

THEORY OF OPERATION

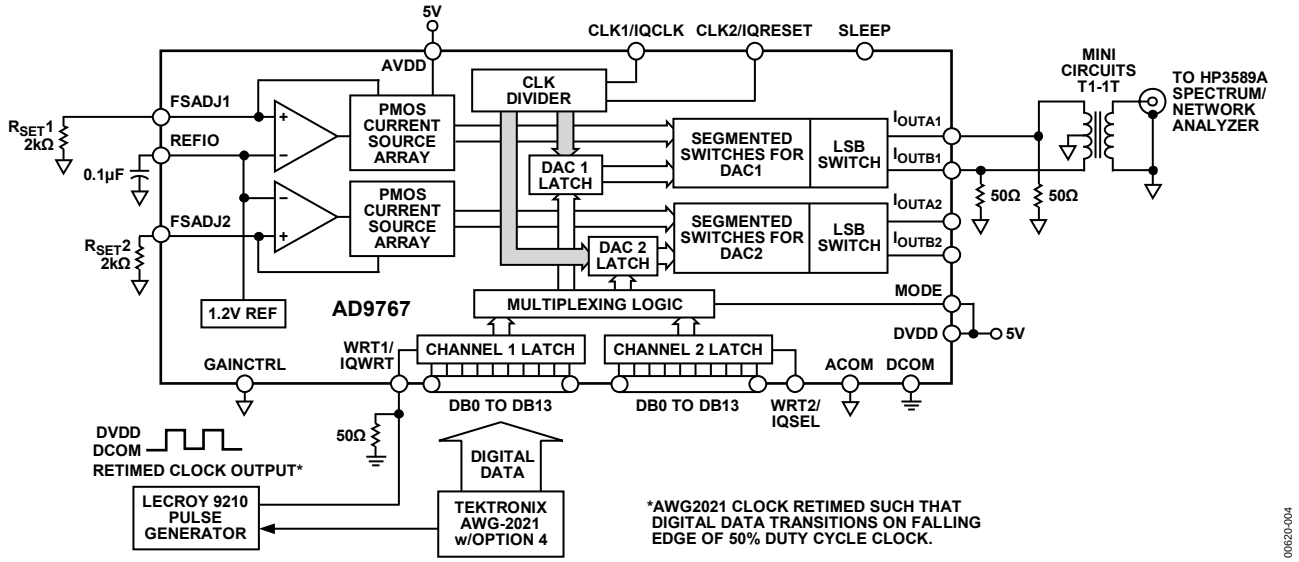

Figure 21. Basic AC Characterization Test Setup for AD9767, Testing Port 1 in Dual-Port Mode, Using Independent GAINCTRL Resistors on FSADJ1 and FSADJ2

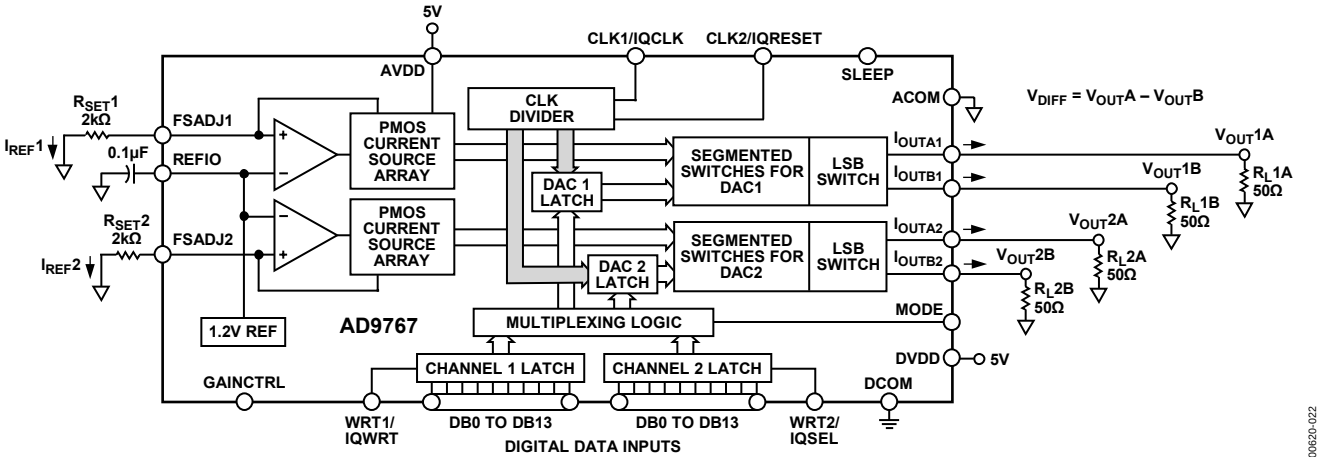

Figure 22. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 22 shows a simplified block diagram of the AD9767. The AD9767 consists of two DACs, each with its own independent digital control logic and full-scale output current control. Each DAC contains a PMOS current source array capable of providing up to 20 mA of full-scale current (I_{OUTFS}).

The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSB is a binary weighted fraction of the middle bit current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances the dynamic performance for multitone or low amplitude signals and helps maintain the DAC high output impedance (that is, >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9767 have separate power supply inputs (AVDD and DVDD) that can operate independently at 3.3 V or 5.0 V. The digital section, capable of operating up to a 125 MSPS clock rate and consists of edge triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V band gap voltage reference, and two reference control amplifiers.

The full-scale output current of each DAC is regulated by separate reference control amplifiers and can be set from 2 mA to 20 mA via an external resistor (R_{SET}), connected to the full scale adjust (FSADJ) pin. The external resistor, in combination with both the reference control amplifier and voltage reference (V_{REFIO}), sets the reference current (I_{REF}), which is replicated to the segmented current sources with the proper scaling factor. The full-scale current (I_{OUTFS}) is 32 × I_{REF}.

REFERENCE OPERATION

The AD9767 contains an internal 1.20 V band gap reference. This can easily be overridden by an external reference with no effect on performance. REFIO serves as either an input or output, depending on whether an internal or external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 µF capacitor. The internal reference voltage is present at REFIO. If the voltage at REFIO is used elsewhere in the circuit, an external buffer amplifier with an input bias current of less than 100 nA is used. An example of the use of the internal reference is shown in Figure 23.

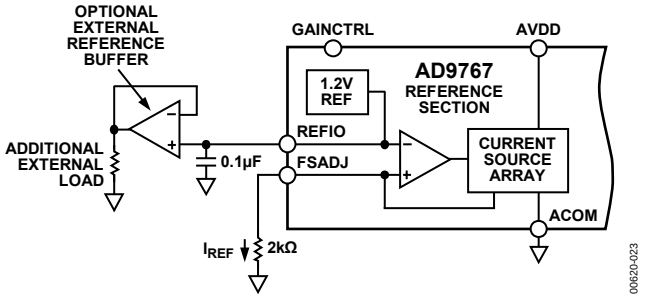

Figure 23. Internal Reference Configuration

An external reference can be applied to REFIO as shown in Figure 24. The external reference can provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. The 0.1 µF compensation capacitor is not required because the internal reference is overridden, and the relatively high input impedance of REFIO minimizes any loading of the external reference.

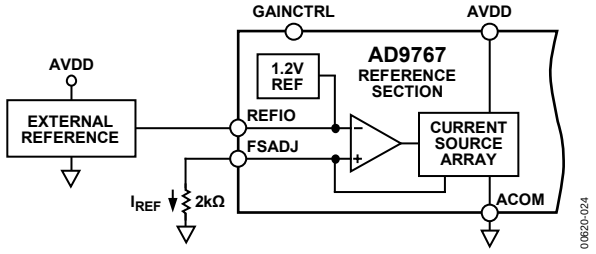

Figure 24. External Reference Configuration

GAIN CONTROL MODE

The AD9767 allows the gain of each channel to be independently set by connecting one R_{SET} resistor to FSADJ1 and another R_{SET} resistor to FSADJ2. To add flexibility and reduce system cost, a single R_{SET} resistor can be used to set the gain of both channels simultaneously.

When GAINCTRL is low (that is, connected to AGND), the independent channel gain control mode, using two resistors, is enabled. In this mode, individual R_{SET} resistors are connected to FSADJ1 and FSADJ2. When GAINCTRL is high (that is, connected to AVDD), the master/slave channel gain control mode, using one resistor, is enabled. In this mode, a single R_{SET} resistor is connected to FSADJ1, and the resistor on FSADJ2 must be removed.

Note that only parts with a date code of 9930 or later have the master/slave gain control function. For parts with a date code before 9930, Pin 42 is connected to AGND, and the part operates in the two-resistor, independent gain control mode.

REFERENCE CONTROL AMPLIFIER

Both of the DACs in the AD9767 contain a control amplifier that is used to regulate the full-scale output current (I_{OUTFS}). The control amplifier is configured as a V-I converter as shown in Figure 23, so that its current output (I_{REF}) is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scale factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} from 2 mA to 20 mA by setting I_{REF} between 62.5 µA and 625 µA. The wide adjustment range of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9767, which is proportional to I_{OUTFS} (see the Power Dissipation section). The second relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low frequency, small signal multiplying applications.

DAC TRANSFER FUNCTION

Both DACs in the AD9767 provide complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} provides a near full-scale current output (I_{OUTFS}) when all bits are high (for example, DAC CODE = 16383), while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as

$$I_{OUTA} = (DAC\ CODE/16384) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (16383 - DAC\ CODE)/16384) \times I_{OUTFS} \quad (2)$$

where *DAC CODE* = 0 to 16383 (decimal representation).

I_{OUTFS} is a function of the reference current (I_{REF}). This is nominally set by a reference voltage (V_{REFIO})and external resistor (R_{SET}). It can be expressed as

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where

$$I_{REF} = V_{REFIO}/R_{SET} \quad (4)$$

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} are directly connected to matching resistive loads (R_{LOAD}) that are tied to analog common (ACOM). Note that R_{LOAD} can represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB}, as is the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note that the full-scale value of V_{OUTA} and V_{OUTB} must not exceed the specified output compliance range to maintain specified distortion and linearity performance:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA}, I_{OUTB} and I_{REF}, V_{DIFF} can be expressed as

$$V_{DIFF} = \{(2 \times DAC\ CODE - 16383)/16384\} \times (32 \times R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

Equation 7 and Equation 8 highlight some of the advantages of operating the AD9767 differentially. First, the differential operation helps cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

The gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9767 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship, as shown in Equation 8.

ANALOG OUTPUTS

The complementary current outputs in each DAC, I_{OUTA}, and I_{OUTB}, can be configured for single-ended or differential operation. I_{OUTA} and I_{OUTB} can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor (R_{LOAD}), as described by Equation 5 through Equation 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB}, can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9767 is optimum and specified using a differential transformer coupled output in which the voltage swing at I_{OUTA} and I_{OUTB} is limited to ±0.5 V. If a single-ended unipolar output is desired, select I_{OUTA}.

The distortion and noise performance of the AD9767 can be enhanced when it is configured for differential operation. The common-mode error sources of both I_{OUTA} and I_{OUTB} can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load, assuming no source termination. Because the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer allows the AD9767 to provide the required power and voltage levels to different loads.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 kΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration results in the optimum dc linearity. Note the INL/DNL specifications for the AD9767 are measured with I_{OUTA} maintained at a virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process.

Operation beyond this maximum limit can result in a breakdown of the output stage and affect the reliability of the AD9767.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.25 V for an I_{OUTFS} = 20 mA to 1.00 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9767 output (V_{OUTA} and/or V_{OUTB}) to extend its output compliance range must size R_{LOAD} accordingly. Operation beyond this compliance range adversely affects the AD9767 linearity performance and subsequently degrades its distortion performance.

DIGITAL INPUTS

The AD9767 digital inputs consist of two channels. For the dual-port mode, each DAC has its own dedicated 14-bit data port, WRT line, and CLK line. In the interleaved timing mode, the function of the digital control pins changes as described in the Interleaved Mode Timing section. The 14-bit parallel data inputs follow straight binary coding, where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge triggered master/slave latch. The DAC outputs are updated following either the rising edge or every other rising edge of the clock, depending on whether dual or interleaved mode is being used. The DAC outputs are designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse width. The setup and hold times can be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges can affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

DAC TIMING

The AD9767 can operate in two timing modes, dual and interleaved, which are described in the following section. The block diagram in Figure 27 represents the latch architecture in the interleaved timing mode.

Dual-Port Mode Timing

When the MODE pin is at Logic 1, the AD9767 operates in dual-port mode. The AD9767 functions as two distinct DACs. Each DAC has its own completely independent digital input and control lines.

The AD9767 features a double-buffered data path. Data enters the device through the channel input latches (see Figure 21). This data is then transferred to the DAC latch in each signal path. Once the data is loaded into the DAC latch, the analog output settles to its new value. For general consideration, the WRT lines control the channel input latches and the CLK lines control the DAC latches. Both sets of latches are updated on the rising edge of their respective control signals.

The rising edge of CLK occurs before or simultaneously with the rising edge of WRT. If the rising edge of CLK occurs after the rising edge of WRT, a 2 ns minimum delay must be maintained from the rising edge of WRT to the rising edge of CLK.

Timing specifications for dual-port mode are shown in Figure 25 and Figure 26.

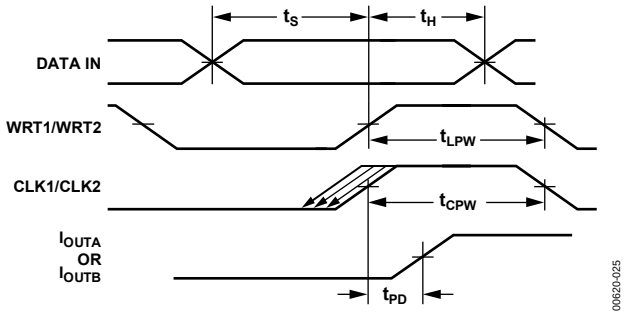

Figure 25. Dual Mode Timing

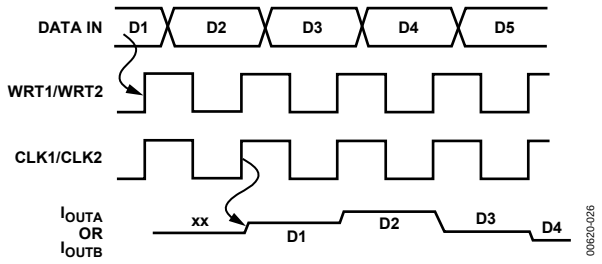

Figure 26. Dual Mode Timing

Interleaved Mode Timing

When the MODE pin is at Logic 0, the AD9767 operates in interleaved mode (see Figure 27). WRT1 now functions as IQWRT and CLK1 functions as IQCLK. WRT2 functions as IQSEL and CLK2 functions as IQRESET.

Data enters the device on the rising edge of IQWRT. The logic level of IQSEL steers the data to either Channel Latch 1 (IQSEL = 1) or to Channel Latch 2 (IQSEL = 0).

When IQRESET is high, IQCLK is disabled. When IQRESET goes low, the following rising edge on IQCLK updates both DAC latches with the data present at their inputs. In the interleaved mode, IQCLK is divided by 2 internally. Following this first rising edge, the DAC latches are updated only on every other rising edge of IQCLK. In this way, IQRESET is used to synchronize the routing of the data to the DACs.

As with the dual-port mode, IQCLK occurs before or simultaneously with IQWRT.

The digital inputs are CMOS-compatible with logic thresholds, $V_{THRESHOLD}$, set to approximately half the digital positive supply (DVDD), or

$$V_{THRESHOLD} = DVDD/2\ (\pm 20\%)$$

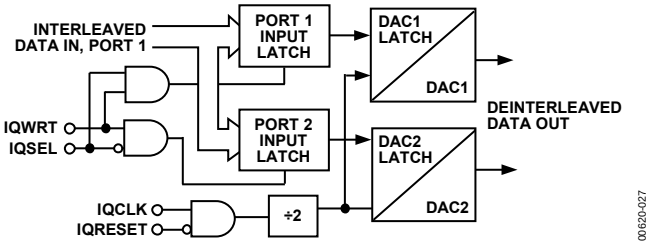

Figure 27. Latch Structure Interleaved Mode

Timing specifications for interleaved mode are shown in Figure 28 and Figure 29.

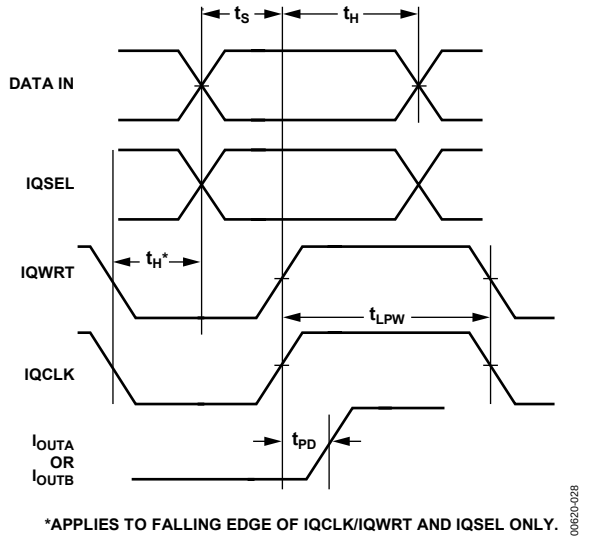

Figure 28. Interleaved Mode Timing

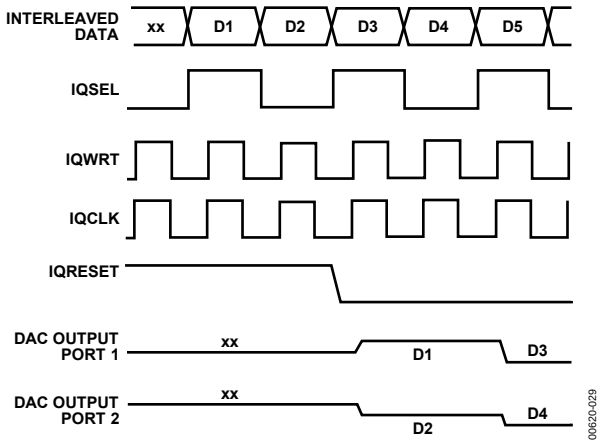

Figure 29. Interleaved Mode Timing

The internal digital circuitry of the AD9767 is capable of operating over a digital supply range of 3.3 V to 5.0 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage of the TTL drivers V_{OH} (max). A DVDD of 3 V to 3.3 V typically ensures proper compatibility with most TTL logic families. Figure 30 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar, with the exception that it contains an active pull-down circuit, thus ensuring that the AD9767 remains enabled if this input is left disconnected.

Because the AD9767 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. Operating the AD9767 with reduced logic swings and a corresponding digital supply (DVDD) results in the lowest data feedthrough and on-chip digital noise. The drivers of the digital data interface circuitry are specified to meet the minimum setup and hold times of the AD9767 as well as its required minimum/maximum input logic level thresholds.

Digital signal paths are kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value (20 Ω to 100 Ω) resistor network between the AD9767 digital inputs and driver outputs can be helpful in reducing any overshooting and ringing at the digital inputs that contribute to digital feedthrough. For longer board traces and high data update rates, stripline techniques with proper impedance and termination resistors should be considered in order to maintain clean digital inputs.

The external clock driver circuitry provides the AD9767 with a low jitter clock input meeting the minimum/maximum logic levels while providing fast edges. Fast clock edges help minimize any jitter that manifests itself as phase noise on a reconstructed waveform. Thus, the clock input is driven by the fastest logic family suitable for the application.

Note that the clock input can also be driven via a sine wave, which is centered around the digital threshold (DVDD/2) and meets the minimum/maximum logic threshold. This typically results in a slight degradation in the phase noise, which becomes more noticeable at higher sampling rates and output frequencies. In addition, at higher sampling rates, the 20% tolerance of the digital logic threshold can be considered, because it affects the effective clock duty cycle and, subsequently, cuts into the required data setup and hold times.

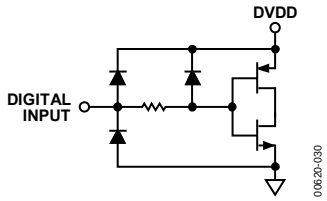

Figure 30. Equivalent Digital Input

INPUT CLOCK AND DATA TIMING RELATIONSHIP

SNR in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9767 is rising edge triggered and so exhibits SNR sensitivity when the data transition is close to this edge. The goal when applying the AD9767 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 31 shows the relationship of SNR to clock placement with different sample rates. Note that at the lower sample rates, much more tolerance is allowed in clock placement, while much more care must be taken at higher rates.

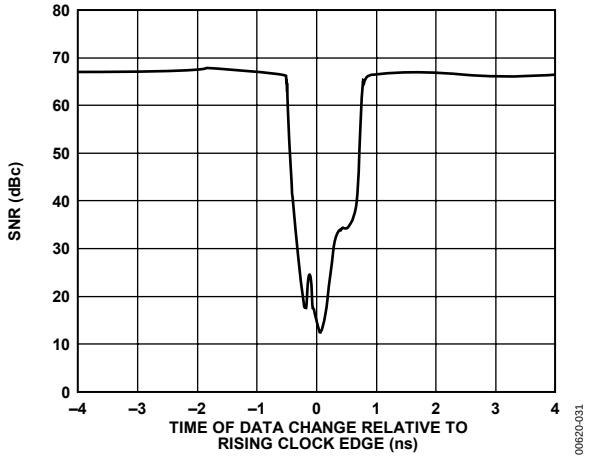

Figure 31. SNR vs. Clock Placement @ f_{OUT} = 20 MHz and f_{CLK} = 125 MSPS

Figure 32. I_{AVDD} vs. I_{OUTFS}

SLEEP MODE OPERATION

The AD9767 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the supply range of 3.3 V to 5.0 V and over the full temperature range. This mode can be activated by applying a Logic Level 1 to the SLEEP pin. The SLEEP pin logic threshold is equal to 0.5 × AVDD. This digital input also contains an active pull-down circuit that ensures the AD9767 remains enabled if this input is left disconnected. The AD9767 takes less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION

The power dissipation (P_D) of the AD9767 is dependent on several factors, including

- The power supply voltages (AVDD and DVDD)
- The full-scale current output (I_{OUTFS})
- The update rate (f_{CLK})
- The reconstructed digital input waveform

The power dissipation is directly proportional to the analog supply current (I_{AVDD}) and the digital supply current (I_{DVDD}). I_{AVDD} is directly proportional to I_{OUTFS}, as shown in Figure 32, and is insensitive to f_{CLK}.

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLK}, and digital supply DVDD. Figure 33 and Figure 34 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLK}) for various update rates with DVDD = 5 V and DVDD = 3.3 V, respectively. Note that I_{DVDD} is reduced by more than a factor of 2 when DVDD is reduced from 5 V to 3.3 V.

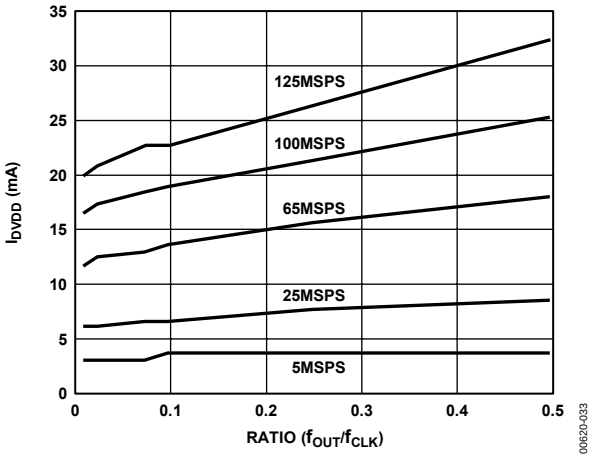

Figure 33. I_{DVDD} vs. Ratio @ DVDD = 5 V

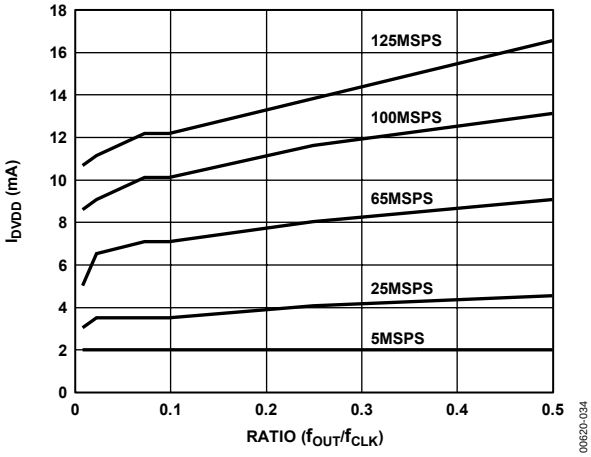

Figure 34. I_{DVDD} vs. Ratio @ DVDD = 3.3 V

APPLYING THE AD9767

OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9767. Unless otherwise noted, I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration can consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage results if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD}, referred to as ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground-referred output voltage. Alternatively, an amplifier can be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity, because I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note that I_{OUTA} provides slightly better performance than I_{OUTB}.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to single-ended signal conversion, as shown in Figure 35. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer pass band. An RF transformer such as the Mini-Circuits® T1-1T provides excellent rejection of common-mode distortion (that is, even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios can also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB}. The complementary voltages appearing at I_{OUTA} and I_{OUTB} (V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and are maintained with the specified output compliance range of the AD9767. A differential resistor (R_{DIFF}) can be inserted in applications where the output of the transformer is connected to the load (R_{LOAD}) via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer impedance ratio and provides the proper source termination, resulting in a low VSWR. Approximately half the signal power is dissipated across R_{DIFF}.

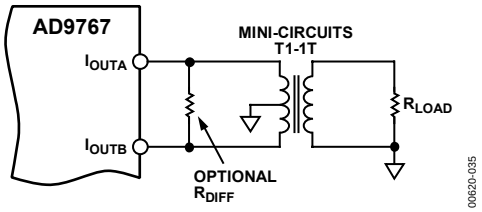

Figure 35. Differential Output Using a Transformer

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion, as shown in Figure 36. The AD9767 is configured with two equal load resistors (R_{LOAD}) of 25 Ω. The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB}, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp distortion performance by preventing the DAC high slewing output from overloading the op amp input.

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate from a dual supply, because its output is approximately ±1.0 V. Select a high speed amplifier capable of preserving the differential performance of the AD9767 while meeting other system level objectives (cost or power). Consider the op amp differential gain, its gain setting resistor values, and full-scale output swing capabilities when optimizing this circuit.

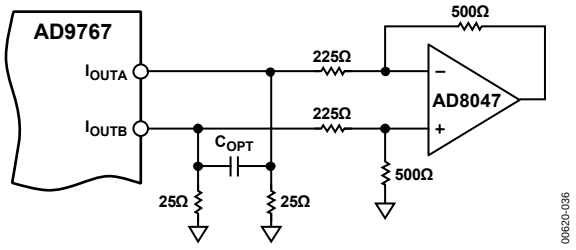

Figure 36. DC Differential Coupling Using an Op Amp

The differential circuit shown in Figure 37 provides the necessary level-shifting required in a single supply system. In this case, AVDD, which is the positive analog supply for both the AD9767 and the op amp, is also used to level-shift the differential output of the AD9767 to midsupply (that is, AVDD/2). The AD8055 is a suitable op amp for this application.

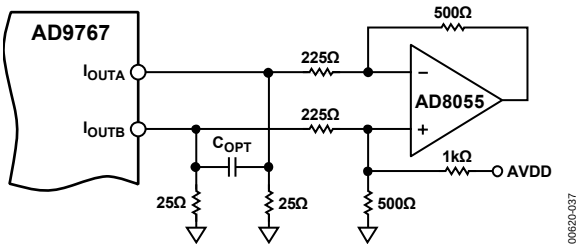

Figure 37. Single-Supply DC Differential-Coupled Circuit

SINGLE-ENDED, UNBUFFERED VOLTAGE OUTPUT

Figure 38 shows the AD9767 configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable because the nominal full-scale current (I_{OUTFS}) of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB}. The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL), as discussed in the Analog Outputs section. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

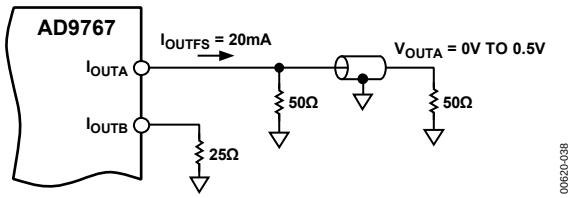

Figure 38. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 39 shows a buffered single-ended output configuration in which the Op Amp U1 performs an I-V conversion on the AD9767 output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC INL performance, as described in the Analog Outputs section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates can be limited by U1 slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. Set the full-scale output within U1 voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance can result with a reduced I_{OUTFS}, because the signal current U1 required to sink is subsequently reduced.

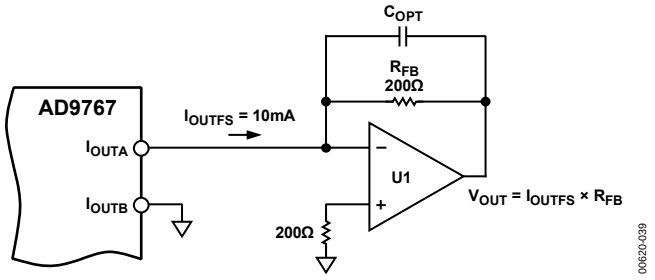

Figure 39. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER-SUPPLY REJECTION

Many applications seek high speed and high performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing, as well as power supply bypassing and grounding, to ensure optimum performance. Figure 45 to Figure 53 illustrate the recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9767 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution. This is referred to as the power supply rejection ratio. For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise occurs over the spectrum of tens of kilohertz to several megahertz. The PSRR vs. frequency of the AD9767 AVDD supply over this frequency range is shown in Figure 40.

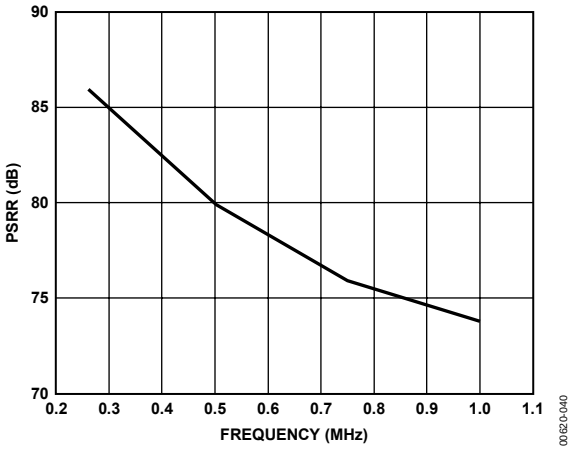

Figure 40. Power Supply Rejection Ratio vs. Frequency

Note that the units in Figure 40 are given in units of amps out/volts in. Noise on the analog power supply has the effect of modulating the internal current sources, and therefore the output current. The voltage noise on AVDD, therefore, is added in a nonlinear manner to the desired I_{OUT}. PSRR is very code-dependent, thus producing mixing effects that can modulate low frequency power supply noise to higher frequencies. Worst-case PSRR for either one of the differential DAC outputs occurs when the full-scale current is directed towards that output. As a result, the PSRR measurement in Figure 40 represents a worst-case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV of noise and, for simplicity's sake (to ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise appears as current noise superimposed on the DAC full-scale current, I_{OUTFS}, one must determine the PSRR in decibels using Figure 40

at 250 kHz. To calculate the PSRR for a given R_{LOAD} such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 40 by the scaling factor 20 × log (RLOAD). For instance, if RLOAD is 50 Ω, the PSRR is reduced by 34 dB (for example, PSRR of the DAC at 250 kHz, which is 85 dB in Figure 40, becomes 51 dB VOUT/VIN).

Proper grounding and decoupling are primary objectives in any high speed, high resolution system. The AD9767 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, decouple the analog supply (AVDD) to the analog common (ACOM), as close to the chip as physically possible. Similarly, decouple the digital supply (DVDD) to the digital common (DCOM) as close to the chip as possible.

For those applications that require a single 5 V or 3.3 V supply for both the analog and digital supplies, a clean analog supply can be generated using the circuit shown in Figure 41. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR-type electrolytic and tantalum capacitors.

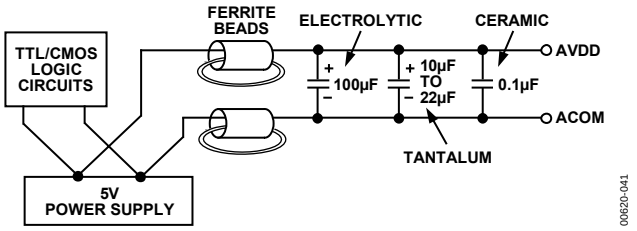

Figure 41. Differential LC Filter for Single 5 V and 3.3 V Applications

APPLICATIONS

VDSL APPLICATIONS USING THE AD9767

Very high frequency digital subscriber line (VDSL) technology is growing rapidly in applications requiring data transfer over relatively short distances. By using quadrature amplitude modulation (QAM) and transmitting the data in discrete multiple tones (DMT), high data rates can be achieved.

As with other multitone applications, each VDSL tone is capable of transmitting a given number of bits, depending on the signal-to-noise ratio (SNR) in a narrow band around that tone. For a typical VDSL application, the tones are evenly spaced over the range of several kHz to 10 MHz. At the high frequency end of this range, performance is generally limited by cable characteristics and environmental factors such as external interferers. Performance at the lower frequencies is much more dependent on the performance of the components in the signal chain. In addition to in-band noise, intermodulation from other tones can also potentially interfere with the data recovery for a given tone. The two graphs in Figure 42 and Figure 43 represent a 500 tone missing bin test vector, with frequencies evenly spaced from 400 Hz to 10 MHz. This test is very commonly done to determine if distortion limits the number of bits that can be transmitted in a tone. The test vector has a series of missing tones around 750 kHz, which is represented in Figure 42, and a series of missing tones around 5 MHz, which is represented in Figure 43. In both cases, the spurious-free dynamic range (SFDR) between the transmitted tones and the empty bins is greater than 60 dB.

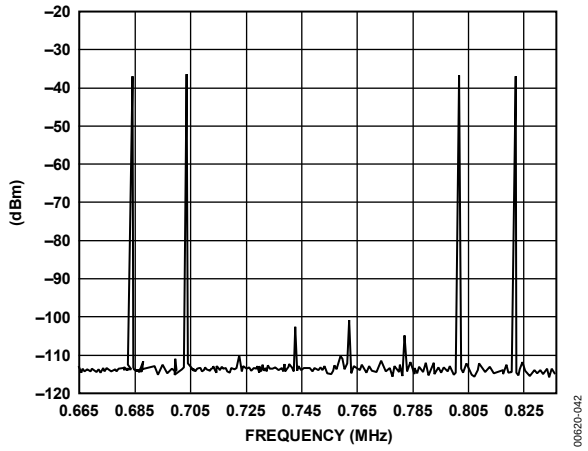

Figure 42. Notch in Missing Bin at 750 kHz Is Down >60 dB (Peak Amplitude = 0 dBm)

CDMA

Code division multiple access (CDMA) is an air transmit/receive scheme in which the signal in the transmit path is modulated with a pseudorandom digital code (sometimes referred to as the spreading code). The effect of this is to spread the transmitted signal across a wide spectrum.

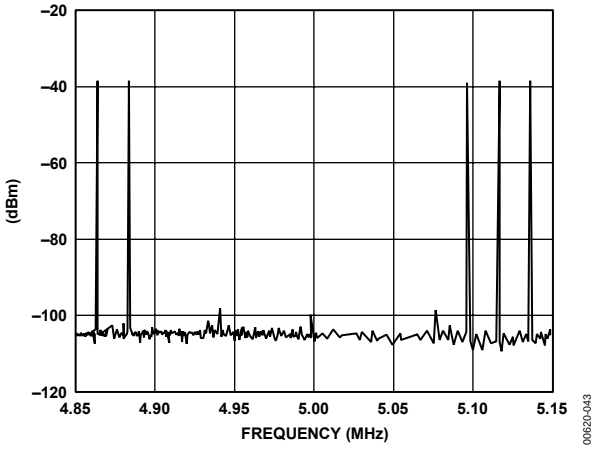

Figure 43. Notch in Missing Bin at 5 MHz Is Down >60 dB (Peak Amplitude = 0 dBm)

Similar to a discrete multitone (DMT) waveform, a CDMA waveform containing multiple subscribers can be characterized as having a high peak to average ratio (that is, crest factor), thus demanding highly linear components in the transmit signal path. The bandwidth of the spectrum is defined by the CDMA standard being used and is implemented in operation by using a spreading code with particular characteristics.

Distortion in the transmit path can lead to power being transmitted out of the defined band. The ratio of power transmitted in-band to out-of-band is often referred to as adjacent channel power (ACP). This is a regulatory issue due to the possibility of interference with other signals being transmitted by air. Regulatory bodies define a spectral mask outside of the transmit band, and the ACP must fall under this mask. If distortion in the transmit path causes the ACP to be above the spectral mask, then filtering, or different component selection, is needed to meet the mask requirements.

Figure 44 shows the AD9767, when used with the AD8346, reconstructing a wideband CDMA signal at 2.4 GHz. The base-band signal is being sampled at 65 MSPS and has a chip rate of 8 M chips.

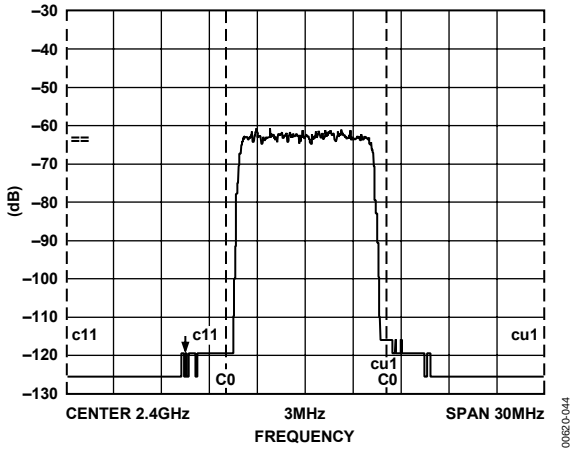

Figure 44. CDMA Signal, 8 M Chips Sampled at 65 MSPS, Recreated at 2.4 GHz Adjacent Channel Power > 60 dBm

EVALUATION BOARD

GENERAL DESCRIPTION

The AD9767-EB is an evaluation board for the AD9767 14-bit dual DAC. Careful attention to layout and circuit design, combined with a prototyping area, allow the user to easily and effectively evaluate the AD9767 in any application where a high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9767 in various configurations. Possible output configurations include transformer-coupled, resistor-terminated, and single and differential outputs. The digital inputs can be used in dual-port or interleaved mode and are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. When operating the AD9767, best performance is obtained by running the DVDD at 3.3 V and the AVDD at 5 V.

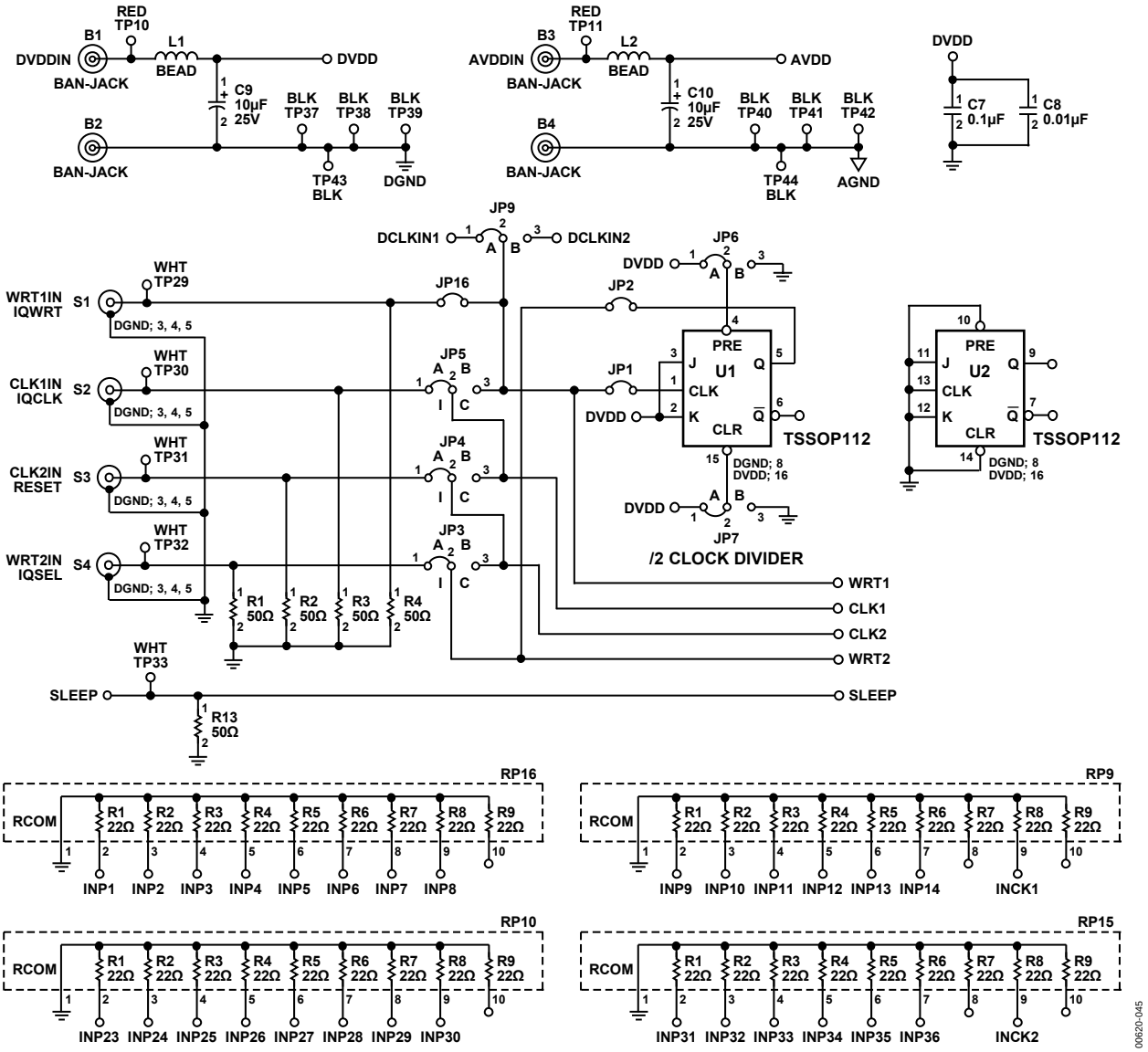

Figure 45. Power Decoupling and Clocks on AD9767 Evaluation Board

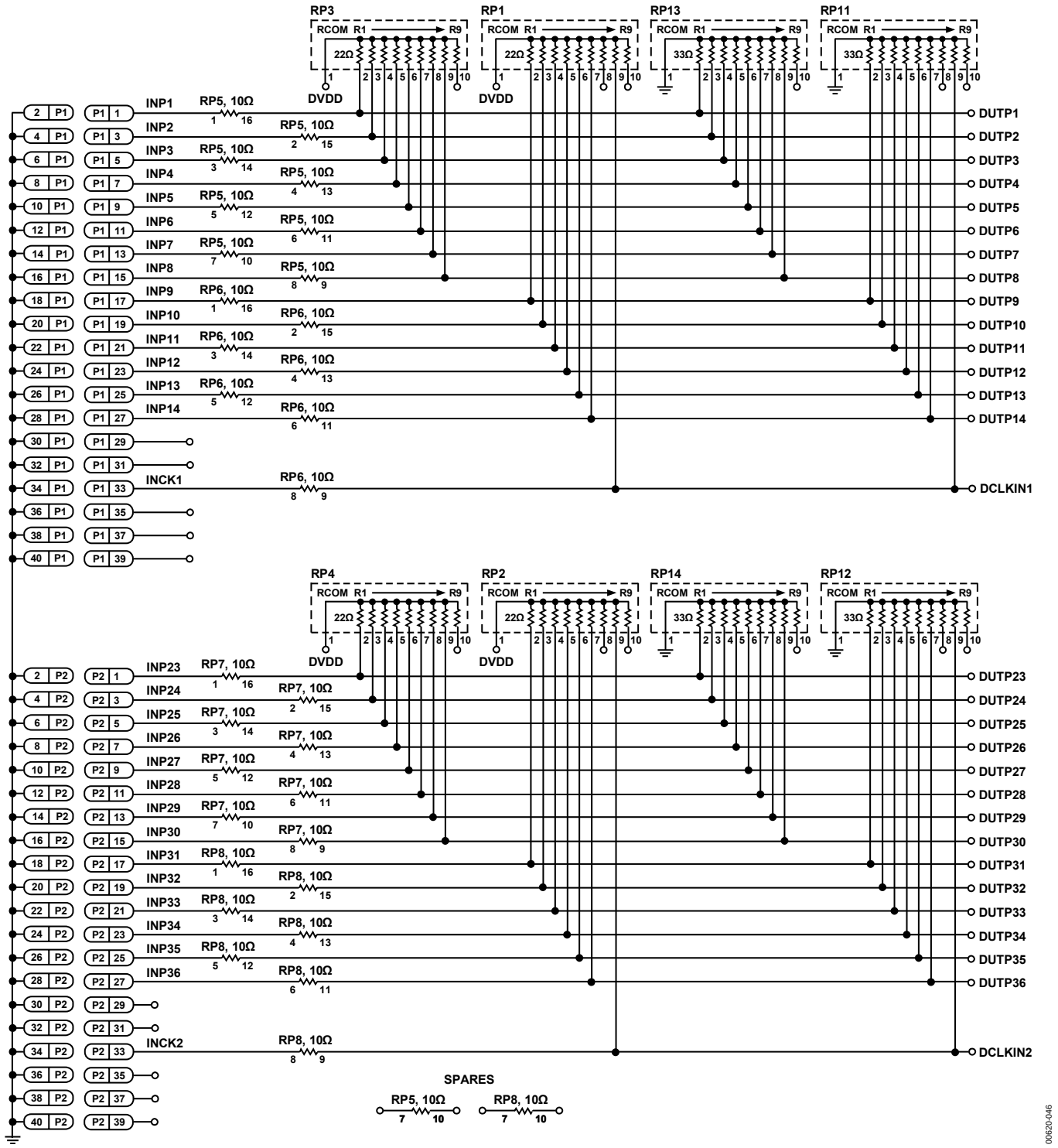

Figure 46. Digital Input Signal Conditioning

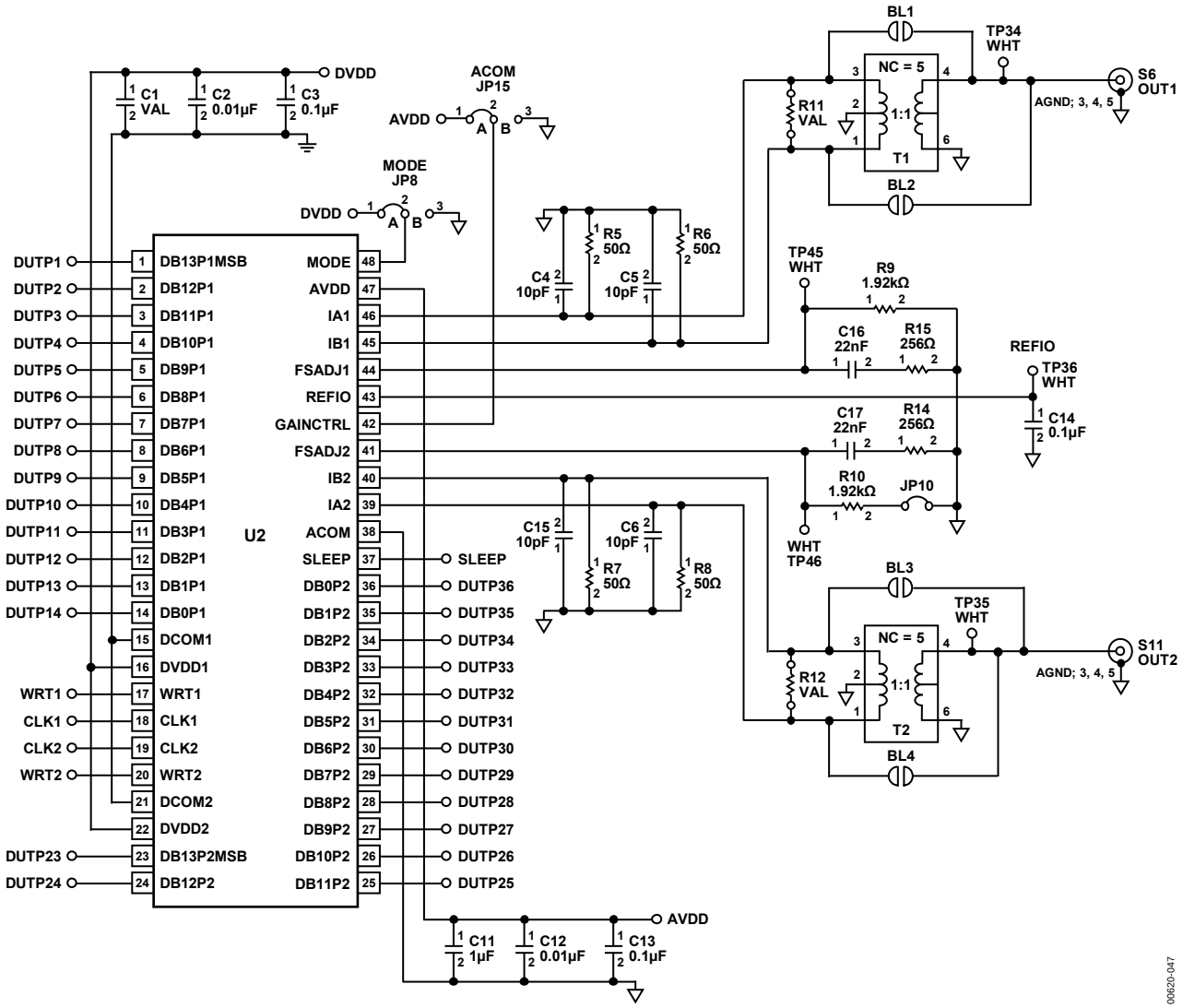

Figure 47. AD9767 and Output Signal Conditioning

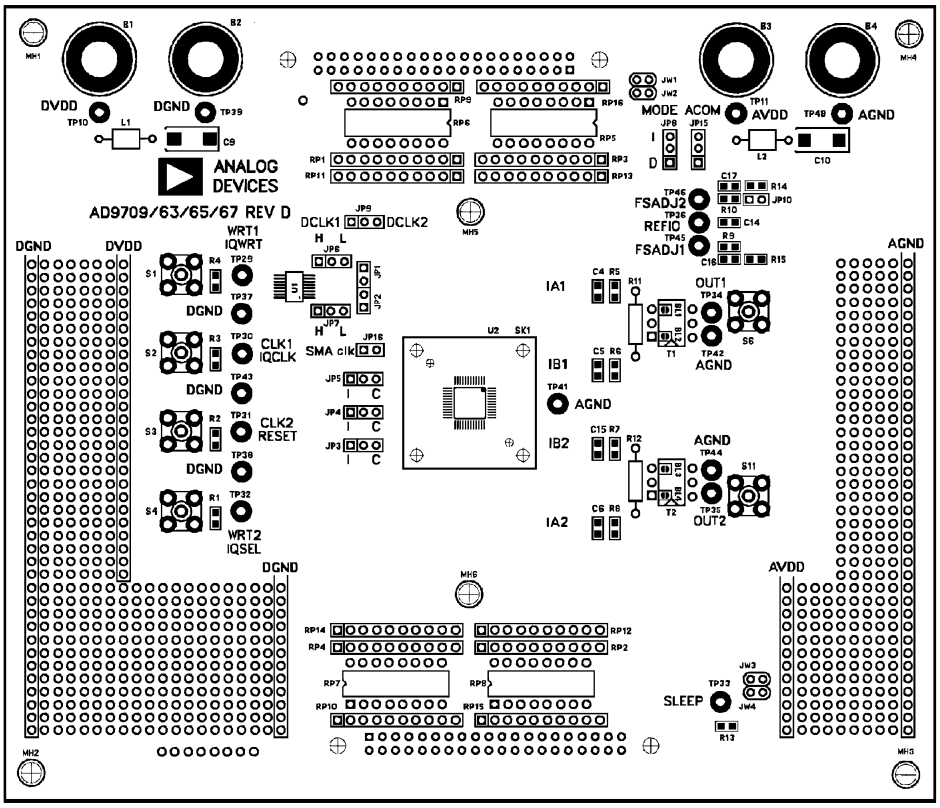

Figure 48. Assembly, Top Side

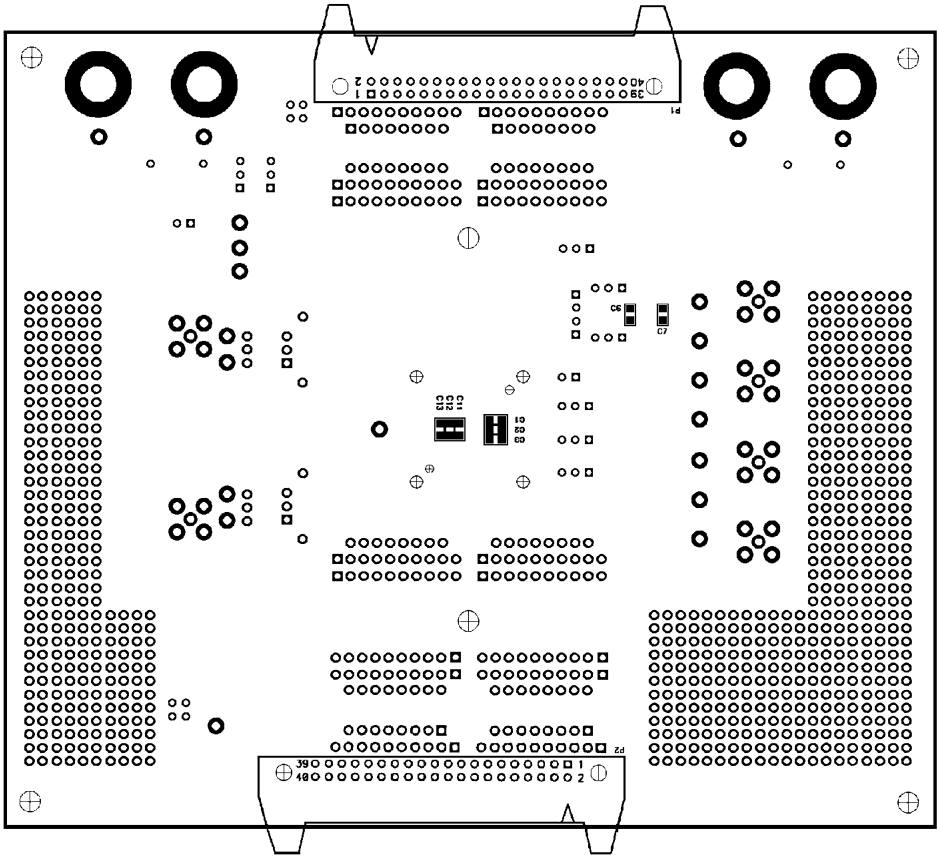

Figure 49. Assembly, Bottom Side

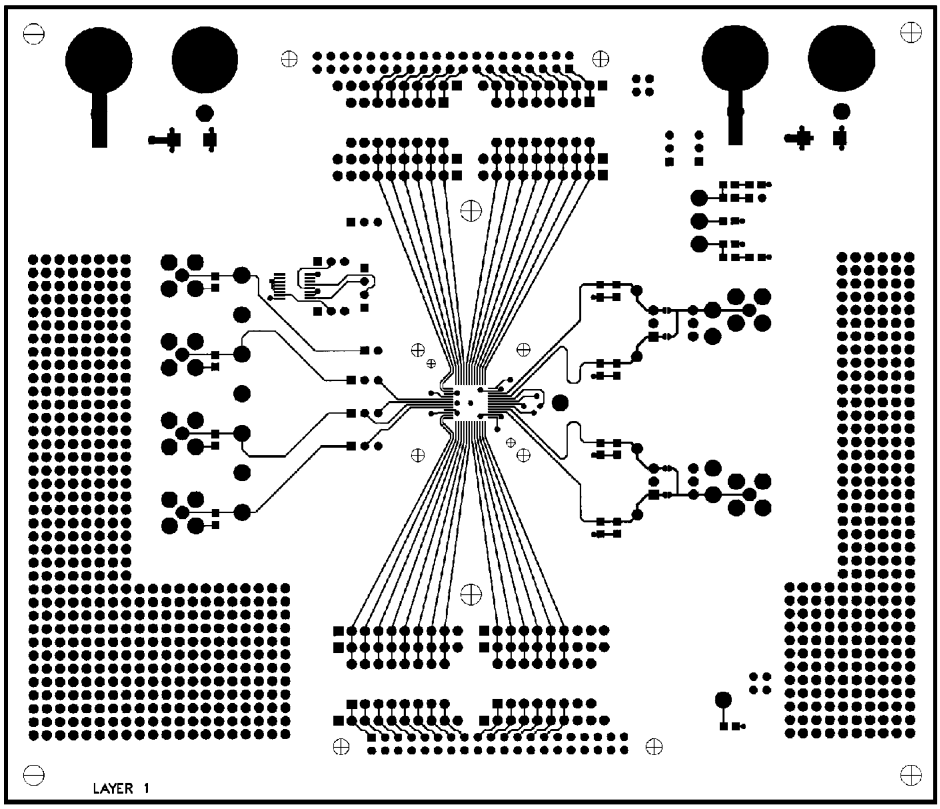

Figure 50. Layer 1, Top Side

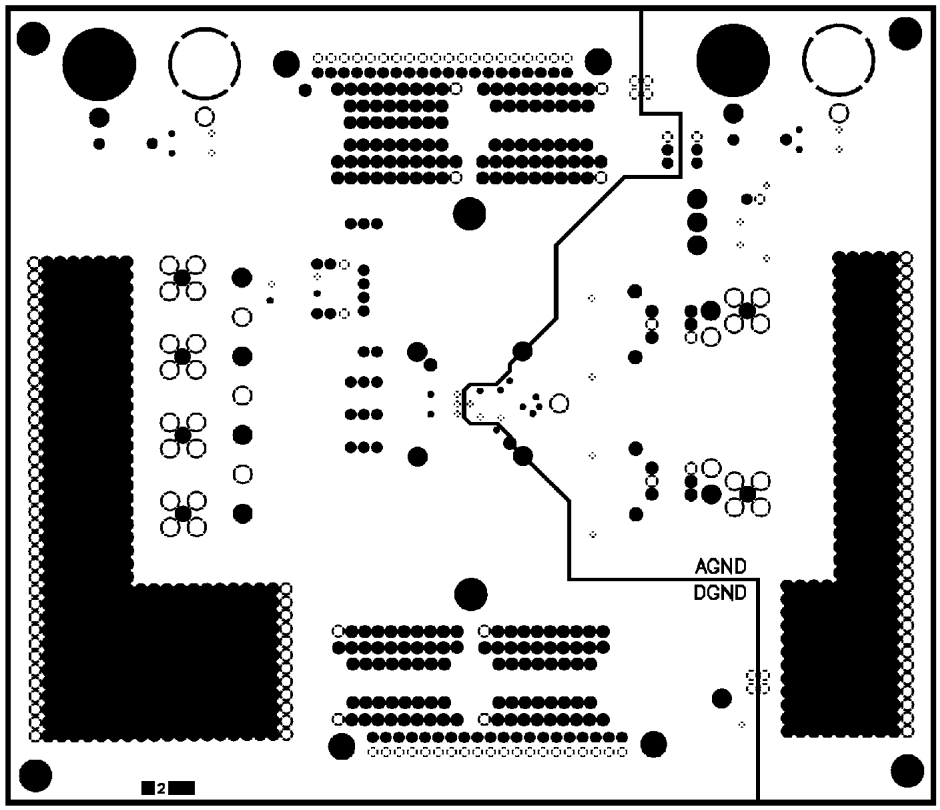

Figure 51. Layer 2, Ground Plane

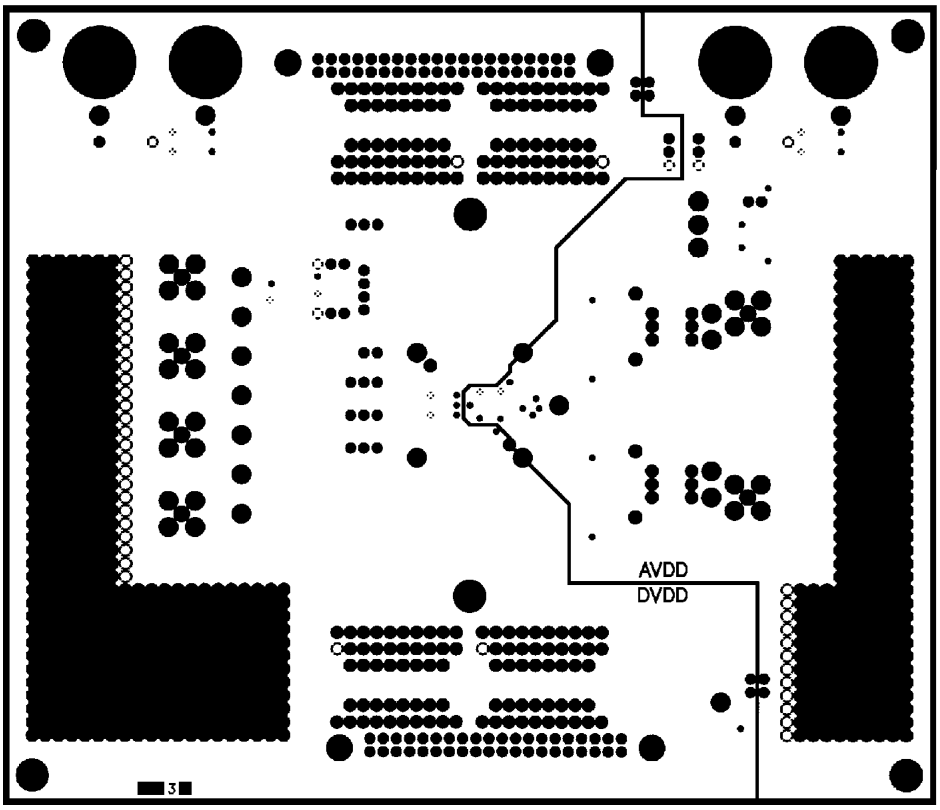

Figure 52. Layer3, Power Plane

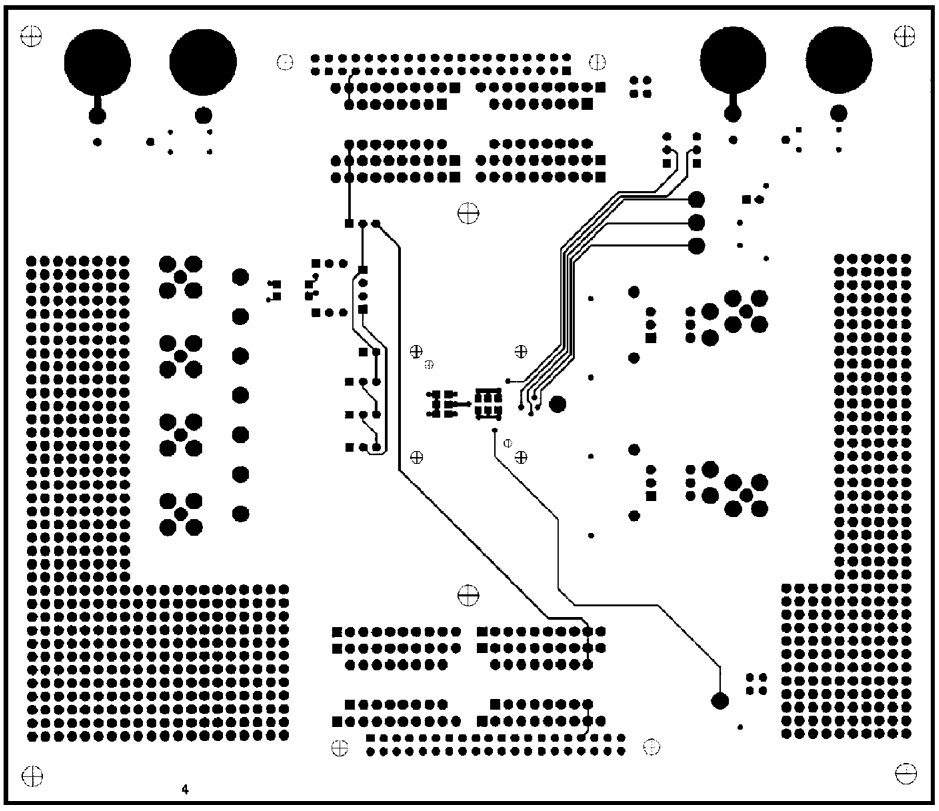

Figure 53. Layer 4, Bottom Side

OUTLINE DIMENSIONS

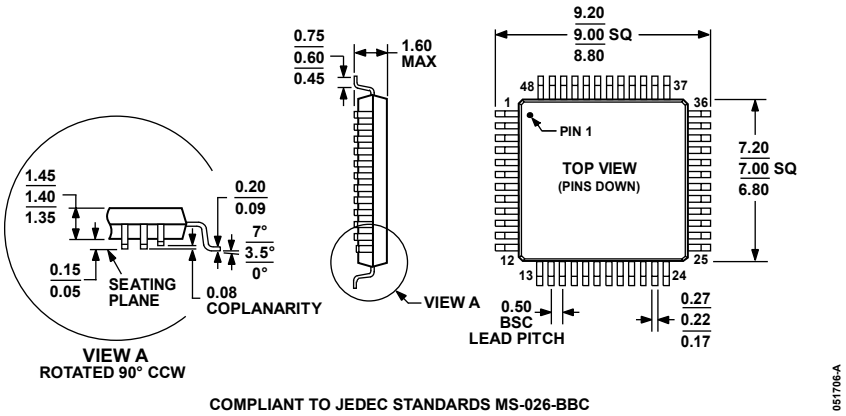

Figure 54. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9767AST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9767ASTRL	–40°C to +85°C	48-Lead LQFP	ST-48
AD9767ASTZ[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD9767ASTZRL[1]	–40°C to +85°C	48-Lead LQFP	ST-48
AD9767-EB		Evaluation Board	

[1] Z = Pb-free part.

C00620-0-10/06(C)