National Semiconductor

ADVANCED INFORMATION

September 2002

DP83865BVH Gig PHYTER® V 10/100/1000 Ethernet Physical Layer

General Description

The DP83865 is a fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83865 is an ultra low power version of the DP83861 and DP83891. It uses advanced 0.18 um, 1.8 V CMOS technology, fabricated at National Semiconductor's South Portland, Maine facility.

The DP83865 is designed for easy implementation of 10/100/1000 Mb/s Ethernet LANs. It interfaces directly to Twisted Pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII) or the IEEE 802.3z Gigabit Media Independent Interface (GMII).

The DP83865 is a fourth generation Gigabit PHY with field proven architecture and performance. Its robust performance ensures drop-in replacement of existing 10/100 Mb/s equipment with 10/100/1000 Mb/s networking infrastructure.

Applications

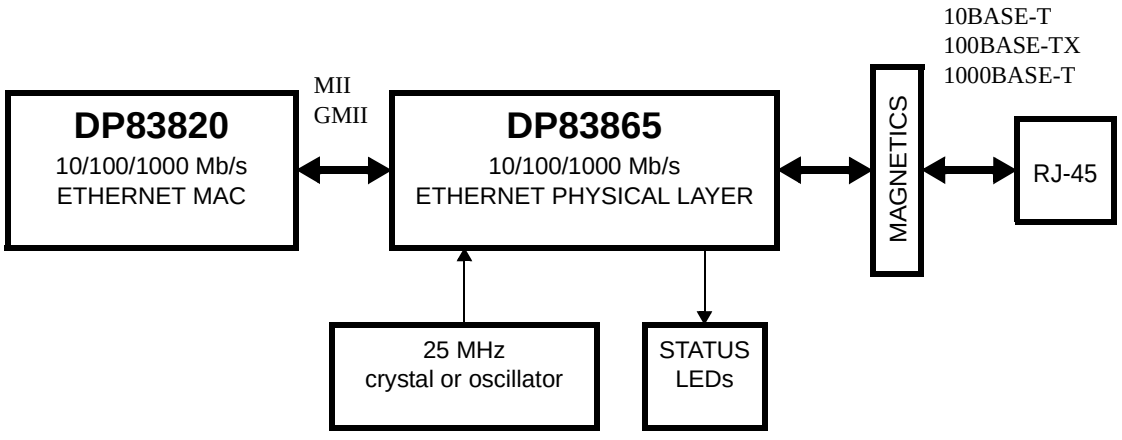
The DP83865 fits applications in:

- 10/100/1000 Mb/s capable node cards
- Switches with 10/100/1000 Mb/s capable ports
- High speed uplink ports (backbone)

Features

- Fully compliant with IEEE 10BASE-T, 100BASE-TX and 1000BASE-T specifications (802.3u, 802.3z, 802.3ab).
- Integrated PMD sublayer featuring adaptive equalization and baseline wander compensation according to ANSI X3.T12.
- 3.3 V or 2.5 V MAC interfaces:
  - IEEE 802.3u MII
  - IEEE 802.3z GMII
- User programmable GMII pin ordering.
- IEEE 802.3u Auto-Negotiation and Parallel Detection
  - Fully Auto-Negotiates between 1000 Mb/s, 100 Mb/s, and 10 Mb/s full duplex and half duplex devices
- LED support for activity, full / half duplex, link1000, link100 and link10 or user programmable (manual on/off).
- Supports 25 MHz operation with crystal or oscillator.
- Requires only two power supplies, 1.8 V (core and analog) and 2.5 V (analog and I/O). 3.3V is supported as an alternative supply for I/O voltage.
- User programmable interrupt.
- Supports Auto-MDIX at 10, 100 and 1000 Mb/s.
- Supports JTAG (IEEE1149.1).
- Ultra low power consumption of one watt typical.
- Management port (MDC / MDIO).
- 128-pin PQFP package (14mm x 20mm).
- WOL support.

System Diagram



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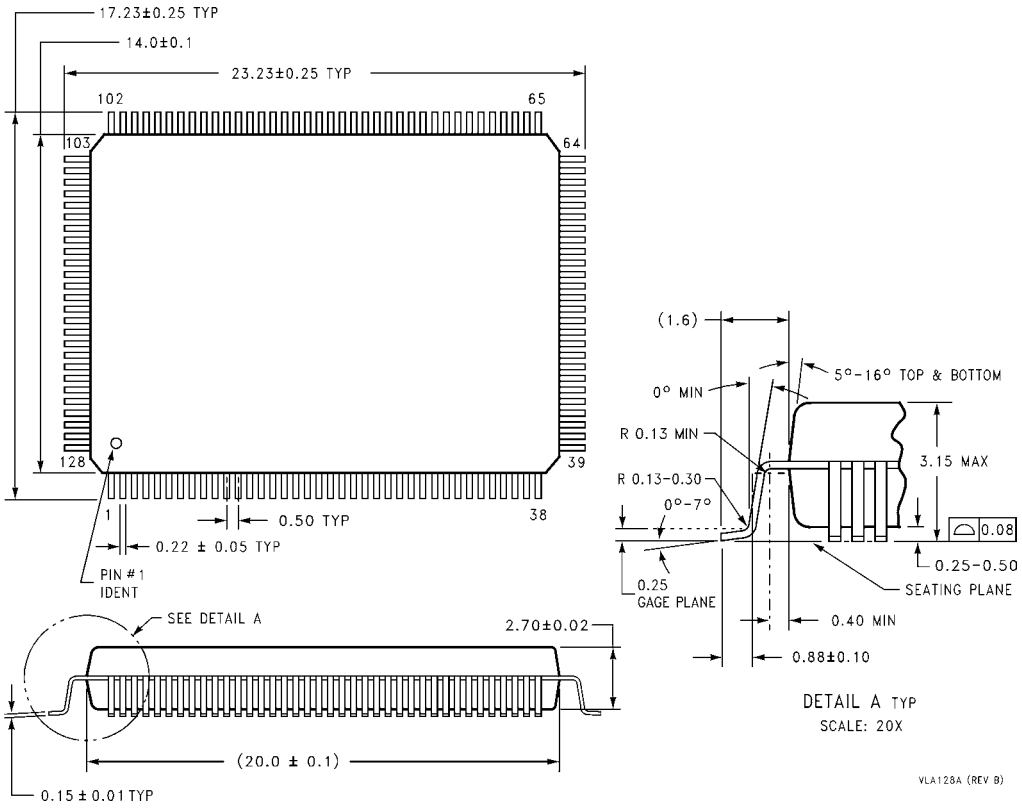
Physical Dimensions inches (millimeters) unless otherwise noted



128 Plastic Leaded Flat Pack
NS Package Number VLA128A
Dimensions in mm

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Francais Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

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