Structure : Silicon monolithic integrated circuit
Product name : USB host MP3 Decoder
Model : BU9431-D1
Outline drawing : Figure-1
Terminal block diagram : Figure-2
Functions : BU9431−D1 is MP3 decoder IC which contains USB host and headphone output function.
(1) MP3 decode function contained. (available for MPEG1, 2 and 2.5, Layer 1, 2 and 3)
(2) USB 2.0 Full Speed host function contained.
(3) Headphone amp output contained.
(4) TQFP64 pin (0.5mm pitch)

● Absolute maximum ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Power-supply Voltage (Analog block, IO)	V_{DD1MAX}	4.5	V
Power-supply Voltage (CORE)	V_{DD2MAX}	2.1	V
Terminal Voltage	V_{INOUT}	-0.3~V_{DD1}+0.3	V
Storage Temperature Range	Tstg	−55～+125	°C
Operating Temperature Range	Topr	−40～85	°C
Allowable dissipation*1	Pd	1000	mW

*1 For an operation with Ta = 25°C or more, it shall be reduced 10mW per °C.

● Operating conditions

Item	Symbol	Rating	Unit	Applicable pins
Power Supply Voltage (Analog block, IO)	V_{DD1}	3.0～3.6	V	DVDDIO, DCVDD, DAVDD, AVDDC, VDD_PLL
Power Supply Voltage (CORE)	V_{DD2}	1.45～1.65	V	DVDD, BATT

※ This product is not designed for protection against radioactive rays.

MPEG Layer-3 audio decoding technology licensed from Fraunhofer IIS and Thomson.

● Electrical characteristics

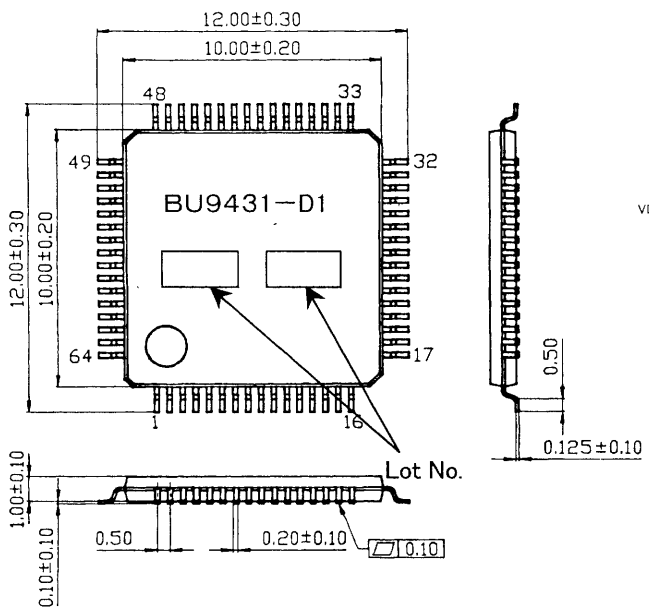
(Unless otherwise specified Ta=25°C, V_{DD1}=3.3V, V_{DD2}=1.6V, XIN_PLL=16.9344MHz, XIN_USB=12.0MHz)

Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN.	TYP.	MAX.		
Total						
Circuit current (V_{DD1})	I_{DD1}	-	25.0	60.0	mA	*1
Circuit current (V_{DD2})	I_{DD2}	-	23.0	40.0	mA	*2
Digital block						
H-level input voltage 1	V_{IH1}	V_{DD1}*0.7	-	V_{DD1}	V	*3
L-level input voltage 1	V_{IL1}	DVSSIO	-	V_{DD1}*0.3	V	*3
H-level input voltage 2	V_{IH2}	V_{DD1}*0.7	-	V_{DD1}	V	*4
L-level input voltage 2	V_{IL2}	DVSSIO	-	V_{DD1}*0.3	V	*4
H-level output voltage 1	V_{OH1}	V_{DD1} - 0.4	-	V_{DD1}	V	I_{OH}=-0.6mA, *5
L-level output voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=0.6mA, *5
H-level output voltage 2	V_{OH2}	V_{DD1} - 0.4	-	V_{DD1}	V	I_{OH}=-1.6mA, *6
L-level output voltage 2	V_{OL2}	0	-	0.4	V	I_{OL}=1.6mA, *6
H-level output voltage 3	V_{OH3}	V_{DD1} - 1.0	-	V_{DD1}	V	I_{OH}=-0.6mA, *7
L-level output voltage 3	V_{OL3}	0	-	1.0	V	I_{OL}=0.6mA, *7
USB HOST						
H-level input voltage	V_{IHUSB}	V_{DD1}*0.6	-	V_{DD1}	V	*8
L-level input voltage	V_{ILUSB}	AVSSC	-	V_{DD1}*0.3	V	*8
Output impedance (H)	Z_{OH}	22.0	45.0	60.0	Ω	*8
Output impedance (L)	Z_{OL}	22.0	45.0	60.0	Ω	*8
H-level output voltage	V_{OHUSB}	V_{DD1} - 0.5	-	V_{DD1}	V	*8
L-level output voltage	V_{OLUSB}	0	-	0.3	V	*8
Rise/Fall time	T_r/T_f	-	11	-	ns	*8, Output capacity 50pF
Voltage of crossing point	V_{CRS}	-	V_{DD1}/2	-	V	*8, Output capacity 50pF
Range of differential input	V_{diff}	0.8	-	2.5	V	*8
Differential input sensitivity	V_{sens}	0.2	-	-	V	*8
Pull-down resistance	R_{PD}	10.0	15.0	20.0	kΩ	*8
Head Phone AMP						
Distortion rate	THD	-	0.03	-	%	1kHz, 0dB, sine, *9
Dynamic range	DR	-	88	-	dB	1kHz, -60dB, sine, *9
S/N ratio	S/N	-	93	-	dB	*9
Max output level	V_{smax}	-	0.67	-	Vrms	RL=32Ω,1kHz,0dB, sine, *9

*1 3.3V system IO, Analog power supply DVDDIO, DCVDD, DAVDD, AVDDC, VDD_PLL
*2 1.6V system CORE power supply DVDD, BATT
*3 PWR_SEL, VOL_SEL, KEY0-1, HOST_CLK, HIDF_SEL, MP3_SEL, HOST_DATA,
*4 XIN_PLL, XIN_USB
*5 KEY2-5, AMUTE, MP3_EN, HOST_STS
*6 ACC_LED, ERR_LED, PLAY_LED
*7 XOUT_PLL, XOUT_USB
*8 USB_DP, USB_DM
*9 LHPO, RHPO

● Description of Terminals

No.	Name	I/O	Description of terminals
1	PWR_SEL	I	Auto play start selection at power-on, device connect (H : Stop, L : Playback)
2	VOL_SEL	I	VOL operation selection (H : VOL+, −Validity, L : VOL+, −Invalidity)
3	KEY0	I	Matrix 0 for KEY operation terminal
4	KEY1	I	Matrix 1 for KEY operation terminal
5	DVDDIO	-	IO Power supply (V_{DD1}) terminal
6	KEY2	O	Matrix 2 for KEY operation terminal
7	KEY3	O	Matrix 3 for KEY operation terminal
8	KEY4	O	Matrix 4 for KEY operation terminal
9	KEY5	O	Matrix 5 for KEY operation terminal
10	HOST_CLK	I	Host serial command clock input terminal
11	HIDF_SEL	I	Hidden file playback selection (H: It playback, L: It doesn't playback)
12	MP3_SEL	I	MPEG Audio Layer selection (H: Only MP3 is playback, L: MP1, MP2, and MP3 can be playback)
13	TEST1	I	Connect to V_{DD1} system power supply terminal (TEST PIN)
14	HOST_DATA	I	Host serial command data input terminal
15	DVDD	-	CORE Power supply (V_{DD2}) terminal
16	DVDDIO	-	IO Power supply (V_{DD1}) terminal
17	AMUTE	O	Audio mute output terminal (H: Mute release, L: Mute)
18	MP3_EN	O	MP3 playback standby terminal (H: system initialization)
19	DVSSIO	-	IO GND terminal
20	TEST2	-	Connect to V_{DD2} system power supply terminal (TEST PIN)
21	TEST3	-	Connect to DCVSS terminal (TEST PIN)
22	TEST4	-	Connect to V_{DD2} system power supply terminal (TEST PIN)
23	TEST5	-	Connect to DCVSS terminal (TEST PIN)
24	TEST6	-	Connect to V_{DD2} system power supply terminal (TEST PIN)
25	TEST7	-	Connect to DCVSS terminal (TEST PIN)
26	DCVSS	-	GND terminal
27	TEST8	-	OPEN (TEST_PIN)
28	TEST9	-	OPEN (TEST_PIN)
29	TEST10	-	OPEN (TEST_PIN)
30	DCVDD	-	Power supply (V_{DD1}) terminal
31	TEST11	-	OPEN (TEST_PIN)
32	PWSW	I	Connect to DCVSS.
33	BATT	-	Power supply (V_{DD2}) terminal
34	DAVDD	-	Head Phone AMP power supply (V_{DD1}) terminal
35	RHPO	O	Head Phone AMP Rch output terminal
36	DAVSS	-	Head Phone AMP GND terminal
37	VCDACO	O	Head Phone AMP reference voltage output terminal
38	CPOP	O	Head Phone AMP POP noise prevention output terminal
39	CMUTE	O	Head Phone AMP Soft mute output terminal
40	DAVSS	-	Head Phone AMP GND terminal
41	LHPO	O	Head Phone AMP Lch output terminal
42	DAVDD	-	Head Phone AMP power supply (V_{DD1}) terminal
43	REXTI	O	USB bias resistor (12kΩ) connecting terminal
44	XIN_USB	I	X 'tal(12MHz) connecting input terminal
45	XOUT_USB	O	X 'tal(12MHz) connecting terminal
46	AVDDC	-	USB Power supply (V_{DD1}) terminal
47	USB_DP	I/O	USB D+ I/O terminal
48	USB_DM	I/O	USB D- I/O terminal
49	AVSSC	-	USB GND terminal
50	VSS_PLL	-	PLL GND terminal
51	XIN_PLL	I	X 'tal(16.9344MHz) connecting input terminal
52	XOUT_PLL	O	X 'tal(16.9344MHz) connecting terminal
53	VDD_PLL	-	PLL Power supply (V_{DD1}) terminal
54	DVDD	-	CORE Power supply (V_{DD2}) terminal
55	HOST_STS	O	Host serial command status output terminal
56	TEST12	I	Connect to V_{DD1} system power supply terminal (TEST PIN)
57	TEST13	I	Connect to V_{DD1} system power supply terminal (TEST PIN)
58	TEST14	I	Connect to V_{DD1} system power supply terminal (TEST PIN)
59	ACC_LED	O	LED lighting output when USB memory is being accessed
60	ERR_LED	O	Error generation LED lighting output
61	PLAY_LED	O	LED lighting output at PLAY
62	DVSS	-	CORE GND terminal
63	TMODEX	I	Test mode input terminal. Connect to V_{DD1} system power supply terminal
64	DVSSIO	-	IO GND terminal



(UNIT: mm)

Figure-1 Outline Drawing

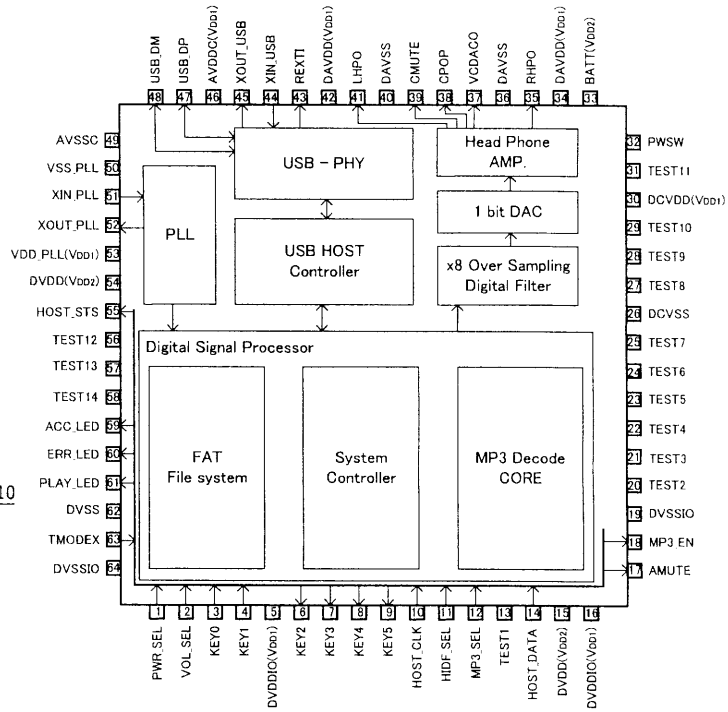


Figure-2 Terminal block diagram(Top view)

● Directions

(1)Power on Reset

Please note the following points to operate power-on reset with which internal is generated normally when the power supply starts.
①After 1.6V power supply are turned on, 3.3V power supply are turned on, when the power supply starts.
②Power-on reset might not operate normally when 1.6V power supply are momentarily turned off. In this case, please turn on the power supply again by the method of ① after turning off all power supply system.

(2)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as power-supply voltage, operating temperature range, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(3) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant

(4) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(5) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.