

Dual and Quad, JFET Input Precision High Speed Op Amps

FEATURES

- 14V/μs Slew Rate: 10V/μs Min
- 5MHz Gain-Bandwidth Product
- Fast Settling Time: 1.3μs to 0.02%
- 150μV Offset Voltage (LT1057): 450μV Max
- 180μV Offset Voltage (LT1058): 600μV Max
- 2μV/°C V_{OS} Drift: 7μV/°C Max
- 50pA Bias Current at 70°C
- Low Voltage Noise:
 - 13nV/√Hz at 1kHz
 - 26nV/√Hz at 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample-and-Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters

DESCRIPTION

The LT[®]1057 is a matched JFET input dual op amp in the industry standard 8-pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

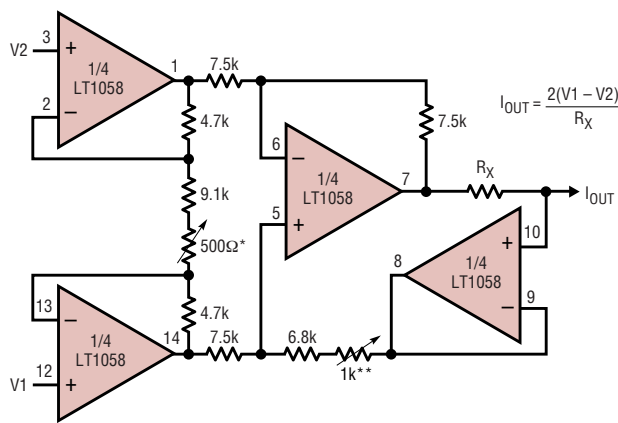
The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14-pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. The LT1058 can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

Both the LT1057 and LT1058 are available in the plastic PDIP package and the surface mount SO package.

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TYPICAL APPLICATION

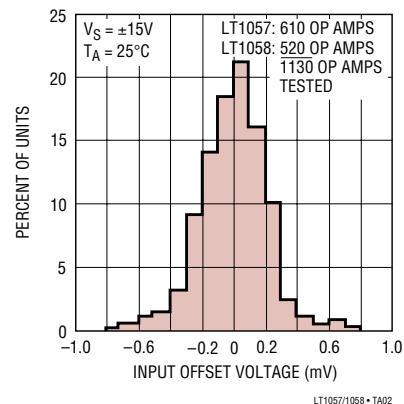
Current Output, High Speed, High Input Impedance Instrumentation Amplifier



*GAIN ADJUST
 **COMMON MODE REJECTION ADJUST
 BANDWIDTH = 2MHz

LT1057/1058 • TA01

Distribution of Offset Voltage (All Packages, LT1057 and LT1058)



LT1057/LT1058

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $\pm 20V$
 Differential Input Voltage $\pm 40V$
 Input Voltage $\pm 20V$
 Output Short-Circuit Duration Indefinite
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

Operating Temperature Range

LT1057AM/LT1057M/
 LT1058AM/LT1058M (**OBsolete**)... $-55^{\circ}C$ to $125^{\circ}C$
 LT1057AC/LT1057C/LT1057S
 LT1058AC/LT1058C/LT1058S $0^{\circ}C$ to $70^{\circ}C$
 LT1057I $-40^{\circ}C \leq T_A \leq 85^{\circ}C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>SW PACKAGE 16-LEAD PLASTIC (WIDE) SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 90^{\circ}C/W$</p>	<p>TOP VIEW</p> <p>SW PACKAGE 16-LEAD PLASTIC (WIDE) SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 90^{\circ}C/W$</p>	<p>TOP VIEW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 200^{\circ}C/W$</p> <p>Please note that the LT1057S8/LT1057IS8 standard surface mount pin-out differs from that of the LT1057 standard Cerdip/PDIP packages.</p>	<p>ORDER PART NUMBER</p> <p>LT1057S8 LT1057IS8</p> <p>S8 PART MARKING</p> <p>1057 1057I</p>
<p>ORDER PART NUMBER</p> <p>LT1057SW LT1057ISW</p>	<p>ORDER PART NUMBER</p> <p>LT1058SW LT1058ISW</p>	<p>TOP VIEW</p> <p>H PACKAGE 8-LEAD METAL CAN OBsolete PACKAGE Consider the N8 or S8 Package for Alternate Source</p>	<p>ORDER PART NUMBER</p> <p>LT1057AMH LT1057MH LT1057ACH LT1057CH</p>
<p>TOP VIEW</p> <p>N14 PACKAGE 14-LEAD PDIP $T_{JMAX} = 110^{\circ}C, \theta_{JA} = 130^{\circ}C/W$</p> <p>J14 PACKAGE 14-LEAD CERDIP $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 100^{\circ}C/W$</p>	<p>ORDER PART NUMBER</p> <p>LT1058ACN LT1058CN</p> <p>LT1058AMJ LT1058MJ LT1058ACJ LT1058CJ</p>	<p>ORDER PART NUMBER</p> <p>LT1057ACN8 LT1057CN8</p> <p>LT1057ACJ8 LT1057CJ8 LT1057AMJ8 LT1057MJ8</p>	<p>TOP VIEW</p> <p>N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 100^{\circ}C, \theta_{JA} = 130^{\circ}C/W$</p> <p>J8 PACKAGE 8-LEAD CERDIP $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 100^{\circ}C/W$</p>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057		150	450	200	800	μV	
		LT1057 (S8 Package)				220	1200	μV	
		LT1058		180	600	250	1000	μV	
I_{OS}	Input Offset Current	Fully Warmed Up		3	40	4	50	pA	
I_B	Input Bias Current	Fully Warmed Up		± 5	± 50	± 7	± 75	pA	
	Input Resistance	Differential		10^{12}		10^{12}		Ω	
		Common Mode $V_{CM} = -11V$ to 8V		10^{12}		10^{12}		Ω	
		Common Mode $V_{CM} = 8V$ to 11V		10^{11}		10^{11}		Ω	
	Input Capacitance			4		4		pF	
e_n	Input Noise Voltage	0.1Hz to 10Hz, LT1057 LT1058			2.0		2.1	μV_{P-P}	
					2.4		2.5	μV_{P-P}	
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$ (Note 3)		26		28		nV/\sqrt{Hz}	
				13	22	14	24	nV/\sqrt{Hz}	
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 4)		1.5	4	1.8	6	fA/\sqrt{Hz}	
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$ $V_O = \pm 10V, R_L = 1k$	150	350		100	300	V/mV	
			120	250		80	220	V/mV	
	Input Voltage Range		± 10.5	14.3		± 10.5	14.3	V	
				-11.5			-11.5	V	
CMRR	Common Mode Rejection Ratio	LT1057 LT1058		86	100		82	98	dB
				84	98		80	96	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103		86	102	dB	
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		± 12	± 13	V	
SR	Slew Rate		10	14		8	13	V/ μs	
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3.5	5		3	5	MHz	
I_S	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130	dB	

(LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057 LT1058		0.3	2	mV
				0.35	2.5	
I_{OS}	Input Offset Current	Fully Warmed Up		5	50	pA
I_B	Input Bias Current	Fully Warmed Up		± 10	± 100	pA
	Input Resistance –Differential –Common-Mode	$V_{CM} = -11V$ to 8V $V_{CM} = 8V$ to 11V		0.4		T Ω
				0.4		
				0.05		
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058		2.1		μV_{P-P}
				2.5		
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$		26		nV/\sqrt{Hz}
				13		

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LT1057/LT1058

ELECTRICAL CHARACTERISTICS

(LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$		1.8		fA/ \sqrt{Hz}
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$ $R_L = 2k$ $R_L = 1k$	100 50	300 220		V/mV
	Input Voltage Range		± 10.5	14.3 - 11.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 15V$ LT1057 LT1058	82 80	98 98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		V
SR	Slew Rate		8	13		V/ μs
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3	5		MHz
I_S	Supply Current Per Amplifier			1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		130		dB

The ● denotes the specifications which apply over the temperature range of $0^\circ C \leq T_A \leq 70^\circ C$ or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057IS8), otherwise specifications are $T_A = 25^\circ C$. $V_S = \pm 15V$, $V_{CM} = 0V$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1057AC LT1058AC			LT1057C LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057		250	800	330	1400	μV	
		LT1057IS8	●			500	2300	μV	
		LT1057S8	●			400	1900	μV	
		LT1058	●	300	1200	400	1800	μV	
	Average Temperature Coefficient of Input (Offset Voltage)	LT1057 H/J8 Package	●	1.8	7	2.3	12	$\mu V/^\circ C$	
		N8 Package	●	3	10	4	16	$\mu V/^\circ C$	
		LT1057S8 (Note 5)	●			4	16	$\mu V/^\circ C$	
		LT1057IS8 (Note 5)	●			4.5	16	$\mu V/^\circ C$	
		LT1058 J Package (Note 5)	●	2.5	10	3	15	$\mu V/^\circ C$	
	N Package (Note 5)	●	4	15	5	22	$\mu V/^\circ C$		
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8		18	150	20 35	250 600	pA	
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8		± 50	± 250	± 60 ± 100	± 350 ± 900	pA	
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$	●	70	220	50	200	V/mV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98	80	96	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	102	84	100	dB	
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.8	± 12	± 12.8	V	
I_S	Supply Current Per Amplifier		●		2.8		3.2	mA	
		$T_A = 70^\circ C$		1.4		1.5		mA	

ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only.) The ● denotes specifications which apply over the temperature range of $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ (LT1057SW, LT1058SW) or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057ISW, LT1058ISW), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057	●		0.5	2.5	mV
		LT1058S	●		0.6	3.0	
		LT1058IS	●		0.7	4.0	
	Average Temperature Coefficient of Input Offset Voltage		●		5		$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$			20	250	μA
		Warmed Up, $T_A = 85^\circ C$			35	400	
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$			± 60	± 400	μA
		Warmed Up, $T_A = 85^\circ C$			± 100	± 700	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	LT1057	●	50	200	mV
			LT1058	●	40	200	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	LT1057	●	80	96	dB
			LT1058	●	78	96	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	LT1057	●	84	100	dB
			LT1058	●	82	100	
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.8		V

The ● denotes specifications which apply over the temperature range of $-55^\circ C \leq T_A \leq 125^\circ C$, $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AM LT1058AM			LT1057M LT1058M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057	●		300	1100		400	2000	μV
		LT1058	●		380	1600		550	2500	μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057	●		2.0	7		2.5	12	$\mu V/^\circ C$
		LT1058 (Note 5)	●		2.5	10		3	15	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125^\circ C$			0.15	2		0.2	3	nA
I_B	Input Bias Current	Warmed Up, $T_A = 125^\circ C$			± 0.6	± 4.5		± 0.7	± 6	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120		30	110		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	100		83	98		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.7		± 12	± 12.6		V
I_S	Supply Current Per Amplifier	$T_A = 125^\circ C$			1.25	1.9		1.3	2.2	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; (i.e., out of 100 LT1058s or, 100 LT1057s, typically 240 op amps, or 120 for the LT1057, will be better than the indicated specification).

Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula:

$$i_n = (2qI_b)^{1/2}$$

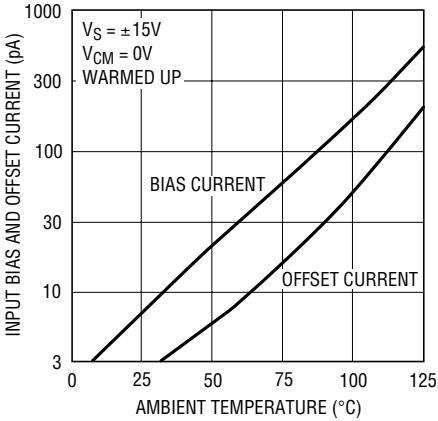
where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 1G swamps the contribution of current noise.

Note 5: This parameter is not 100% tested.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

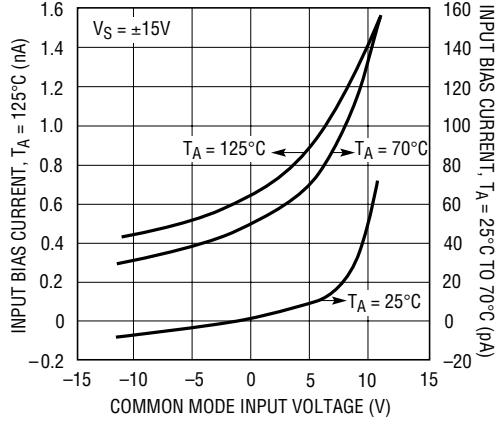
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Currents vs Temperature



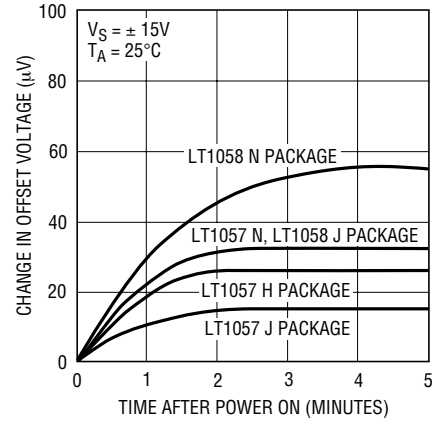
LT1057/1058 • TPC01

Input Bias Current Over the Common-Mode Range



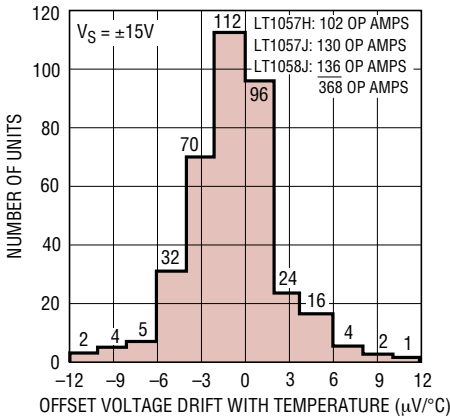
LT1057/1058 • TPC02

Warm-Up Drift



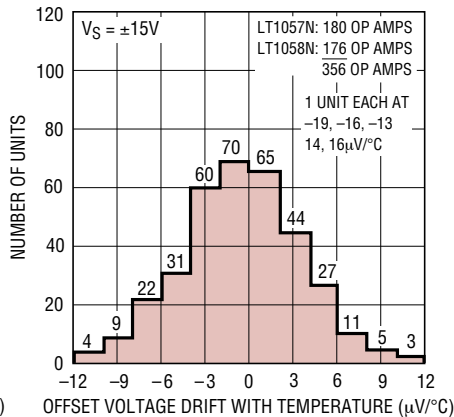
LT1057/1058 • TPC03

Distribution of Offset Voltage Drift with Temperature (H and J Package)



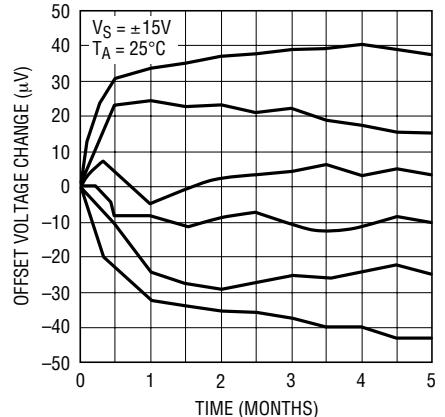
LT1057/1058 • TPC04

Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



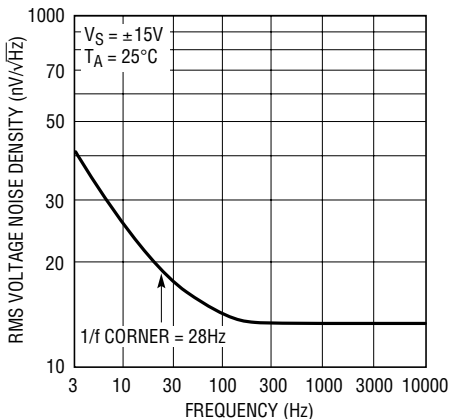
LT1057/1058 • TPC05

Long-Term Drift of Representative Units



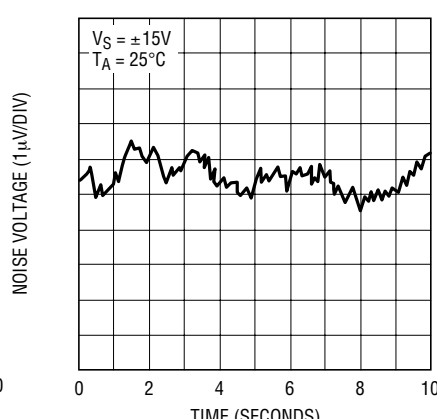
LT1057/1058 • TPC06

Voltage Noise vs Frequency



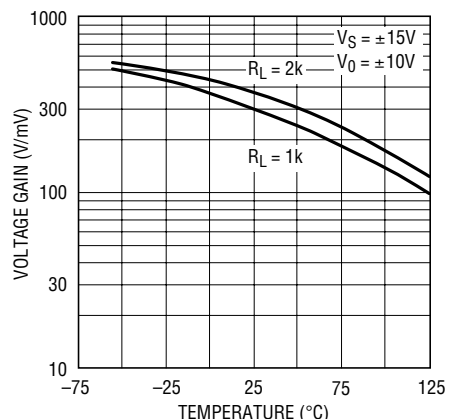
LT1057/1058 • TPC07

0.1Hz to 10Hz Noise



LT1057/1058 • TPC08

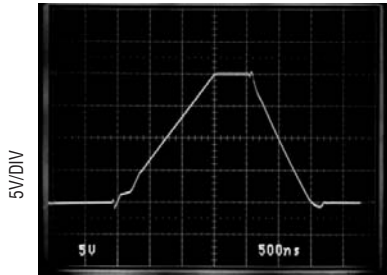
Voltage Gain vs Temperature



LT1057/1058 • TPC09

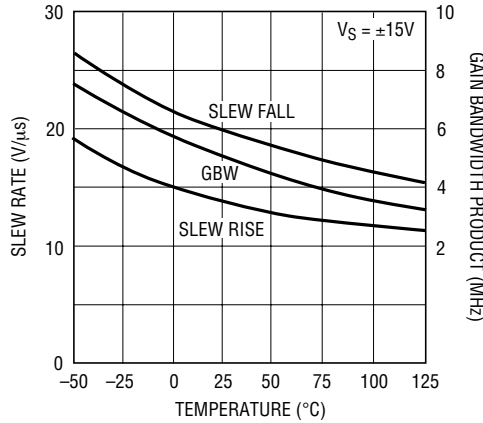
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Response



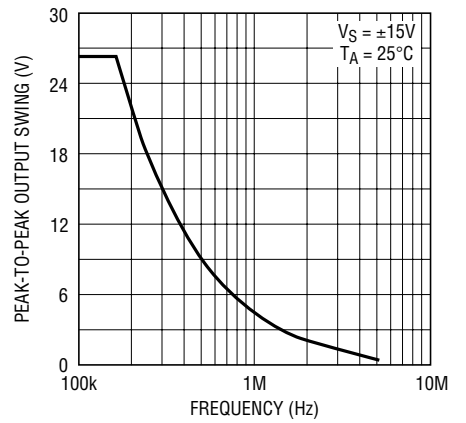
$A_V = +1$
 $C_L = 100\text{pF}$
0.5µs/DIV

Slew Rate, Gain-Bandwidth Product vs Temperature



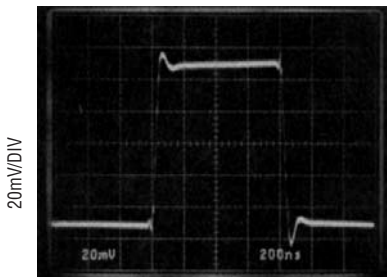
LT1057/1058 • TPC10

Undistorted Output Swing vs Frequency



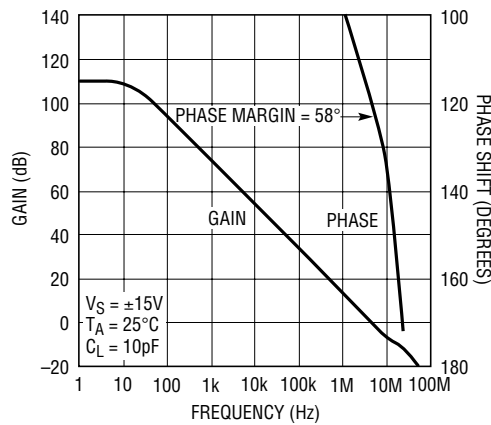
LT1057/1058 • TPC11

Small-Signal Response



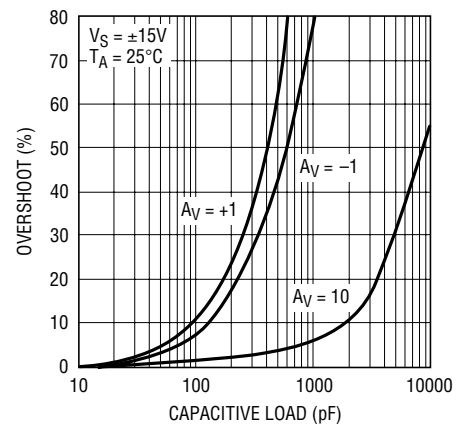
$A_V = +1$
 $C_L = 100\text{pF}$
0.2µs/DIV

Gain, Phase Shift vs Frequency



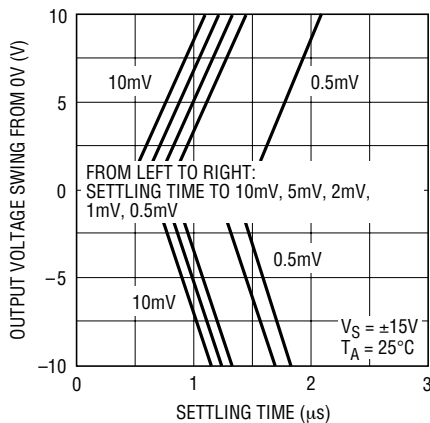
LT1057/1058 • TPC12

Capacitive Load Handling



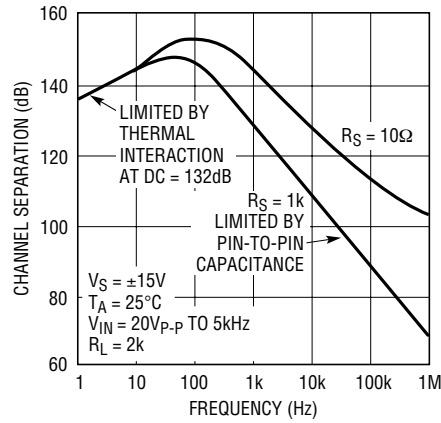
LT1057/1058 • TPC13

Settling Time



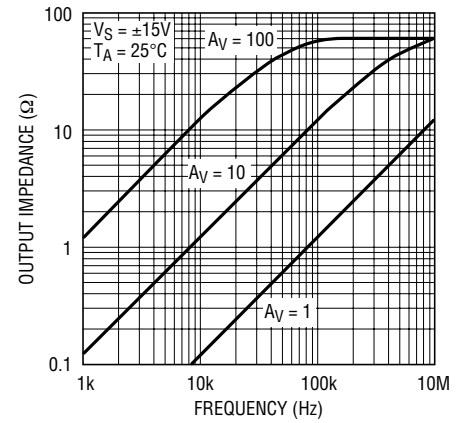
LT1057/1058 • TPC14

Channel Separation vs Frequency



LT1057/1058 • TPC15

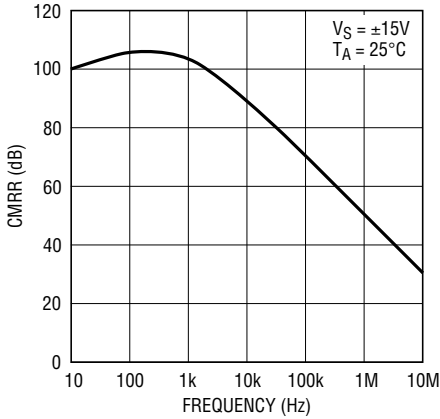
Output Impedance vs Frequency



LT1057/1058 • TPC16

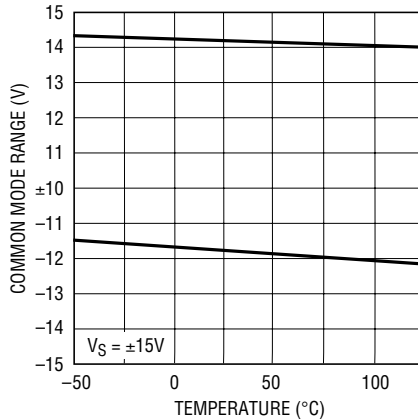
TYPICAL PERFORMANCE CHARACTERISTICS

Common Mode Rejection Ratio vs Frequency



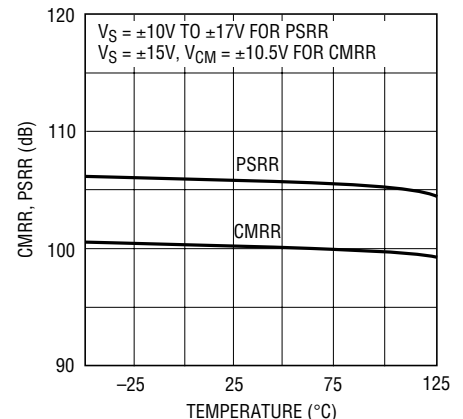
LT1057/1058 • TPC17

Common Mode Range vs Temperature



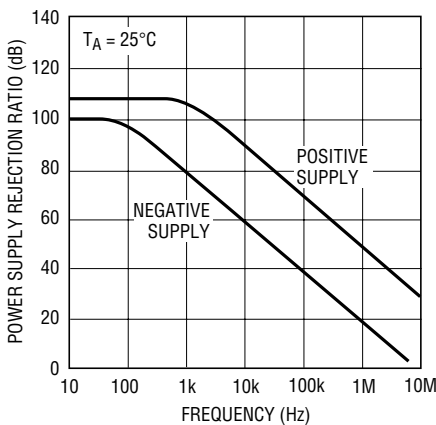
LT1057/1058 • TPC18

Common Mode and Power Supply Rejections vs Temperature



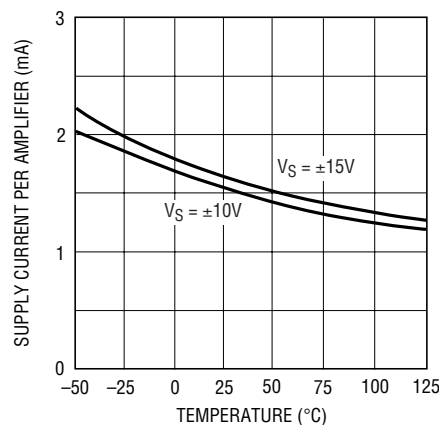
LT1057/1058 • TPC19

Power Supply Rejection Ratio vs Frequency



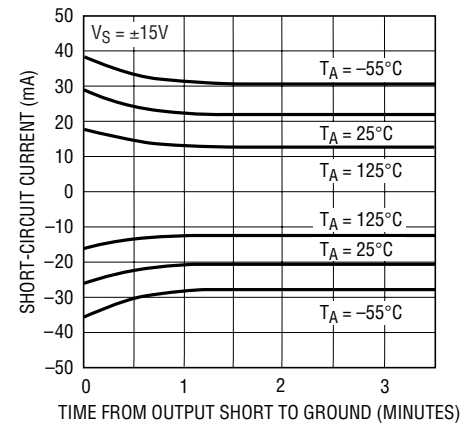
LT1057/1058 • TPC20

Supply Current vs Temperature



LT1057/1058 • TPC21

Short-Circuit Current vs Time (One Output Shorted to Ground)



LT1057/1058 • TPC22

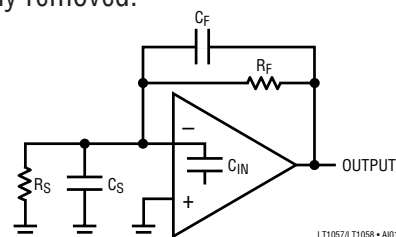
APPLICATIONS INFORMATION

The LT1057 may be inserted directly in LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074 and TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F) a pole will be created with R_F , the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4\text{pF}$). In low closed loop gain configurations and

with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



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APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., PTFE, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations, the guard ring should be tied to ground, in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers (because the transconductance of FETs is considerably lower than that of bipolar transistors). Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

PTFE is a trademark of DuPont.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical $40\mu\text{V}$ hysteresis ($50\mu\text{V}$ on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than $20\mu\text{V}$) hysteresis effect.

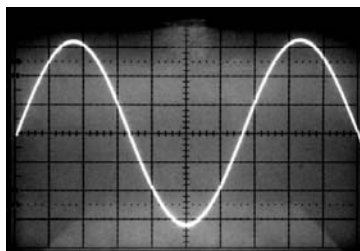
The offset voltage and drift performance are also affected by packaging. In the plastic N package, the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently for best drift performance, as shown in the Typical Performance Characteristics distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

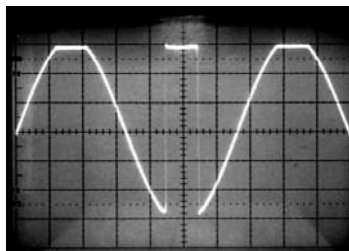
Phase Reversal Protection

Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., below -12V with $\pm 15\text{V}$ supplies). The photos below show a $\pm 16\text{V}$ sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

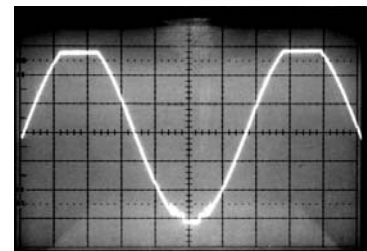
The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.



(A) $\pm 16\text{V}$ Sine Wave Input



(B) LF412A Output

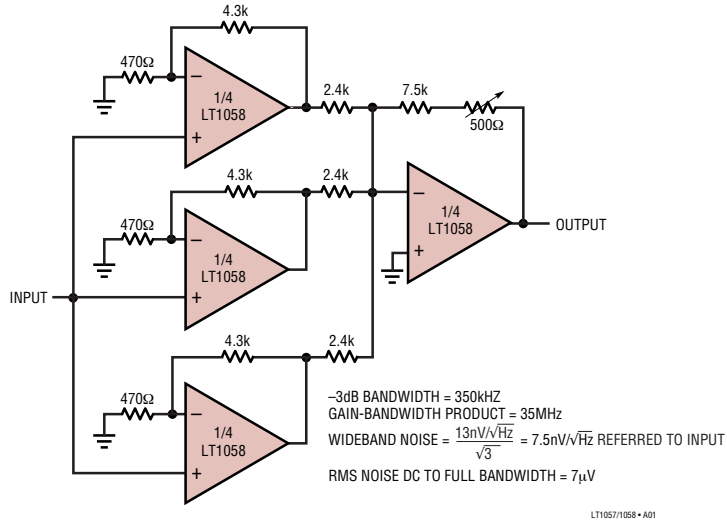


(C) LT1057/LT1058 Output

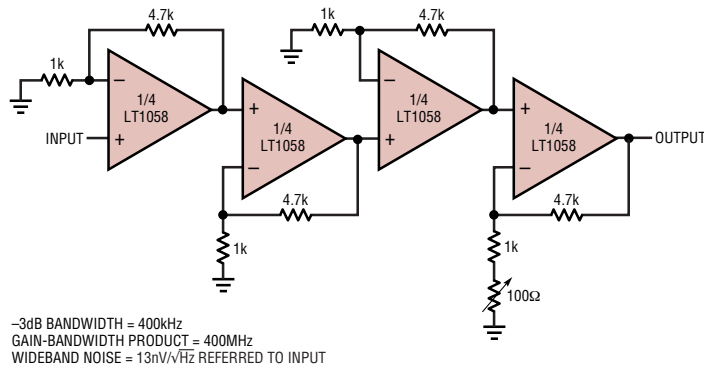
All Photos 5V/Div Vertical Scale, 50 μs /Div Horizontal Scale

TYPICAL APPLICATIONS

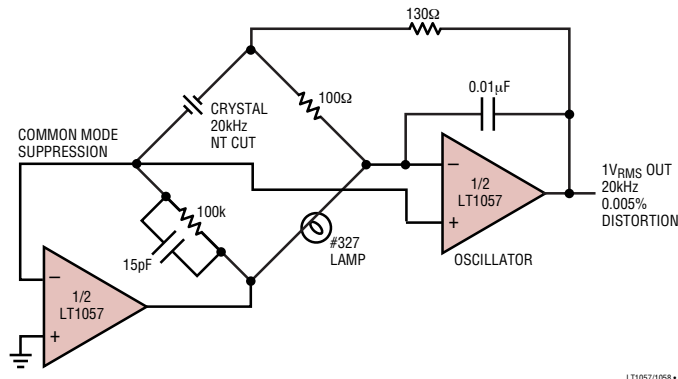
Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



Wideband, High Input Impedance, Gain = 1000 Amplifier

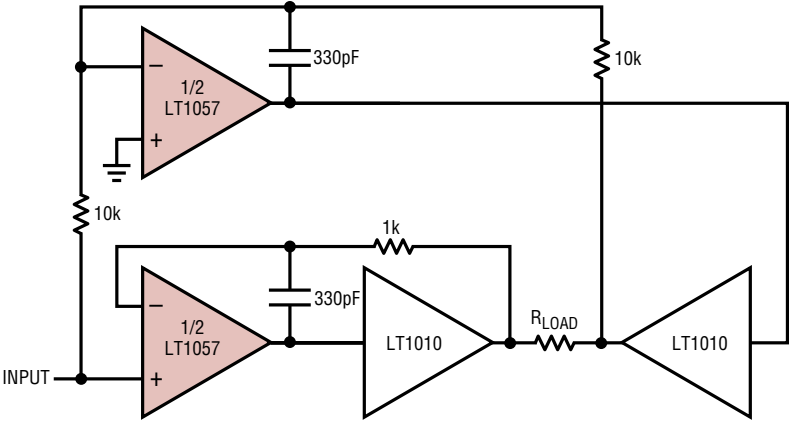


Low Distortion, Crystal Stabilized Oscillator



TYPICAL APPLICATIONS

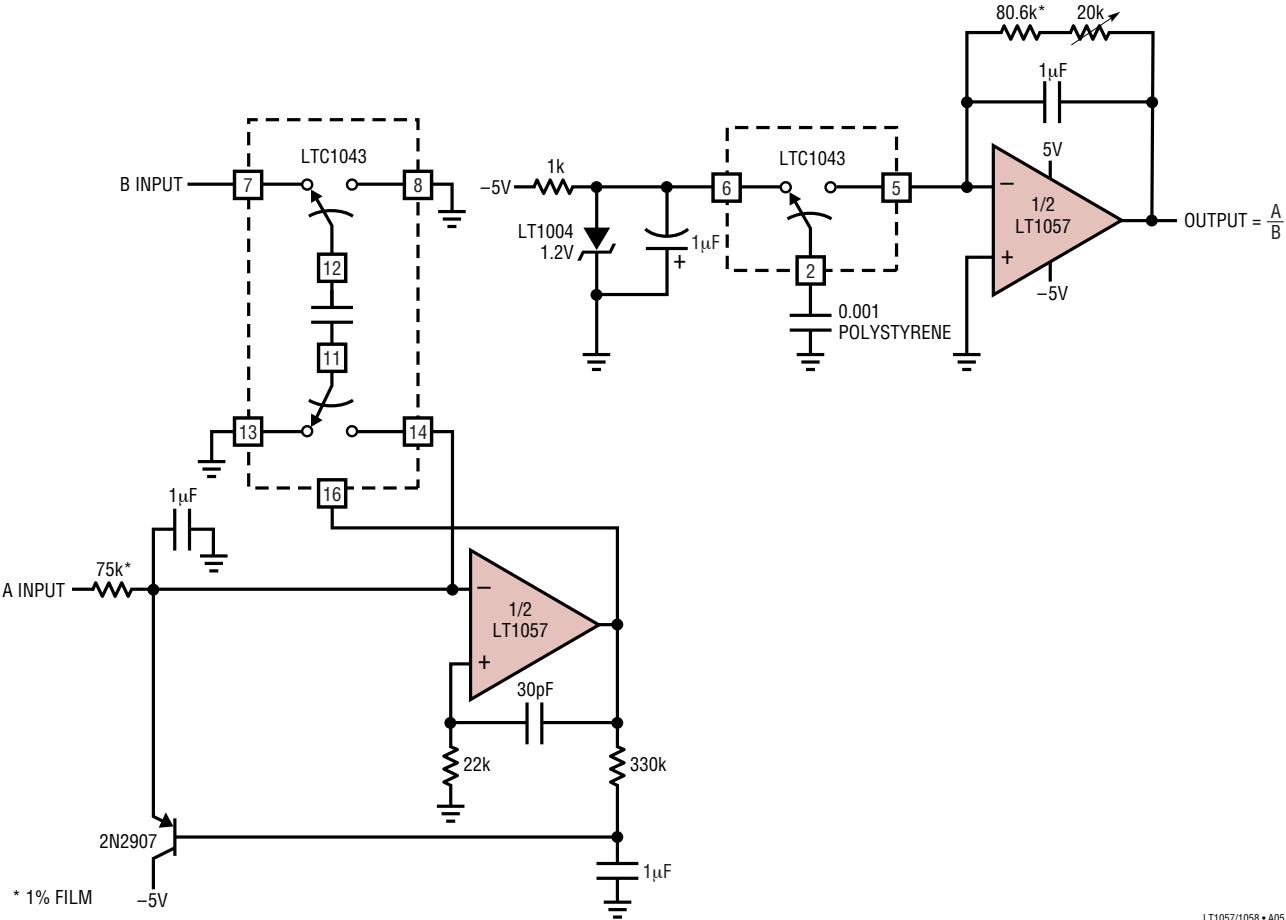
Fast, Precision Bridge Amplifier



SLEW RATE = 14V/ μ s
OUTPUT CURRENT TO LOAD = 150mA
LOAD CAPACITANCE: UP TO 1 μ F

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Analog Divider



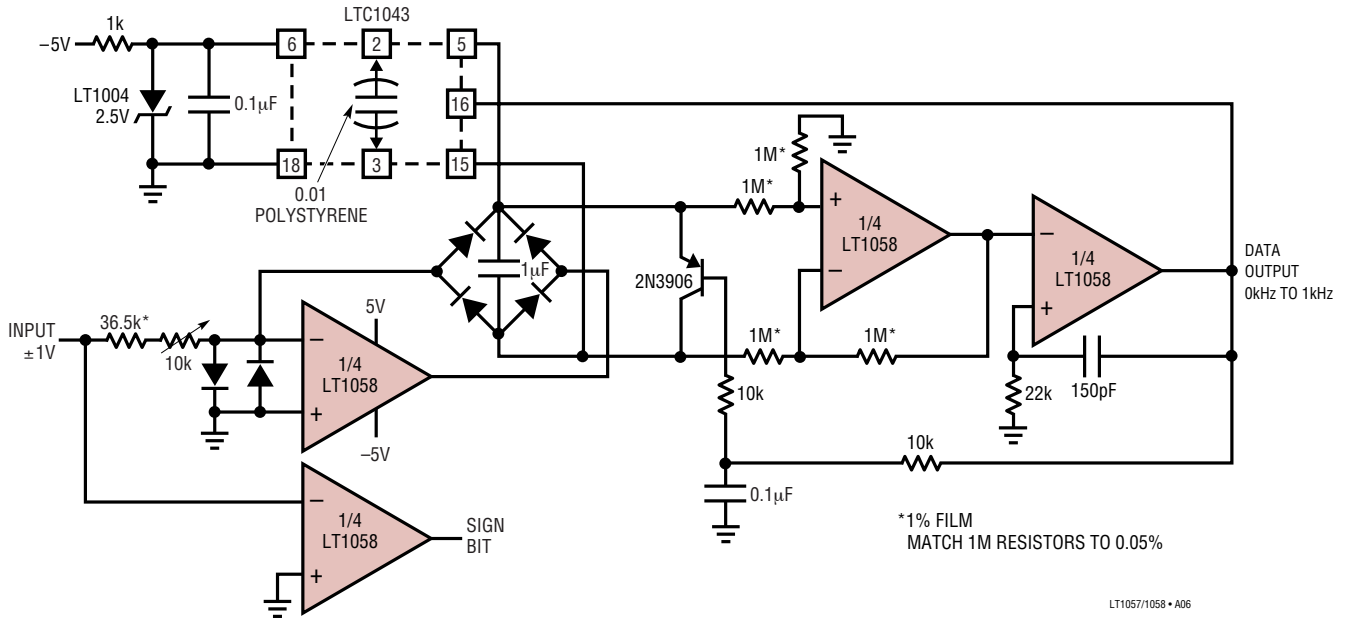
* 1% FILM

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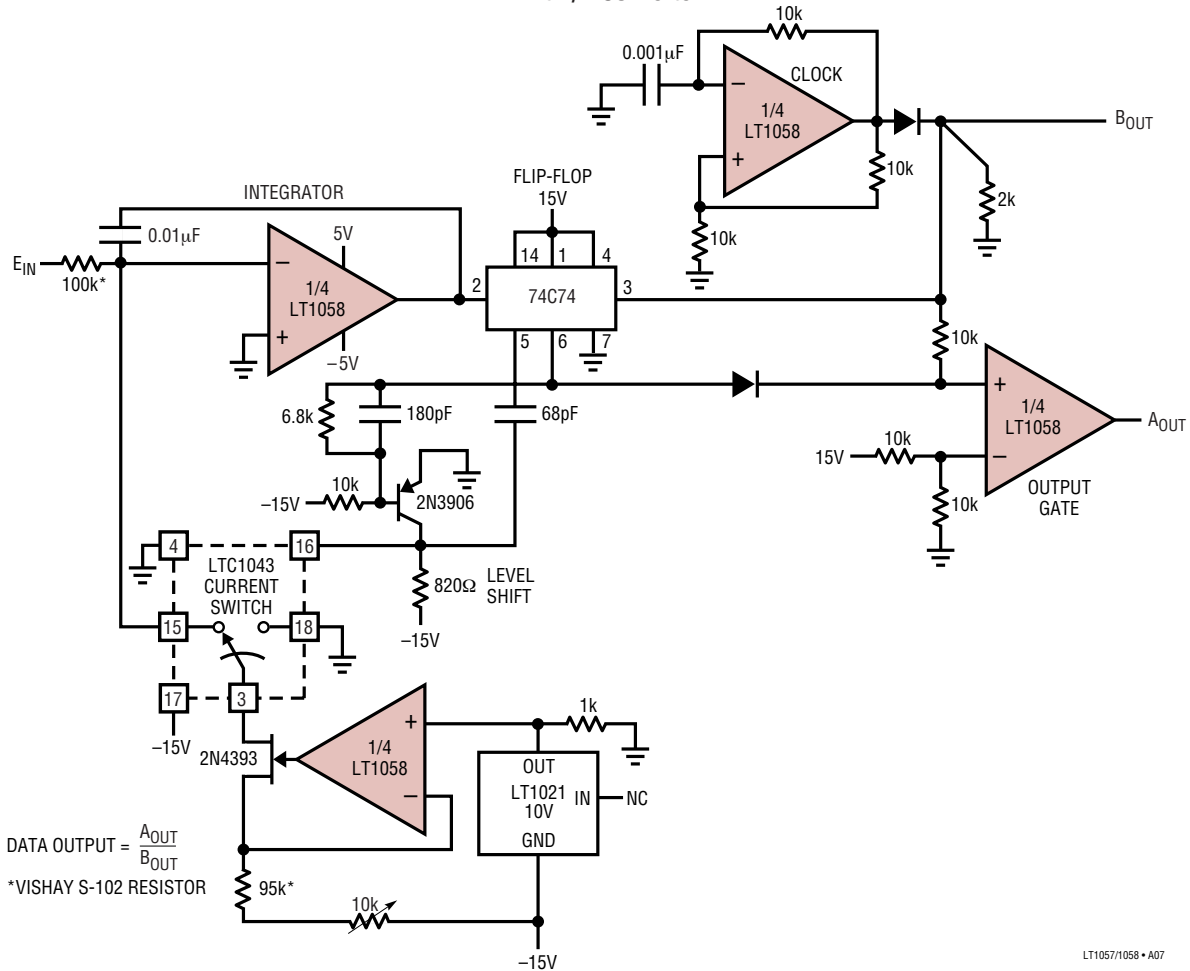
10578fa

TYPICAL APPLICATIONS

Bipolar Input (AC) V/F Converter

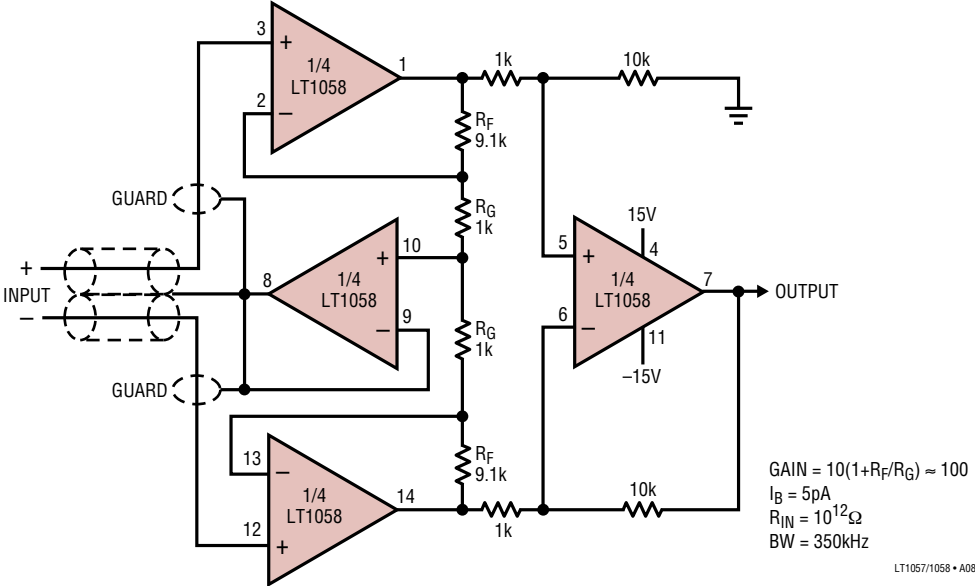


12-Bit A/D Converter

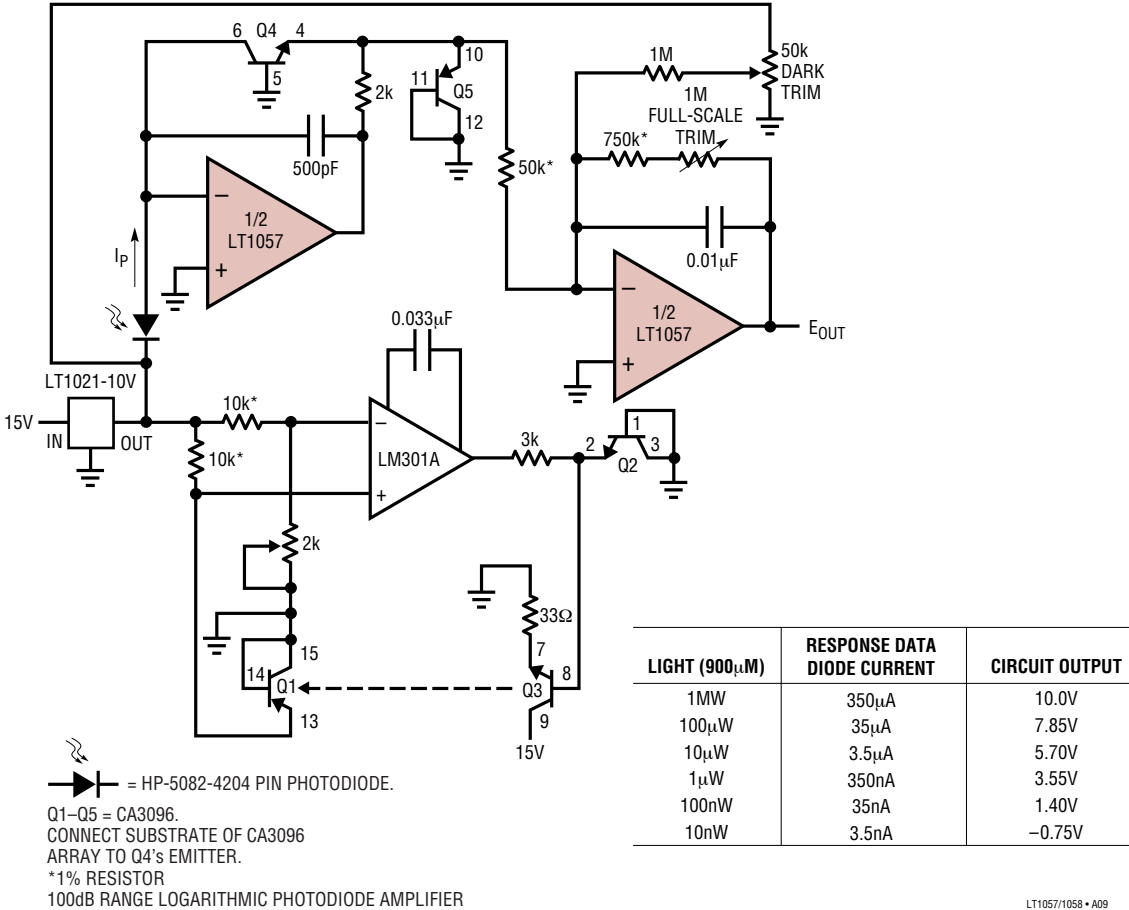


TYPICAL APPLICATIONS

Instrumentation Amplifier with Shield Driver

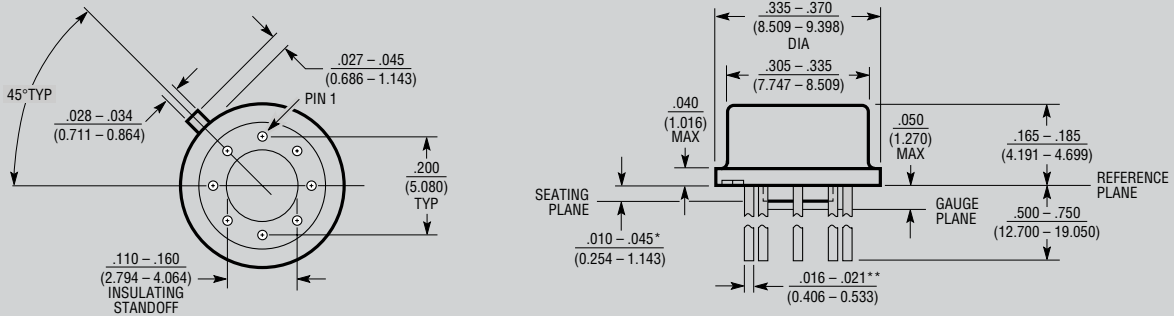


100dB Range Logarithmic Photodiode Amplifier



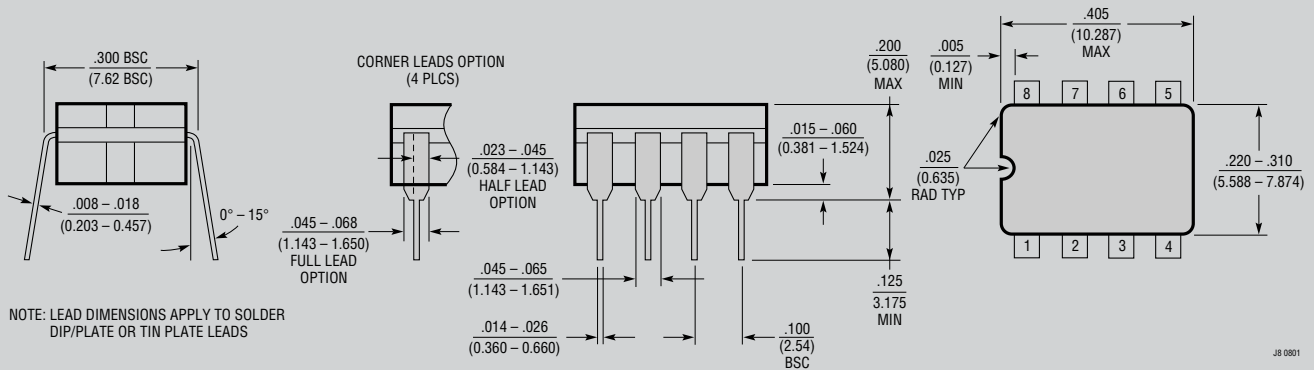
PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
 (Reference LTC DWG # 05-08-1320)

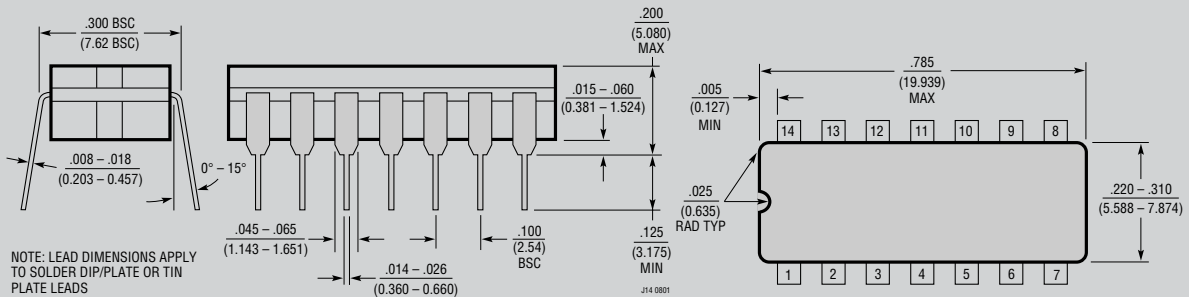


* LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE
 ** FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{.016 - .024}{(0.406 - 0.610)}$ H8(TO-5) 0.200 PCD 0801

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
 (Reference LTC DWG # 05-08-1110)



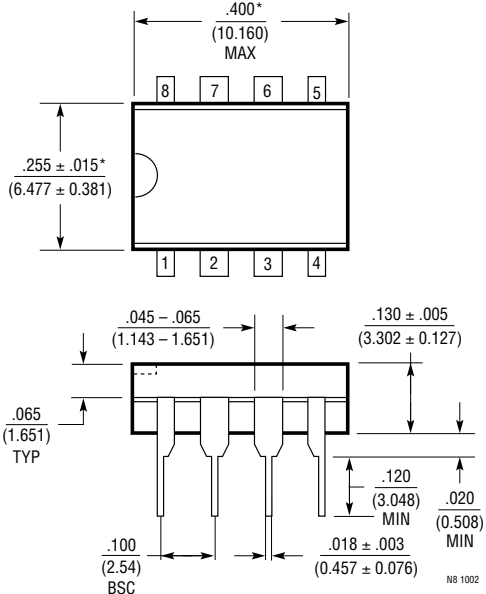
J Package
14-Lead CERDIP (Narrow .300 Inch, Hermetic)
 (Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGES

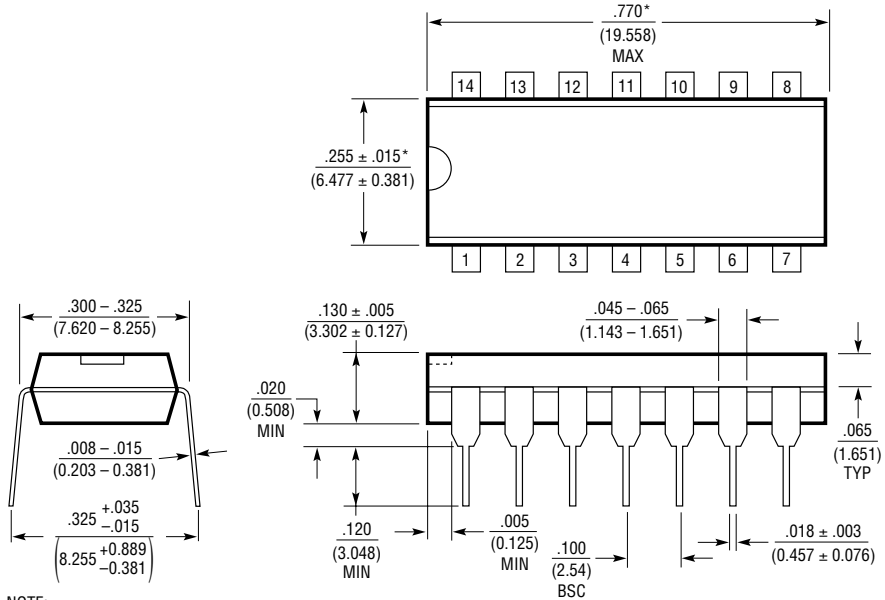
PACKAGE DESCRIPTION

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package 14-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)

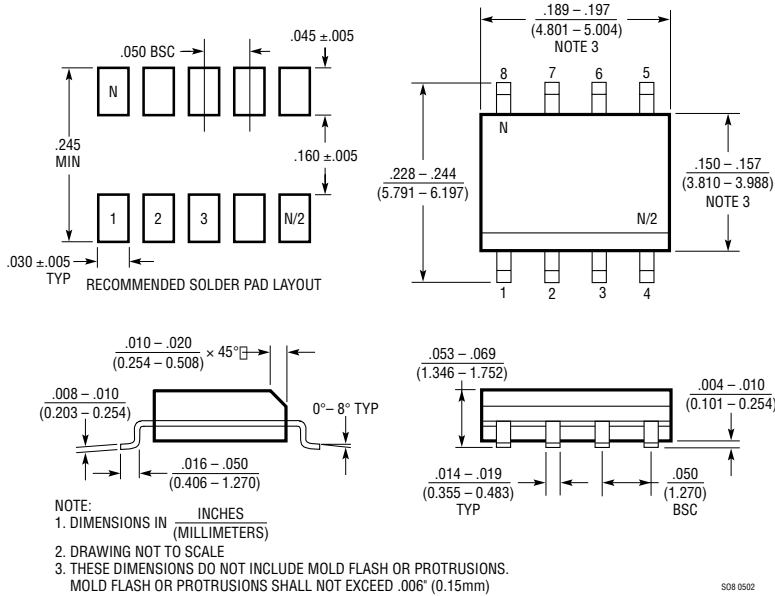


NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N14 1002

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1610)



SW Package
16-Lead Plastic Small Outline (Wide .300 Inch)
 (Reference LTC DWG # 05-08-1620)

