National Semiconductor

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# LMC6035/LMC6036
# Low Power 2.7V Single Supply CMOS Operational Amplifiers

## General Description

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. Both allow for single supply operation and are guaranteed for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its guaranteed 2.7V operation. This provides a "comfort zone" for adequate operation at voltages significantly below 2.7V. Its ultra low input currents ($I_{IN}$) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

## Features

(Typical Unless Otherwise Noted)

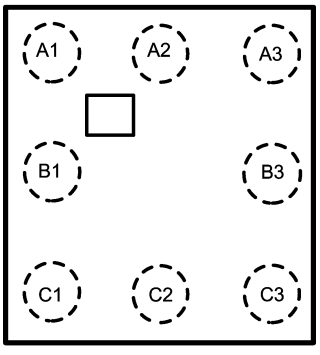
- LMC6035 in micro SMD Package
- Guaranteed 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20fA
- Rail-to-Rail Output Swing
  @ 600Ω: 200mV from either rail at 2.7V
  @ 100kΩ: 5mV from either rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  -0.1V to 2.3V at $V_S$ = 2.7V
- Low Distortion: 0.01% at 10kHz
- LMC6035 Dual LMC6036 Quad
- See AN-1112 for micro SMD considerations

## Applications

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation

## Connection Diagram

**8-Bump microSMD**

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**Top View**
**(Bump Side Down)**

## microSMD Connection Table

| Bump Number | LM6035IBP<br>LMC6035IBPX | LMC6035ITL<br>LMC6035ITLX |
|---|---|---|
| A1 | OUTPUT A | OUTPUT B |
| B1 | IN $A^-$ | $V^+$ |
| C1 | IN $A^+$ | OUTPUT A |
| C2 | $V^-$ | IN $A^-$ |
| C3 | IN $B^+$ | IN $A^+$ |
| B3 | IN $B^-$ | $V^-$ |
| A3 | OUTPUT B | IN $B^+$ |
| A2 | $V^+$ | IN $B^-$ |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance (Note 2) | |
| Human Body Model | 3000V |
| Machine Model | 300V |
| Differential Input Voltage | ± Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to $V^+$ | (Note 8) |
| Output Short Circuit to $V^-$ | (Note 3) |
| Lead Temperature (soldering, 10 sec.) | 260˚C |
| Current at Output Pin | ±18mA |
| Current at Input Pin | ±5mA |
| Current at Power Supply Pin | 35mA |
| Storage Temperature Range | −65˚C to +150˚C |
| Junction Temperature (Note 4) | 150˚C |

## Operating Ratings (Note 1)

| | |
|---|---|
| Supply Voltage | 2.0V to 15.5V |
| Temperature Range | |
| LMC6035I and LMC6036I | $-40˚C \le T_J \le +85˚C$ |
| Thermal Resistance ($\theta_{JA}$) | |
| 8-pin MSOP | 230˚C/W |
| 8-pin SOIC | 175˚C/W |
| 14-pin SOIC | 127˚C/W |
| 14-pin TSSOP | 137˚C/W |
| 8-Bump (6 mil) micro SMD | 220˚C/W |
| 8-Bump (12 mil) Thin micro SMD | 220˚C/W |

## DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.0V, $V_O$ = 1.35V and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | LMC6035I/LMC6036I | | | Units |
|---|---|---|---|---|---|---|
| | | | Min (Note 6) | Typ (Note 5) | Max (Note 6) | |
| $V_{OS}$ | Input Offset Voltage | | | 0.5 | 5<br>**6** | mV |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | | 2.3 | | µV/˚C |
| $I_{IN}$ | Input Current | (Note 11) | | 0.02 | **90** | pA |
| $I_{OS}$ | Input Offset Current | (Note 11) | | 0.01 | **45** | PA |
| $R_{IN}$ | Input Resistance | | | > 10 | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0.7V \le V_{CM} \le 12.7V$,<br>$V^+ = 15V$ | 63<br>**60** | 96 | | dB |
| +PSRR | Positive Power Supply Rejection Ratio | $5V \le V^+ \le 15V$,<br>$V_O = 2.5V$ | 63<br>**60** | 93 | | dB |
| −PSRR | Negative Power Supply Rejection Ratio | $0V \le V^- \le -10V$,<br>$V_O = 2.5V$, $V^+ = 5V$ | 74<br>**70** | 97 | | dB |
| $V_{CM}$ | Input Common-Mode Voltage Range | $V^+ = 2.7V$<br>For CMRR ≥ 40dB | | −0.1 | 0.3<br>**0.5** | V |
| | | | 2.0<br>**1.7** | 2.3 | | |
| | | $V^+ = 3V$<br>For CMRR ≥ 40dB | | −0.3 | 0.1<br>**0.3** | V |
| | | | 2.3<br>**2.0** | 2.6 | | |
| | | $V^+ = 5V$<br>For CMRR ≥ 50dB | | −0.5 | −0.2<br>**0.0** | V |
| | | | 4.2<br>**3.9** | 4.5 | | |
| | | $V^+ = 15V$<br>For CMRR ≥ 50dB | | −0.5 | −0.2<br>**0.0** | V |
| | | | 14.0<br>**13.7** | 14.4 | | |

## DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.0V, $V_O$ = 1.35V and $R_L$ > 1MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | | LMC6035I/LMC6036I Min (Note 6) | LMC6035I/LMC6036I Typ (Note 5) | LMC6035I/LMC6036I Max (Note 6) | Units |
|---|---|---|---|---|---|---|---|
| $A_V$ | Large Signal Voltage Gain (Note 7) | $R_L$ = 600Ω | Sourcing | 100<br>**75** | 1000 | | V/mV |
| | | | Sinking | 25<br>**20** | 250 | | V/mV |
| | | $R_L$ = 2kΩ | Sourcing | | 2000 | | V/mV |
| | | | Sinking | | 500 | | V/mV |
| $V_O$ | Output Swing | $V^+$ = 2.7V<br>$R_L$ = 600Ω to 1.35V | | 2.0<br>**1.8** | 2.5 | | V |
| | | | | | 0.2 | 0.5<br>**0.7** | |
| | | $V^+$ = 2.7V<br>$R_L$ = 2kΩ to 1.35V | | 2.4<br>**2.2** | 2.62 | | V |
| | | | | | 0.07 | 0.2<br>**0.4** | |
| | | $V^+$ = 15V<br>$R_L$ = 600Ω to 7.5V | | 13.5<br>**13.0** | 14.5 | | V |
| | | | | | 0.36 | 1.25<br>**1.50** | |
| | | $V^+$ = 15V,<br>$R_L$ = 2 kΩ to 7.5V | | 14.2<br>**13.5** | 14.8 | | V |
| | | | | | 0.12 | 0.4<br>**0.5** | |
| $I_O$ | Output Current | $V_O$ = 0V | Sourcing | 4<br>**3** | 8 | | mA |
| | | $V_O$ = 2.7V | Sinking | 3<br>**2** | 5 | | |
| $I_S$ | Supply Current | LMC6035 for Both Amplifiers<br>$V_O$ = 1.35V | | | 0.65 | 1.6<br>**1.9** | mA |
| | | LMC6036 for All Four Amplifiers<br>$V_O$ = 1.35V | | | 1.3 | 2.7<br>**3.0** | |

## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.0V, $V_O$ = 1.35V and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Units |
|---|---|---|---|---|
| SR | Slew Rate | (Note 9) | 1.5 | V/µs |
| GBW | Gain Bandwidth Product | $V^+$ = 15V | 1.4 | MHz |
| $\theta_m$ | Phase Margin | | 48 | ° |
| $G_m$ | Gain Margin | | 17 | dB |
| | Amp-to-Amp Isolation | (Note 10) | 130 | dB |
| $e_n$ | Input-Referred Voltage Noise | f = 1kHz<br>$V_{CM}$ = 1V | 27 | $nV/\sqrt{Hz}$ |
| $i_n$ | Input Referred Current Noise | f = 1kHz | 0.2 | $fA/\sqrt{Hz}$ |
| THD | Total Harmonic Distortion | f = 10kHz, $A_V$ = −10<br>$R_L$ = 2kΩ, $V_O$ = 8 $V_{PP}$ | 0.01 | % |

## AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = 1.0V, $V_O$ = 1.35V and $R_L$ > 1 MΩ. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Units |
|---|---|---|---|---|
| | | $V^+$ = 10V | | |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human body model, 1.5kΩ in series with 100pF.

**Note 3:** Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 30mA over long term may adversely affect reliability.

**Note 4:** The maximum power dissipation is a function of $T_{J(MAX)}$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board with no air flow.

**Note 5:** Typical Values represent the most likely parametric norm or one sigma value.

**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:** $V^+$ = 15V, $V_{CM}$ = 7.5V and $R_L$ connected to 7.5V. For Sourcing tests, 7.5V ≤ $V_O$ ≤ 11.5V. For Sinking tests, 3.5V ≤ $V_O$ ≤ 7.5V.

**Note 8:** Do not short circuit output to $V^+$ when $V^+$ is greater than 13V or reliability will be adversely affected.

**Note 9:** $V^+$ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

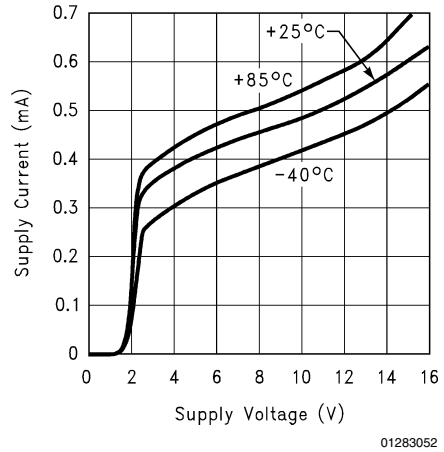
**Note 10:** Input referred, $V^+$ = 15V and $R_L$ = 100kΩ connected to 7.5V. Each amp excited in turn with 1kHz to produce $V_O$ = 12 $V_{PP}$.

**Note 11:** Guaranteed by design.

## Typical Performance Characteristics

Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C

**Supply Current vs. Supply Voltage (Per Amplifier)**

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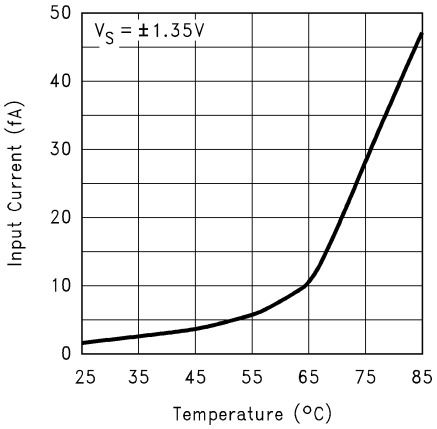
**Input Current vs. Temperature**

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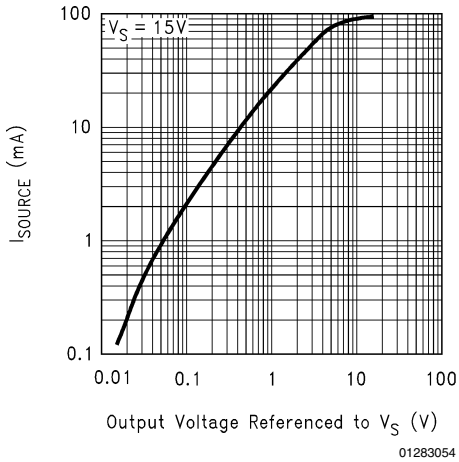
**Sourcing Current vs. Output Voltage**

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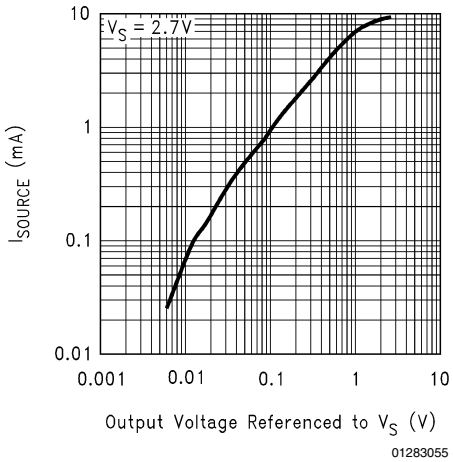
**Sourcing Current vs. Output Voltage**

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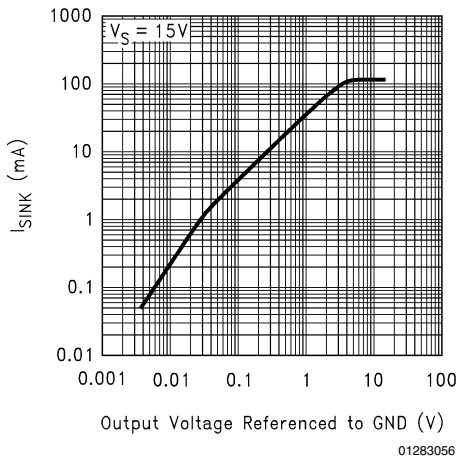
**Sinking Current vs. Output Voltage**

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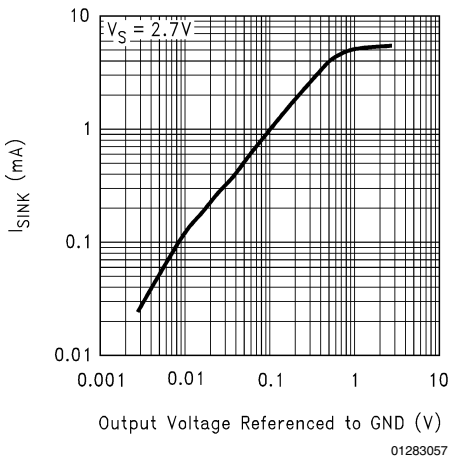
**Sinking Current vs. Output Voltage**

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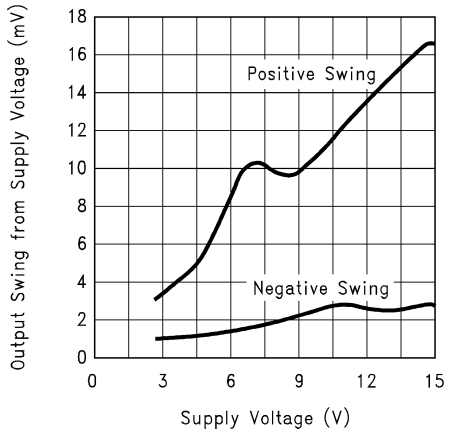
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**Output Voltage Swing vs. Supply Voltage**

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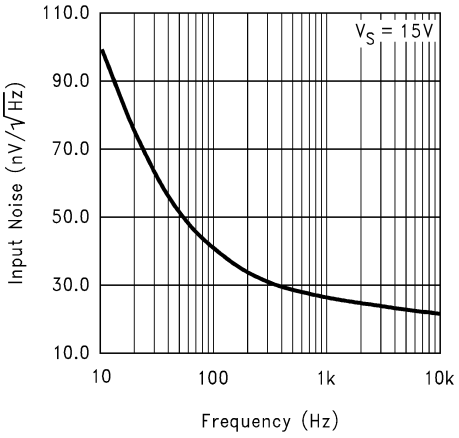
**Input Noise vs. Frequency**

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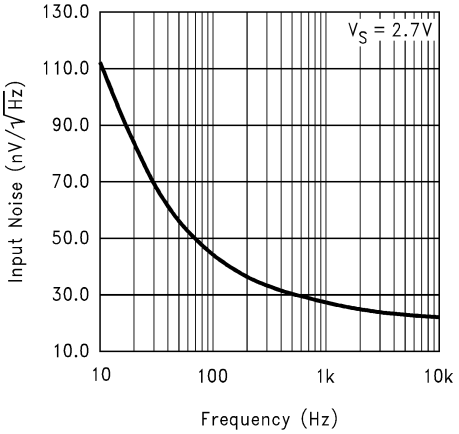
**Input Noise vs. Frequency**

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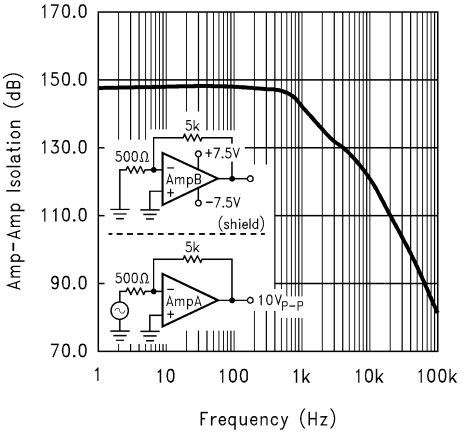
**Amp to Amp Isolation vs. Frequency**

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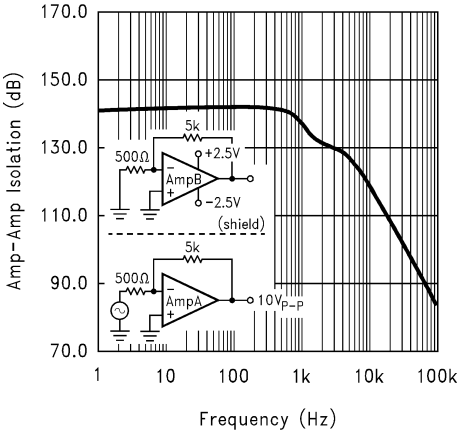
**Amp to Amp Isolation vs. Frequency**

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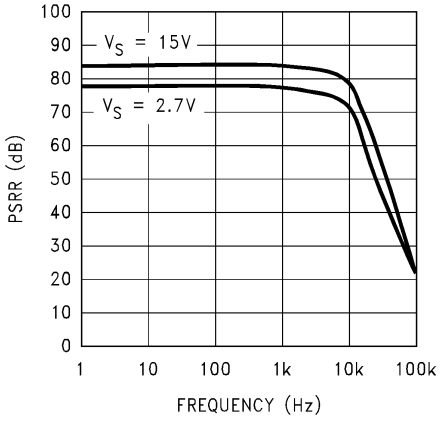
**+PSRR vs. Frequency**

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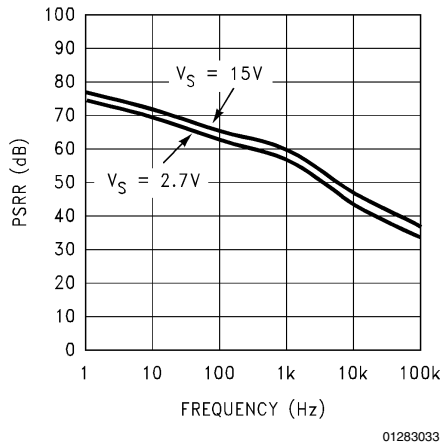
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**−PSRR vs. Frequency**

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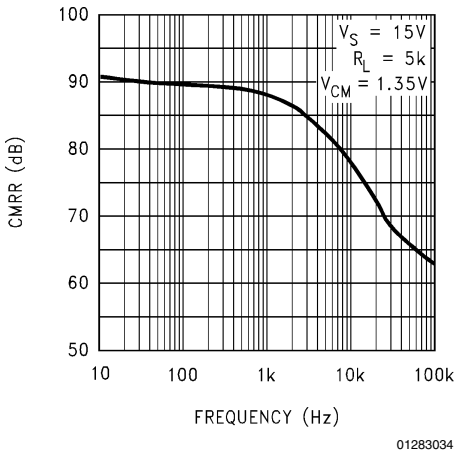
**CMRR vs. Frequency**

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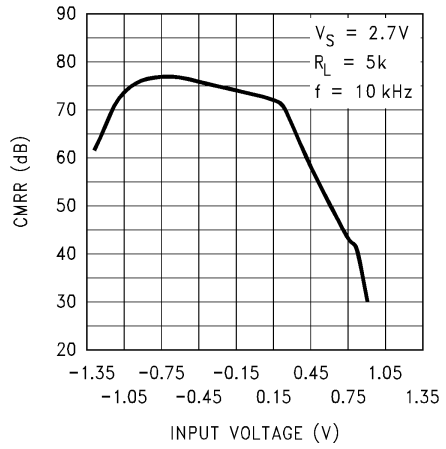
**CMRR vs. Input Voltage**

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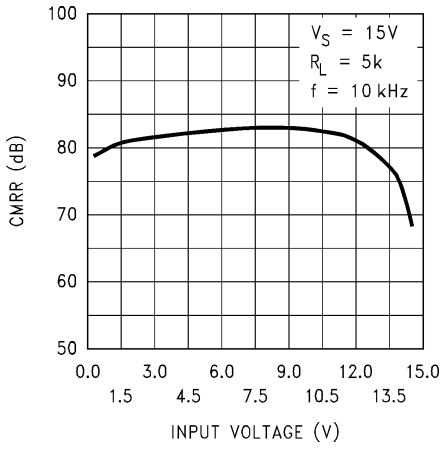
**CMRR vs. Input Voltage**

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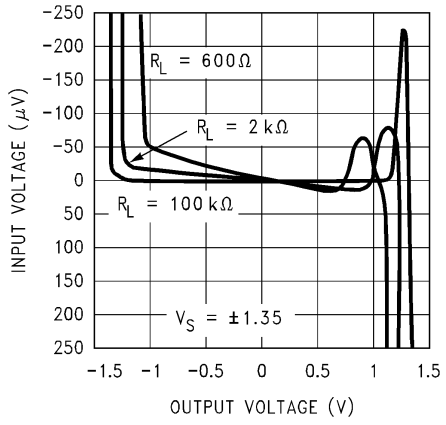
**Input Voltage vs. Output Voltage**

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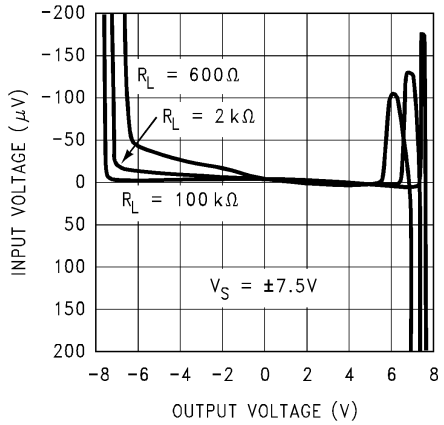
**Input Voltage vs. Output Voltage**

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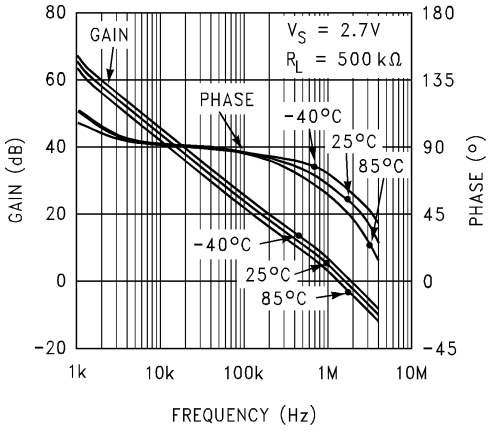
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**Frequency Response vs. Temperature**

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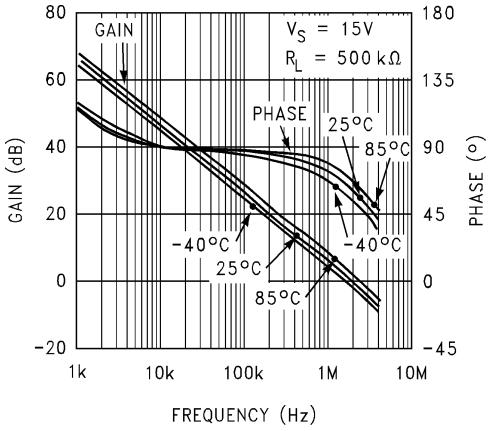
**Frequency Response vs. Temperature**

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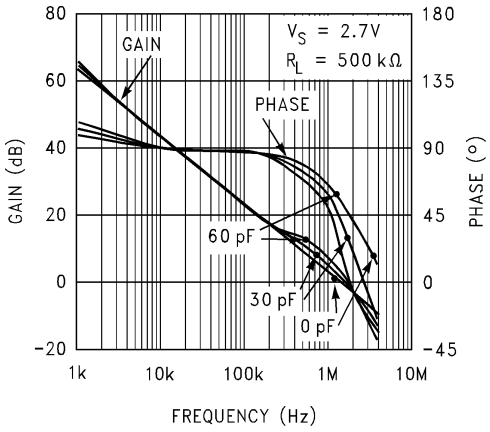
**Gain and Phase vs. Capacitive Load**

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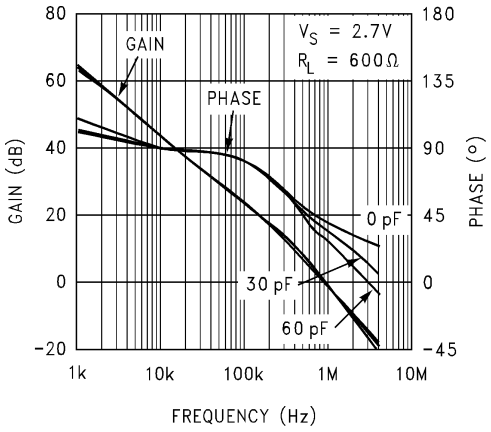
**Gain and Phase vs. Capacitive Load**

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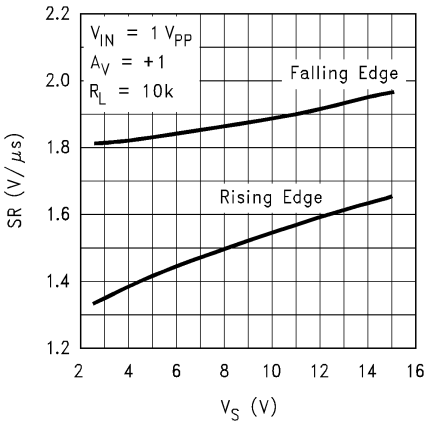
**Slew Rate vs. Supply Voltage**

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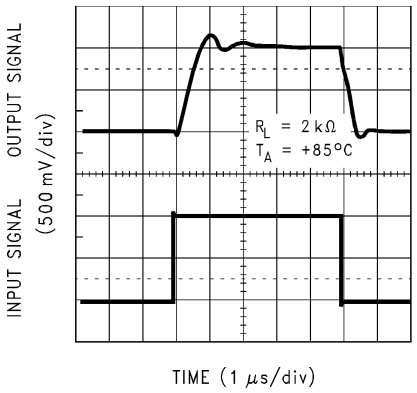
**Non-Inverting Large Signal Response**

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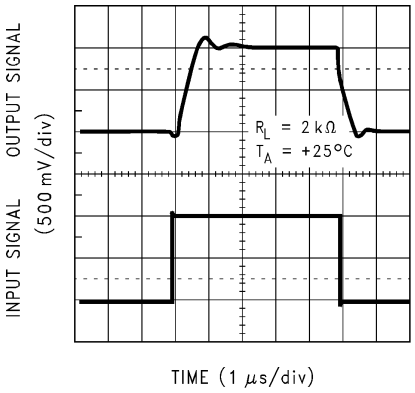
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**Non-Inverting Large Signal Response**

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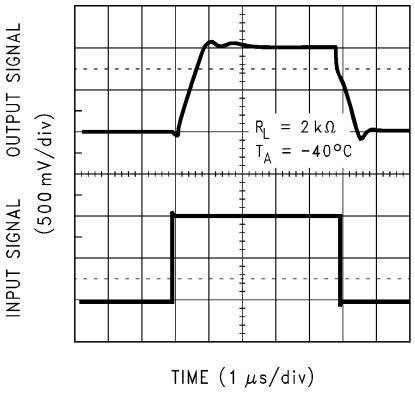
**Non-Inverting Large Signal Response**

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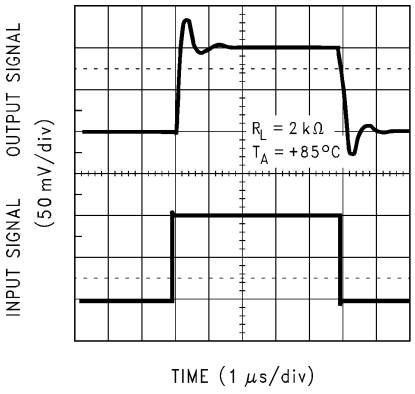
**Non-Inverting Small Signal Response**

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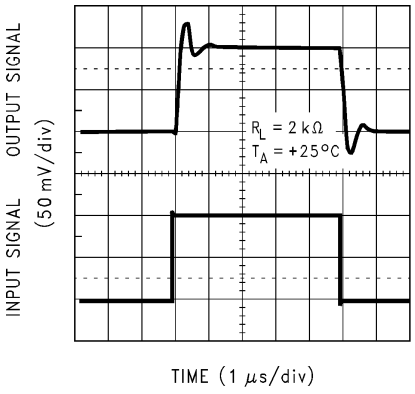
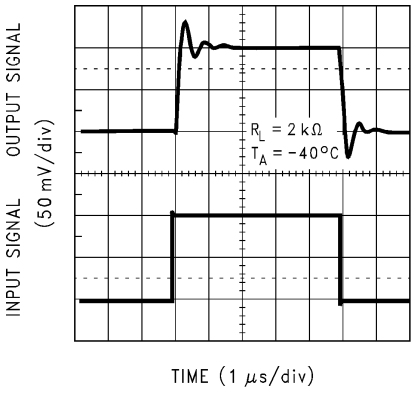
**Non-Inverting Small Signal Response**



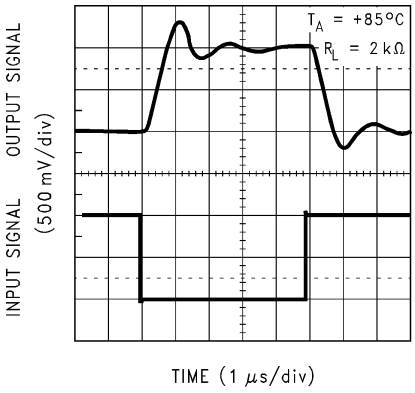

01283024

**Non-Inverting Large Signal Response**




01283025

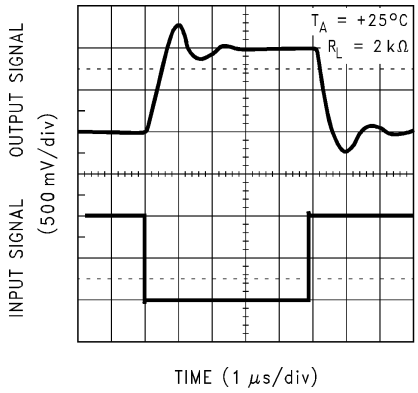
**Inverting Large Signal Response**




01283026

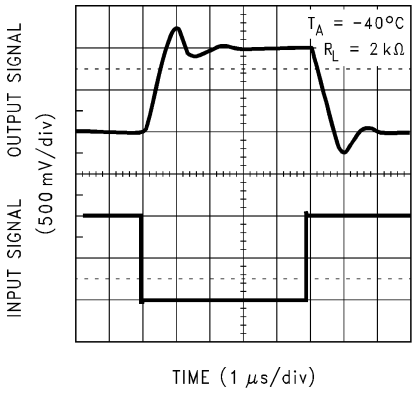
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**Inverting Large Signal Response**



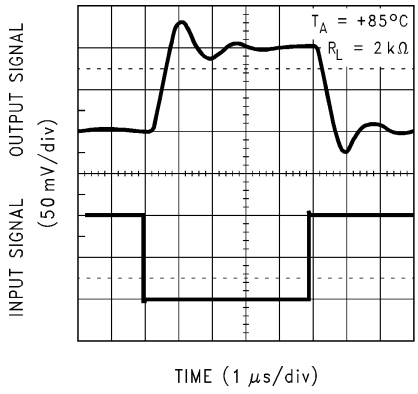

01283027

**Inverting Large Signal Response**



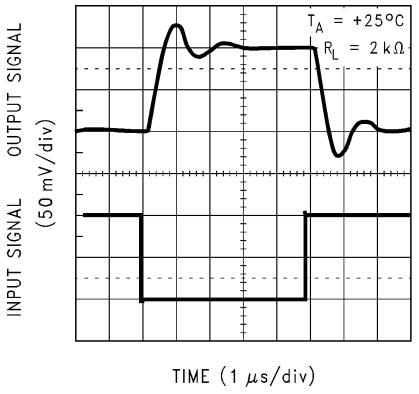

01283028

**Inverting Small Signal Response**



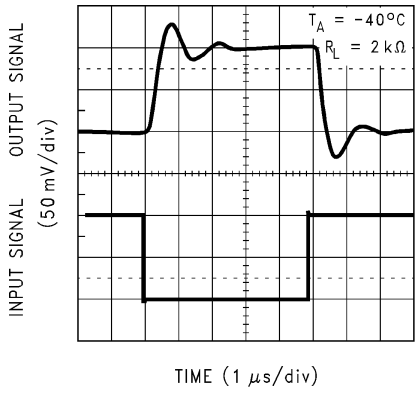

01283029

**Inverting Small Signal Response**



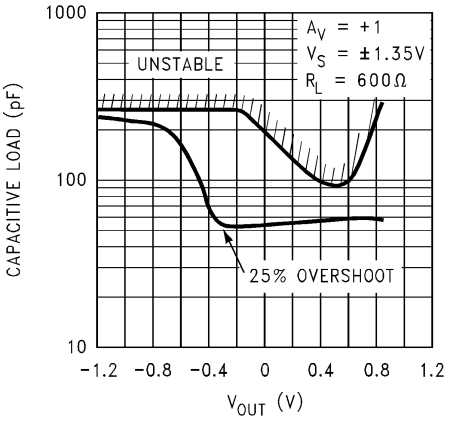

01283030

**Inverting Small Signal Response**




01283031

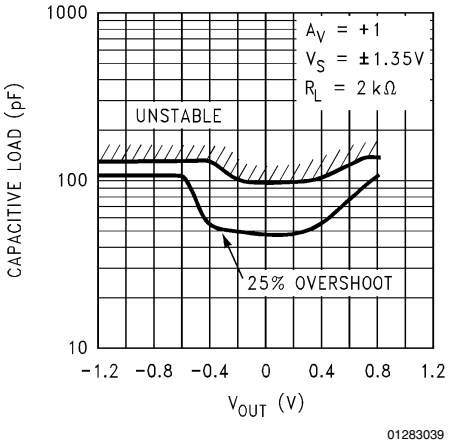
**Stability vs. Capacitive Load**




01283038

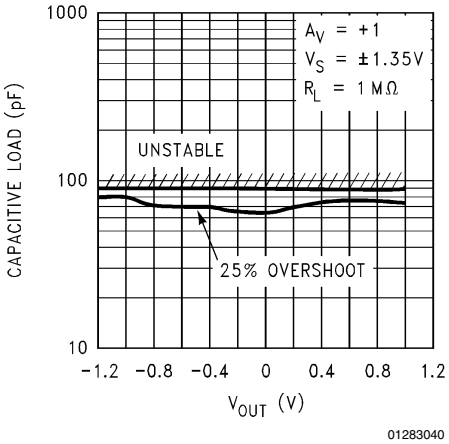
## Typical Performance Characteristics Unless otherwise specified, $V_S$ = 2.7V, single supply, $T_A$ = 25˚C (Continued)

**Stability vs. Capacitive Load**



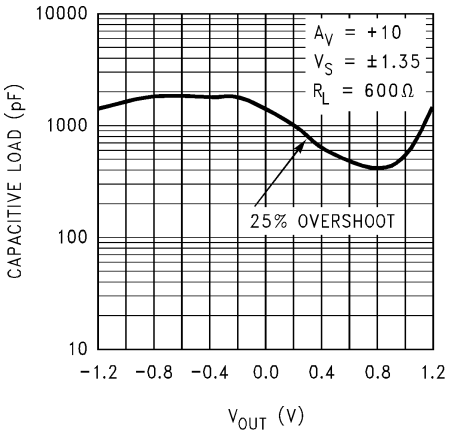

01283039

**Stability vs. Capacitive Load**



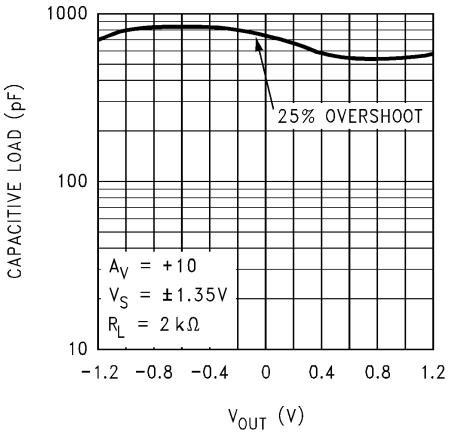

01283040

**Stability vs. Capacitive Load**



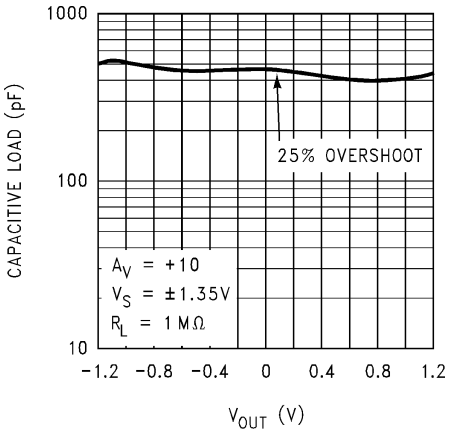

01283041

**Stability vs. Capacitive Load**




01283042

**Stability vs. Capacitive Load**




01283043

# 1.0 Application Notes

## 1.1 Background

The LMC6035/6 is exceptionally well suited for low voltage applications. A desirable feature that the LMC6035/6 brings to low voltage applications is its output drive capability—a hallmark for National's CMOS amplifiers. The circuit of *Figure 1* illustrates the drive capability of the LMC6035/6 at 3V of supply. It is a differential output driver for a one-to-one audio transformer, like those used for isolating ground from the telephone lines. The transformer (T1) loads the op amps with about 600Ω of AC load, at 1 kHz. Capacitor C1 functions to block DC from the low winding resistance of T1. Although the value of C1 is relatively high, its load reactance (Xc) is negligible compared to inductive reactance ($X_l$) of T1.

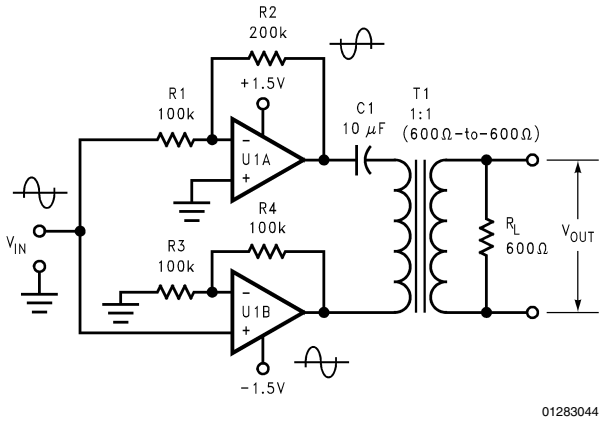



**FIGURE 1. Differential Driver**

The circuit in *Figure 1* consists of one input signal and two output signals. U1A amplifies the input with an inverting gain of –2, while the U1B amplifies the input with a non-inverting gain of +2. Since the two outputs are 180˚ out of phase with each other, the gain across the differential output is 4. As the differential output swings between the supply rails, one of the op amps sources the current to the load, while the other op amp sinks the current.

How good a CMOS op amp can sink or source a current is an important factor in determining its output swing capability. The output stage of the LMC6035/6—like many op amps—sources and sinks output current through two complementary transistors in series. This "totem pole" arrangement translates to a channel resistance ($R_{dson}$) at each supply rail which acts to limit the output swing. Most CMOS op amps are able to swing the outputs very close to the rails—except, however, under the difficult conditions of low supply voltage and heavy load. The LMC6035/6 exhibits exceptional output swing capability under these conditions.

The scope photos of *Figure 2* and *Figure 3* represent measurements taken directly at the output (relative to GND) of U1A, in *Figure 1*. *Figure 2* illustrates the output swing capability of the LMC6035, while *Figure 3* provides a benchmark comparison. (The benchmark op amp is another low voltage (3V) op amp manufactured by one of our reputable competitors.)

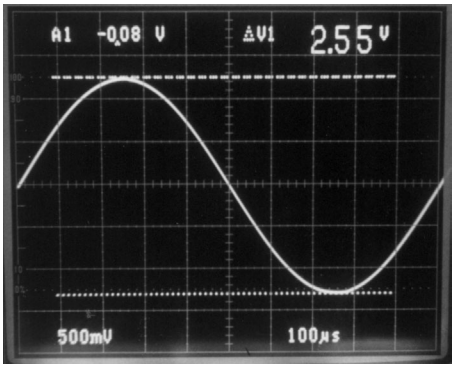



**FIGURE 2. Output Swing Performance of the LMC6035 per the Circuit of *Figure 1***

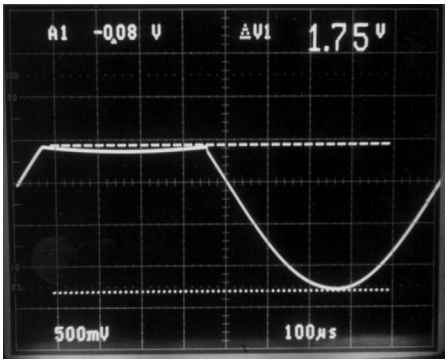



**FIGURE 3. Output Swing Performance of Benchmark Op Amp per the Circuit of *Figure 1***

Notice the superior drive capability of LMC6035 when compared with the benchmark measurement—even though the benchmark op amp uses twice the supply current.

Not only does the LMC6035/6 provide excellent output swing capability at low supply voltages, it also maintains high open loop gain ($A_{VOL}$) with heavy loads. To illustrate this, the LMC6035 and the benchmark op amp were compared for their distortion performance in the circuit of *Figure 1*. The graph of *Figure 4* shows this comparison. The y-axis represents percent Total Harmonic Distortion (THD plus noise) across the loaded secondary of T1. The x-axis represents the input amplitude of a 1 kHz sine wave. (Note that T1 loses about 20% of the voltage to the voltage divider of $R_L$ (600Ω) and T1's winding resistances—a performance deficiency of the transformer.)

# 1.0 Application Notes (Continued)

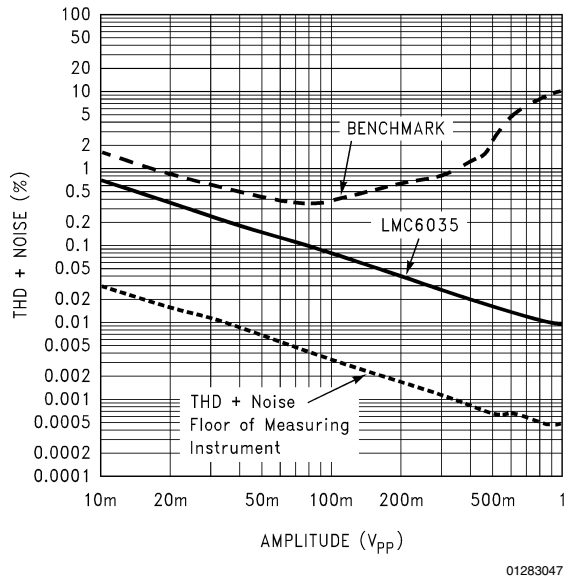



**FIGURE 4. THD+Noise Performance of LMC6035 and "Benchmark" per Circuit of *Figure 1***

*Figure 4* shows the superior distortion performance of LMC6035/6 over that of the benchmark op amp. The heavy loading of the circuit causes the $A_{VOL}$ of the benchmark part to drop significantly which causes increased distortion.

## 1.2 APPLICATION CIRCUITS

### 1.2.1 Low-Pass Active Filter

A common application for low voltage systems would be active filters, in cordless and cellular phones for example. The ultra low input currents ($I_{IN}$) of the LMC6035/6 makes it well suited for low power active filter applications, because it allows the use of higher resistor values and lower capacitor values. This reduces power consumption and space.

*Figure 5* shows a low pass, active filter with a Butterworth (maximally flat) frequency response. Its topology is a Sallen and Key filter with unity gain. Note the normalized component values in parenthesis which are obtainable from standard filter design handbooks. These values provide a 1Hz cutoff frequency, but they can be easily scaled for a desired cutoff frequency ($f_c$). The bold component values of *Figure 5* provide a cutoff frequency of 3kHz. An example of the scaling procedure follows *Figure 5*.

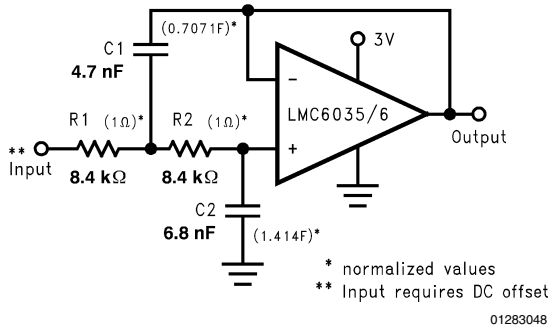



**FIGURE 5. 2-Pole, 3kHz, Active, Sallen and Key, Lowpass Filter with Butterworth Response**

#### 1.2.1.1 Low-Pass Frequency Scaling Procedure

The actual component values represented in bold of *Figure 5* were obtained with the following scaling procedure:

1. First determine the frequency scaling factor (FSF) for the desired cutoff frequency. Choosing $f_c$ at 3kHz, provides the following FSF computation:

   FSF = $2\pi$ x 3kHz $_{(\text{desired cutoff freq.})}$ = 18.84 x $10^3$
2. Then divide all of the normalized capacitor values by the FSF as follows: C1' = $C_{(\text{Normalized})}$/FSF C1' = 0.707/18.84 x $10^3$ = 37.93 x $10^{-6}$ C2' = 1.414/18.84 x $10^3$ = 75.05 x $10^{-6}$ (C1' and C2': prior to impedance scaling)
3. Last, choose an impedance scaling factor (Z). This Z factor can be calculated from a standard value for C2. Then Z can be used to determine the remaining component values as follows:

Z = C2'/$C2_{(\text{chosen})}$ = 75.05 x $10^{-6}$/**6.8nF** = 8.4k

C1 = C1'/Z = 37.93 x $10^{-6}$ /8.4k = 4.52nF

(Standard capacitor value chosen for C1 is **4.7nF** ) R1 = $R1_{(\text{normalized})}$ x Z = 1Ω x 8.4k = 8.4kΩ R2 = $R2_{(\text{normalized})}$ x Z = 1Ω x 8.4k = 8.4kΩ

(Standard value chosen for R1 and R2 is **8.45kΩ** )

### 1.2.2 High Pass Active Filter

The previous low-pass filter circuit of *Figure 5* converts to a high-pass active filter per *Figure 6*.

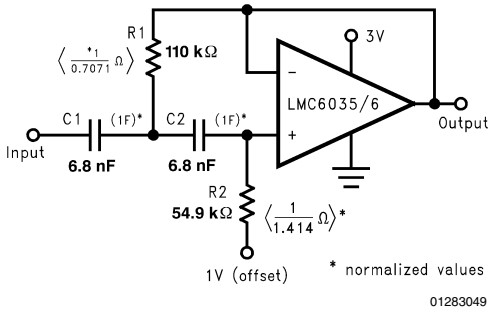



**FIGURE 6. 2 Pole, 300Hz, Sallen and Key, High-Pass Filter**

# 1.0 Application Notes (Continued)

#### 1.2.2.1 High-Pass Frequency Scaling Procedure

Choose a standard capacitor value and scale the impedances in the circuit according to the desired cutoff frequency (300Hz) as follows: C = C1 = C2 Z = 1 Farad/$C_{(chosen)}$ x 2π x (desired cutoff freq.) = 1 Farad/**6.8nF** x 2π x 300 Hz = 78.05k

R1 = Z x $R1_{(normalized)}$ = 78.05k x (1/0.707) = 110.4kΩ

(Standard value chosen for R1 is **110k**Ω )

R2 = Z x $R2_{(normalized)}$ = 78.05k x (1/1.414) = 55.2kΩ

(Standard value chosen for R1 is **54.9k**Ω )

#### 1.2.3 Dual Amplifier Bandpass Filter

The dual amplifier bandpass (DABP) filter features the ability to independently adjust $f_c$ and Q. In most other bandpass topologies, the $f_c$ and Q adjustments interact with each other. The DABP filter also offers both low sensitivity to component values and high Qs. The following application of *Figure 7*, provides a 1kHz center frequency and a Q of 100.

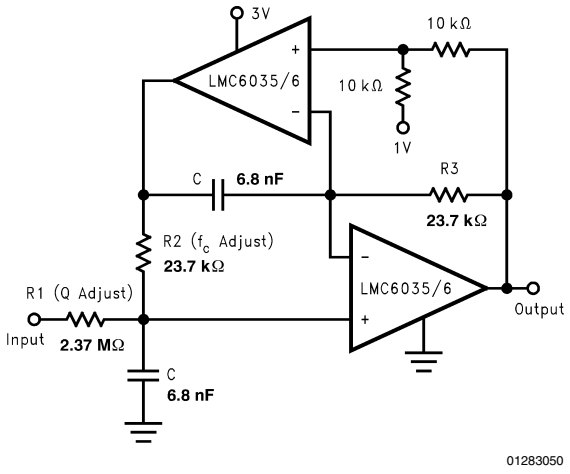



**FIGURE 7. 2 Pole, 1kHz Active, Bandpass Filter**

#### 1.2.3.1 DABP Component Selection Procedure

Component selection for the DABP filter is performed as follows:

1. First choose a center frequency ($f_c$). *Figure 7* represents component values that were obtained from the following computation for a center frequency of 1kHz. R2 = R3 = $1/(2\pi f_c C)$ Given: $f_c$ = 1kHz and $C_{(chosen)}$ = **6.8nF** R2 = R3 = 1/(2π x 3kHz x 6.8nF) = 23.4kΩ
   (Chosen standard value is **23.7k**Ω )
2. Then compute R1 for a desired Q ($f_c$/BW) as follows: R1 = Q x R2. Choosing a Q of 100, R1 = 100 x 23.7kΩ = **2.37M**Ω**.**

### 1.3 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with < 1000pA of leakage current requires special layout of the PC board. If one wishes to take advantage of the ultra-low bias current of the LMC6035/6, typically < 0.04pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may at times appear acceptably low. Under conditions of high humidity, dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6035 or LMC6036 inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See *Figure 8*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the amplifiers actual performance. However, if a guard ring is held within 5mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 9a, b, c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 9 d*.

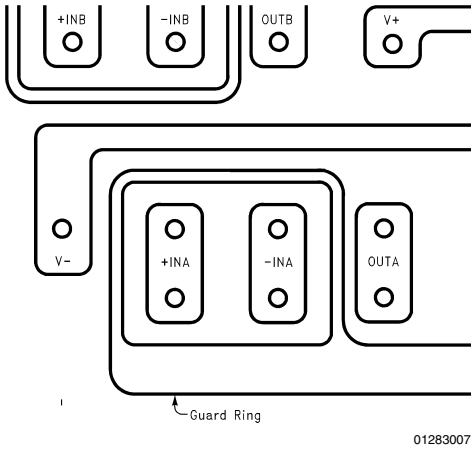



**FIGURE 8. Example, using the LMC6036 of Guard Ring in P.C. Board Layout**

## 1.0 Application Notes (Continued)

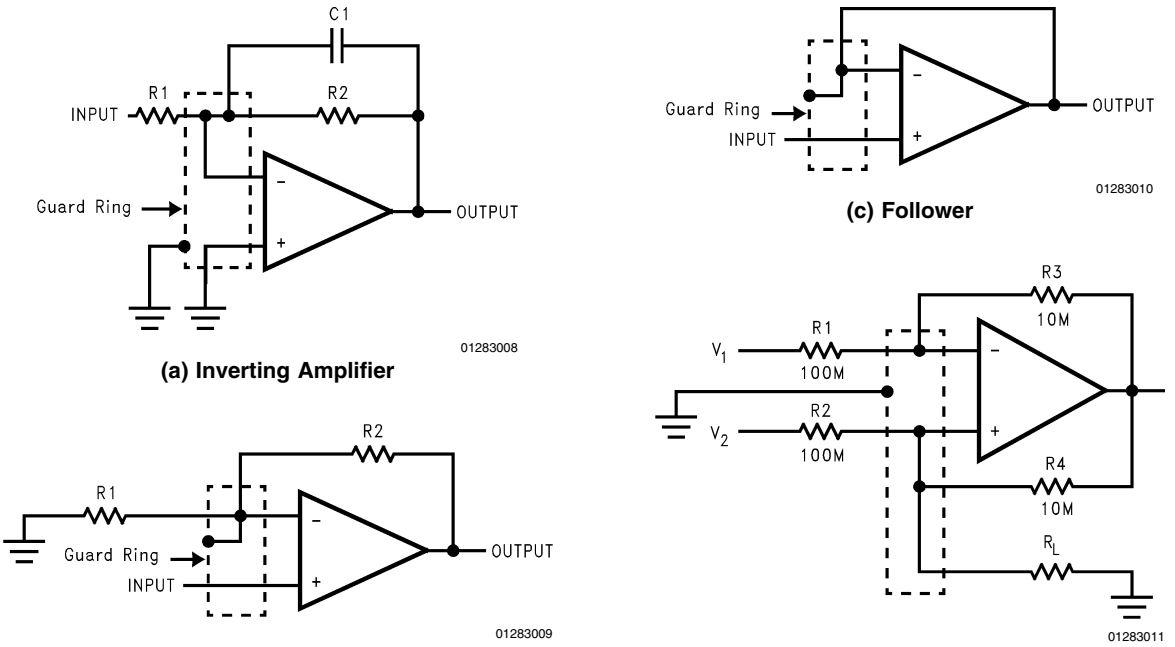



**FIGURE 9. Guard Ring Connections**

### 1.3.1 CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6035/6 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 10*, the addition of a small resistor (50Ω–100Ω) in series with the op amp's output, and a capacitor (5pF–10pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

### 1.4 Micro SMD Considerations

Contrary to what might be guessed, the micro SMD package does not follow the trend of smaller packages having higher thermal resistance. LMC6035 in micro SMD has thermal resistance of 220˚C/W compared to 230˚C/W in MSOP. Even when driving a 600Ω load and operating from ±7.5V supplies, the maximum temperature rise will be under 4.5˚C. For application information specific to micro SMD, see Application note AN-1112.

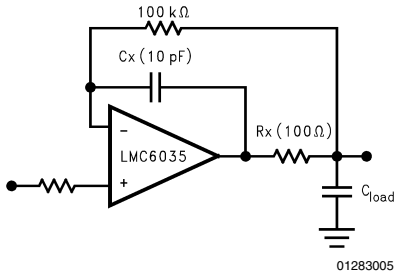



**FIGURE 10. Rx, Cx Improve Capacitive Load Tolerance**

Capacitive load driving capability is enhanced by using a pull up resistor to $V^+$ (*Figure 11*). Typically a pull up resistor conducting 500µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

## 1.0 Application Notes (Continued)

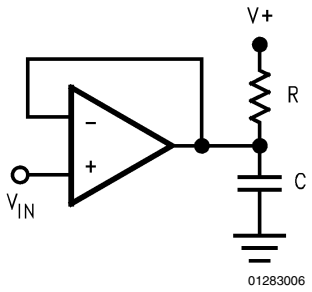
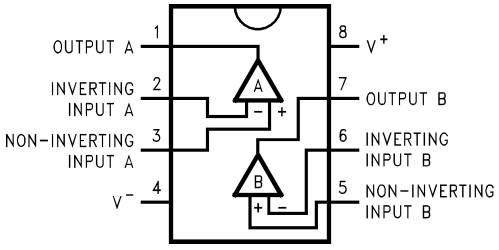



**FIGURE 11. Compensating for Large Capacitive Loads with a Pull Up Resistor**

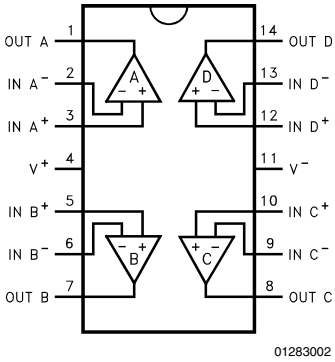
## Connection Diagrams

**8-Pin SO/MSOP**




**Top View**

**14-Pin SO/TSSOP**



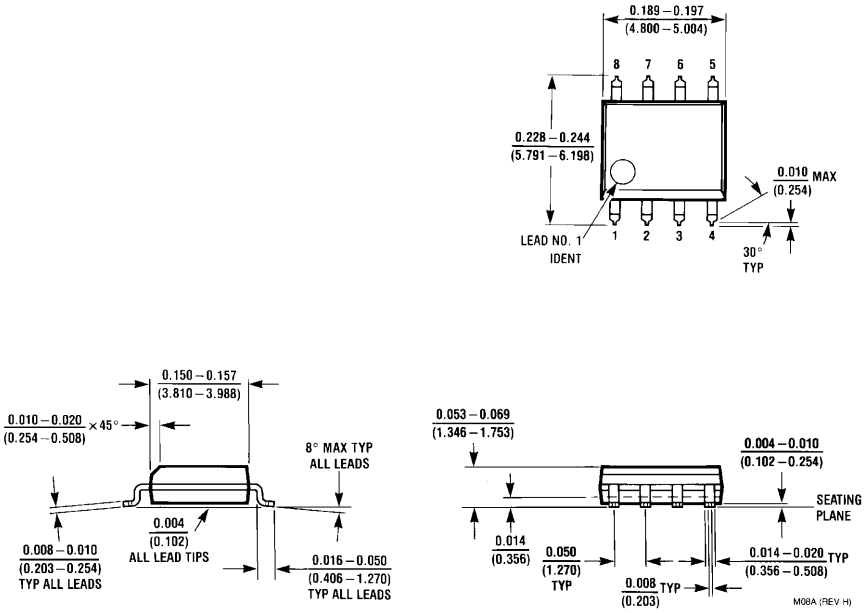

**Top View**

## Ordering Information

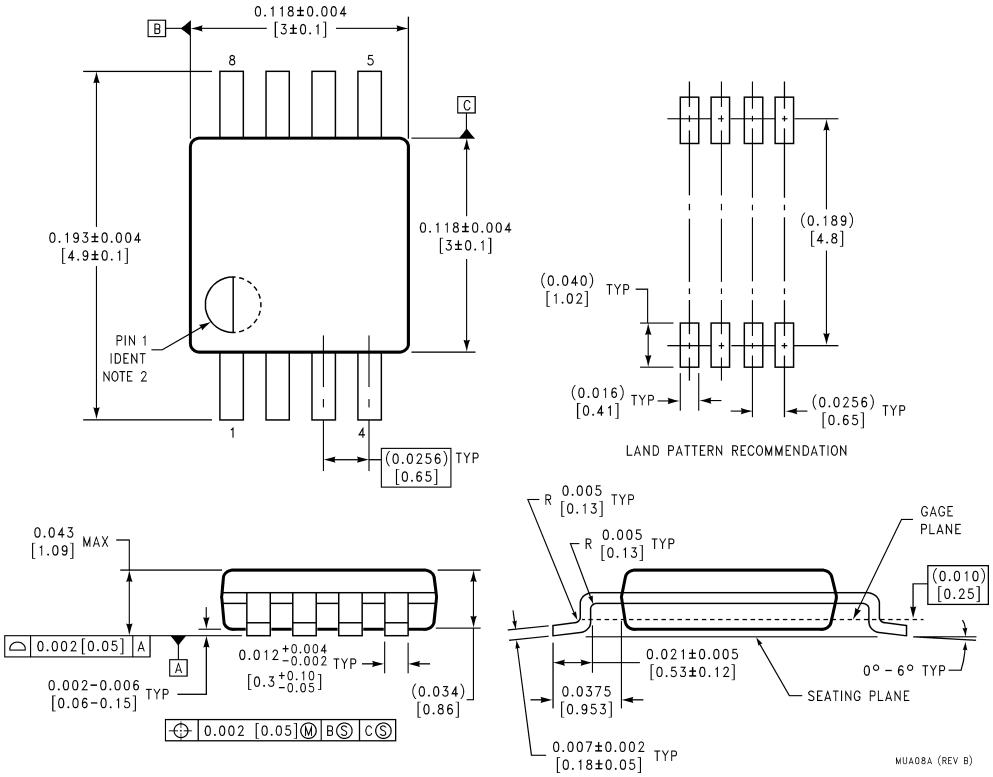
| Package | Temperature Range | Transport Media | NSC Drawing |
|---|---|---|---|
| | **Industrial** **−40˚C to +85˚C** | | |
| 8-pin Small Outline (SO) | LMC6035IM | Rails | M08A |
| | LMC6035IMX | 2.5k Units Tape and Reel | |
| 8-pin Mini Small Outline (MSOP) | LMC6035IMM | 1k Units Tape and Reel | MUA08A |
| | LMC6035IMMX | 3.5k Units Tape and Reel | |
| 14-pin Small Outline (SO) | LMC6036IM | Rails | M14A |
| | LMC6036IMX | 2.5k Units Tape and Reel | |
| 14-pin Thin Shrink Small Outline (TSSOP) | LMC6036IMT | Rails | MTC14 |
| | LMC6036IMTX | 2.5k Units Tape and Reel | |
| 8-Bump micro SMD (Small Bump) | LMC6035IBP | 250 Units Tape and Reel | BPA08FFB |
| | LMC6035IBPX | 3k Units Tape and Reel | |
| 8-Bump Thin micro SMD (Large Bump) | LMC6035ITL | 250 Units Tape and Reel | TLA08JQA |
| | LMC6035ITLX | 3k Units Tape and Reel | |

## Physical Dimensions inches (millimeters)

unless otherwise noted

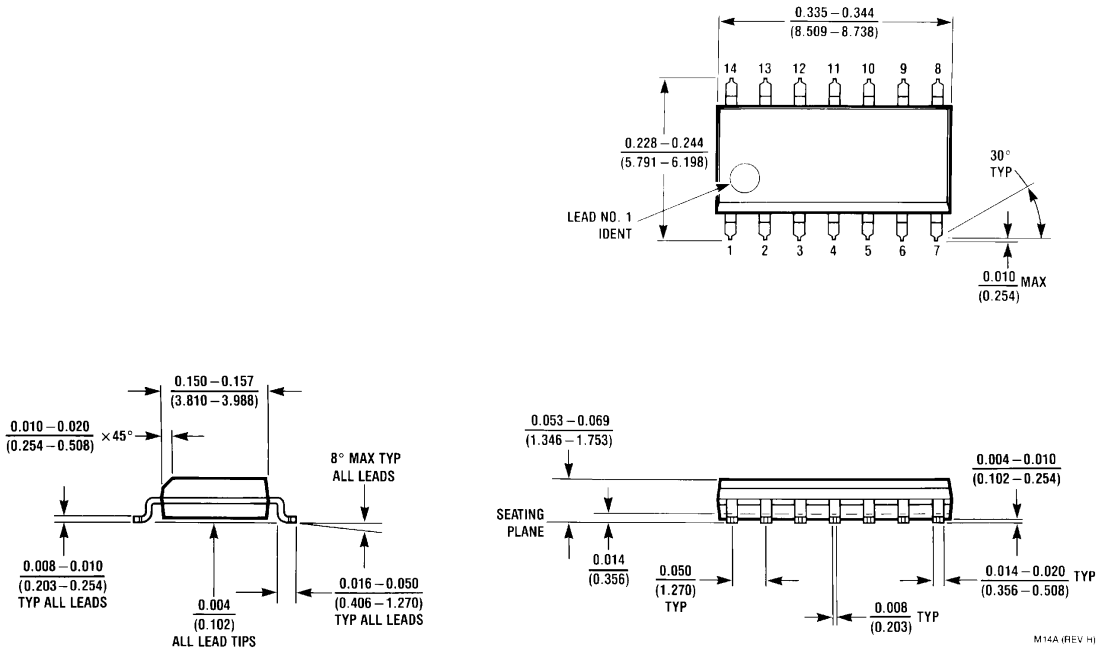



**8-Lead (0.150" Wide) Molded**
**Small Outline Package, JEDEC**
**NS Package Number M08A**

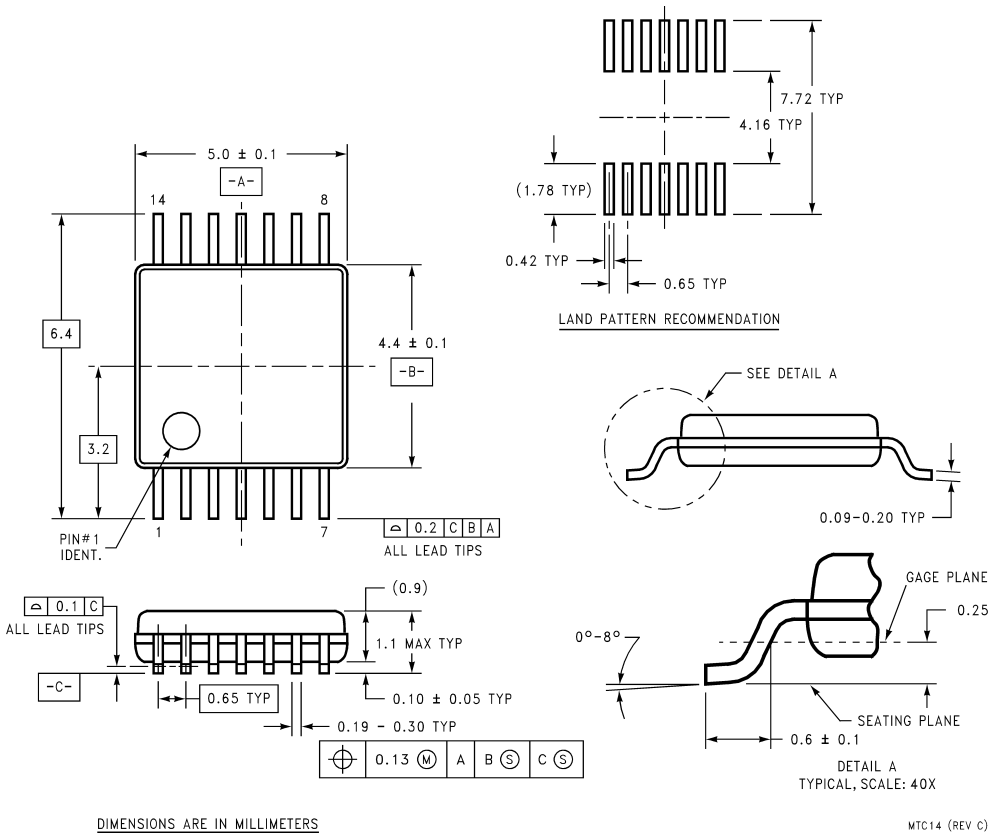



**8-Lead (0.150" Wide) Molded**
**Mini Small Outline Package, JEDEC**
**NS Package Number MUA08A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

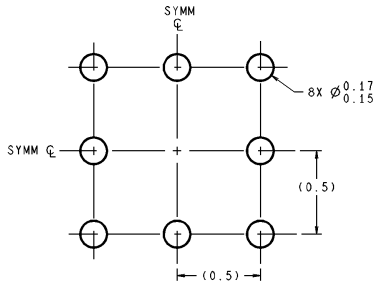



**14-Lead (0.150" Wide) Molded**
**Small Outline Package, JEDEC**
**NS Package Number M14A**



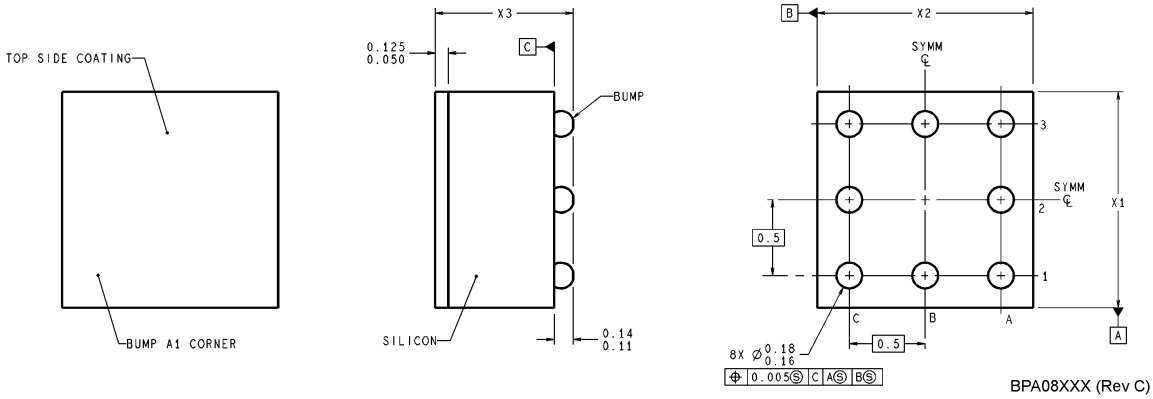

**14-Pin TSSOP**
**NS Package Number MTC14**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION



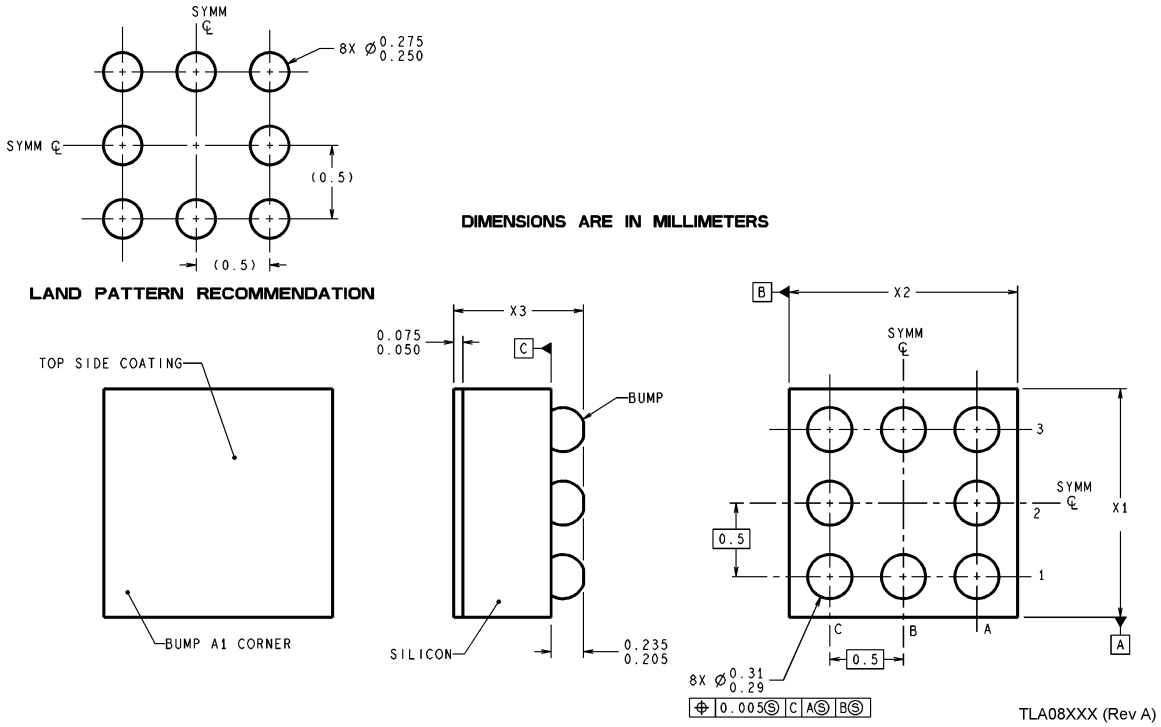

BPA08XXX (Rev C)

NOTE: UNLESS OTHERWISE SPECIFIED.

1. EPOXY COATING.
2. 63Sn/37Pb EUTECTIC BUMP.
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

**8-Bump micro SMD (6 mil bumps)**
**NS Package Number BPA08FFB**
**$X_1$ = 1.412mm $X_2$ = 1.412mm $X_3$ = 0.850mm**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTE: UNLESS OTHERWISE SPECIFIED.

1. EPOXY COATING.
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6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

**8-Bump Thin micro SMD (12 mil bumps)**
**NS Package Number TLA08JQA**
**$X_1$ = 1.717mm $X_2$ = 1.869mm $X_3$ = 0.600mm**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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