AS1710/AS1712

Data Sheet

High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown

1 General Description

The AS1710/AS1712 are low-offset, high-output CMOS op amps that deliver 200mA of peak output current from a single supply (2.7 to 5.5V).

These devices were specifically designed to drive typical headset levels (32Ω), as well as bias RF power amplifiers for wireless handset applications.

The devices are available as the standard products shown in Table 1. See also Ordering Information on page 16.

Table 1. Standard Products

Model	Description	Package
AS1710A	Single Op Amp with Shutdown	SC70-6
AS1710B	Single Op Amp	SC70-5
AS1712A	Quad Op Amp w/Shutdown	TQFN-16 3x3mm

These rail-to-rail I/O, wide-bandwidth amplifiers exhibit a high slew rate of 10V/µs and a gain-bandwidth product of 10MHz.

The integrated shutdown feature (not included in B versions) drives the output low.

These devices operate over the entire automotive temperature range (-40°C to +125°C).

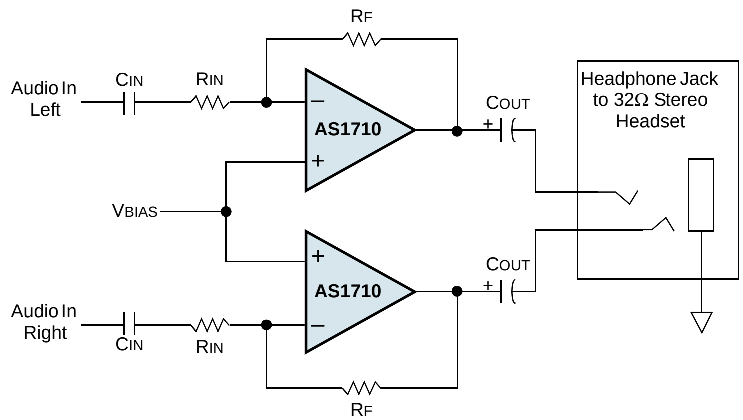
2 Key Features

- Constant Output Drive Capability: 50mA
- Rail-to-Rail Input and Output
- Supply Current: 1.6mA
- Single-Supply Operation: 2.7 to 5.5V
- Gain-Bandwidth Product: 10MHz
- High Slew Rate: 10V/µs
- Voltage Gain: 100dB (R_{LOAD} = 100kΩ)
- Power-Supply Rejection Ratio: -85dB
- No Phase Reversal for Overdriven Inputs
- Unity-Gain Stable for Capacitive Loads: Up to 100pF
- Shutdown Mode (AS1710A) Current: 1nA typ
- Package Types:
  - SC70-6
  - SC70-5
  - TQFN-16 3x3mm

3 Applications

The devices are ideal for portable/battery-powered audio applications, portable headphone speaker drivers (32Ω), hands-free mobile phone kits, TFT panels, sound ports/cards, set-top boxes, biasing controls, DAC converter buffers, transformer/line drivers, motor drivers, and any other battery-operated audio device.

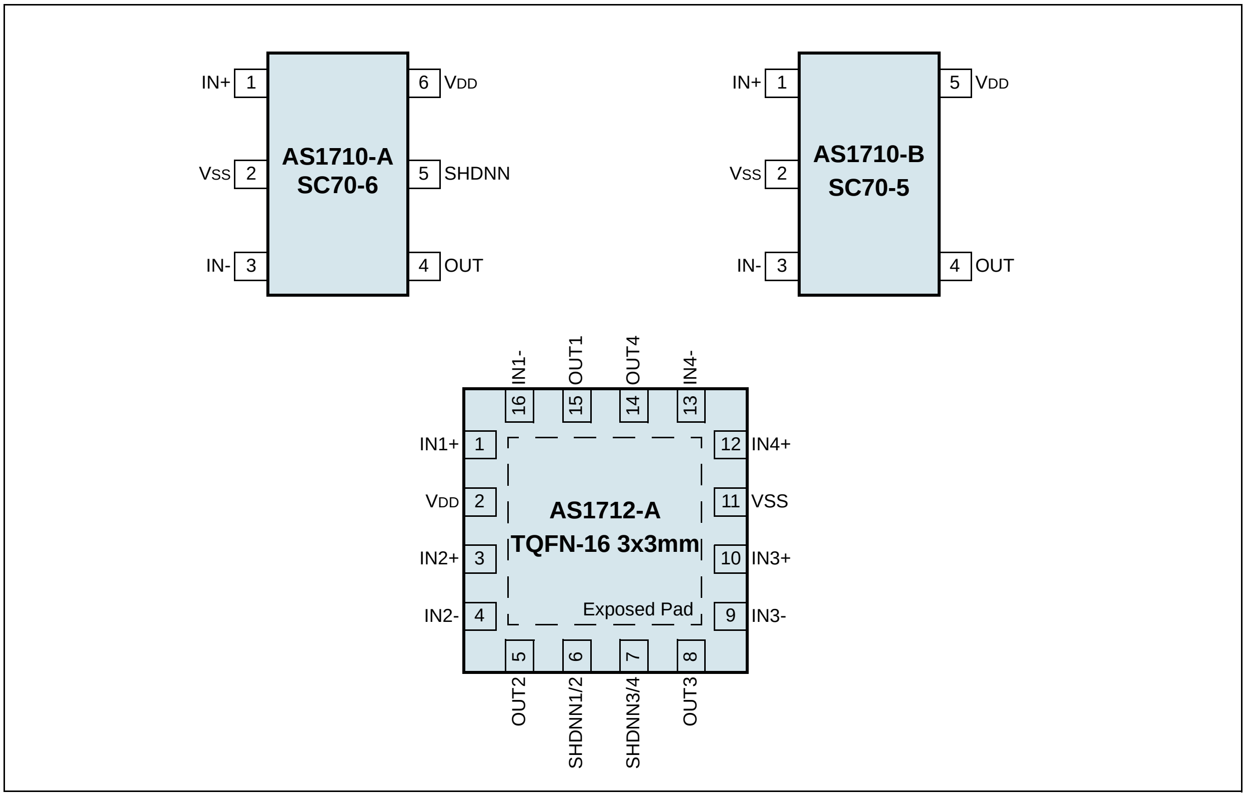
Figure 1. Typical Application



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
See Figure 2	IN+	**Non-inverting Input**
	IN-	**Inverting Input**
	VDD	**Positive Supply Input**
	Vss	**Negative Supply Input.** This pin must be connected to ground in single-supply applications.
	SHDNN	**Active Low Shutdown Control**
	OUT	**Amplifier Output**
	Exposed Pad	**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
Supply Voltage (V_{DD} to V_{SS})			+7	V	
Supply Voltage (All Other Pins)		V_{SS} - 0.3	V_{DD} + 0.3	V	
Output Short-Circuit Duration to V_{DD} or V_{SS}			1	s	
Continuous Power Dissipation	SC70-5		247	mW	Derate at 31mW/ºC above 70ºC
	SC70-6		245		Derate at 31mW/ºC above 70ºC
Thermal Resistance Θ_{JA}	TQFN-16 3x3mm		33	ºC/W	on PCB
Operating Temperature Range		-40	+125	ºC	
Storage Temperature Range		-65	+150	ºC	
Junction Temperature			+150	ºC	
Package Body Temperature			+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

DC Electrical Characteristics

V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = Infinite, V_{SHDNN} = V_{DD}, T_{AMB} = -40 to +125ºC*. Typical values at* T_{AMB} = 25°C*.*

Table 4. DC Electrical Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	Inferred from Power Supply Rejection Ratio Test		2.7		5.5	V
V_{OFFSET}	Input Offset Voltage			-3	0.6	+3	mV
I_{BIAS}	Input Bias Current	V_{CM} = V_{SS} to V_{DD}			50[1]		pA
I_{OFFSET}	Input Offset Current	V_{CM} = V_{SS} to V_{DD}			50[1]		pA
R_{IN}	Input Resistance				1000[1]		MΩ
V_{CM}	Common Mode Input Voltage Range	Inferred from Common Mode Rejection Ratio[1]		V_{SS}		V_{DD}	V
CMRR	Common Mode Rejection Ratio	V_{SS} < V_{CM} < V_{DD}		-45	-70		dB
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.7 to 5.5V		-70	-85		dB
R_{OUT}	Shutdown Output Impedance	V_{SHDNN} = 0V (A-Versions)			130[1]		Ω
$V_{OUT-SHDNN}$	Shutdown Output Voltage	V_{SHDNN} = 0V, R_{LOAD} = 2kΩ to V_{DD} (A-Versions)			170	300	mV
A_{VOL}	Large Signal Voltage Gain	V_{SS} + 0.20V < V_{OUT} < V_{DD} - 0.20V	R_{LOAD} = 100kΩ	85	100		dB
			R_{LOAD} = 2kΩ	79	92		
			R_{LOAD} = 200Ω	69	80		
V_{OUT}	Output Voltage Swing	V_{DD} - V_{OH} or V_{OL} - V_{SS}	R_{LOAD} = 32Ω		350	650	mV
			R_{LOAD} = 200Ω		70	120	
			R_{LOAD} = 2kΩ		9	20	
	Output Voltage	V_{DD} - V_{OH} or V_{OL} - V_{SS}	I_{LOAD} = 10mA, V_{DD} = 2.7V		55	100	mV
			I_{LOAD} = 30mA, V_{DD} = 5V		100	180	
I_{OUT}	Output Source/Sink Current	V_{DD} = 2.7V, V- = V_{CM}, V+ = V_{CM}±100mV			100		mA
		V_{DD} = 5.0V, V- = V_{CM}, V+ = V_{CM}±100mV			200		
I_{DD}	Quiescent Supply Current per OpAmp Output	V_{DD} = 2.7V, V_{CM} = V_{DD}/2			1.6	3.2	mA
		V_{DD} = 5.0V, V_{CM} = V_{DD}/2			2.3	4.6	
$I_{DD-SHDNN}$	Shutdown Supply Current per OpAmp (A-Versions)	V_{SHDNN} = 0V	V_{DD} = 2.7V		1	2000[1]	nA
	SHDNN Logic Threshold (A-Versions)	Shutdown Mode			V_{SS} + 0.3		V
		Normal Operation			V_{DD} - 0.3		
	SHDNN Input Bias Current	V_{SS} < V_{SHDNN} < V_{DD} (A-Versions)			50[1]		pA

1. Guaranteed by design.

AC Electrical Characteristics

V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = Infinite, V_{SHDNN} = V_{DD}, T_{AMB} = -40 to +125ºC*. Typical values at* T_{AMB} = 25°C*.*

Table 5. AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GBWP	Gain-Bandwidth Product	V_{CM} = V_{DD}/2		10		MHz
FPBW	Full-Power Bandwidth	V_{OUT} = 2VP-P, V_{DD} = 5V		2.5		MHz
SR	Slew Rate			10		V/µs
PM	Phase Margin			70		deg
GM	Gain Margin [1]			15		dB
THD+N	Total Harmonic Distortion Plus Noise	f = 10kHz, V_{OUT} = 2V_{P-P}, A_{VCL} = 1V/V		0.05		%
C_{IN}	Input Capacitance			6		pF
en	Voltage-Noise Density[1]	f = 1kHz		15		nV/√Hz
		f = 10kHz		10		
	Capacitive-Load Stability	A_{VCL} = 1V/V, no sustained oscillations		100		pF
t_{SHDN}	Shutdown Time (AS1710A)			1		µs
t_{ENABLE}	Enable Time from Shutdown (AS1710A)			7		µs
t_{ON}	Power-Up Time			20		ns

1. Guaranteed by design.

7 Typical Operating Characteristics

V_{DD} = 2.7V; V_{SS} = 0V, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, R_{LOAD} = ∞, V_{SHDNN} = V_{DD} T_{AMB} = +25ºC (unless otherwise specified).

Figure 3. Gain and Phase vs. Frequency

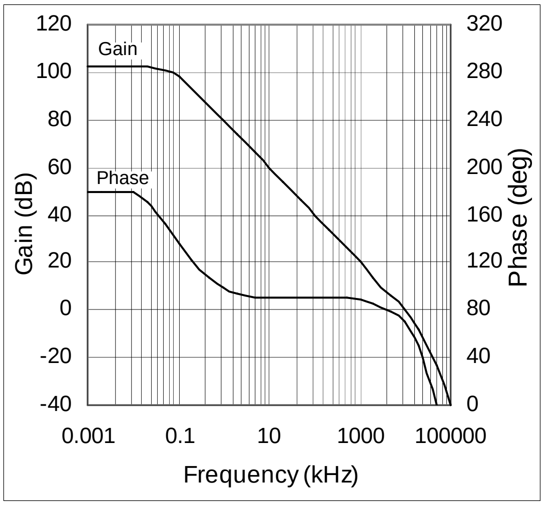


Figure 4. Gain and Phase vs. Frequency, C_{LOAD} = 100pF

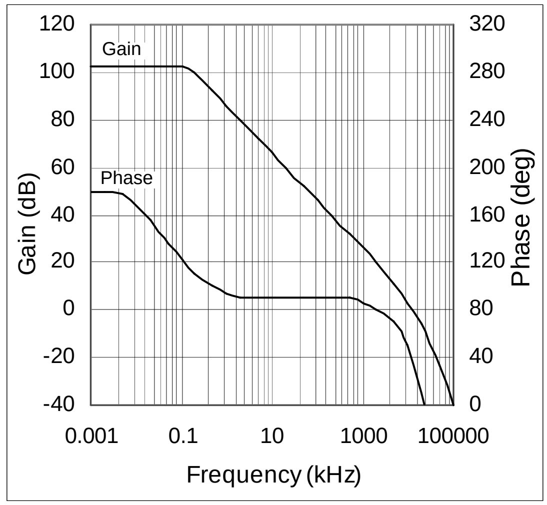


Figure 5. PSRR vs. Frequency

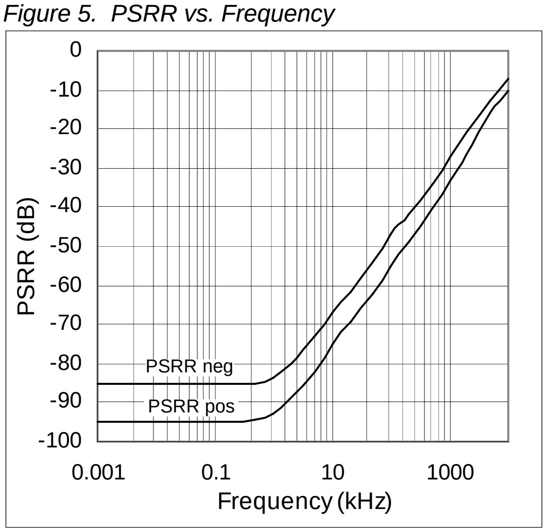


Figure 6. CMRR vs. Frequency

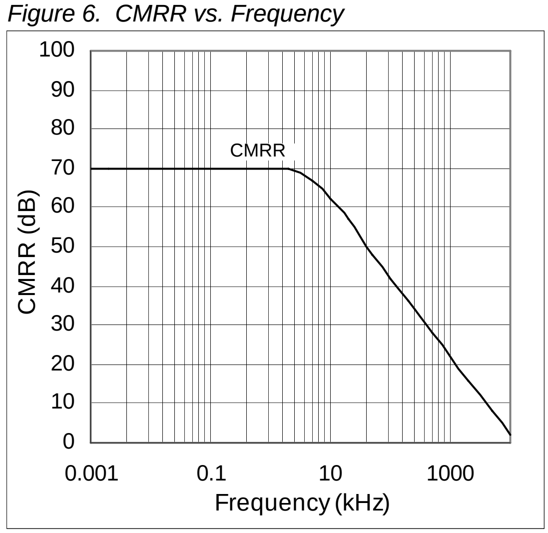


Figure 7. Supply Current vs. Temperature

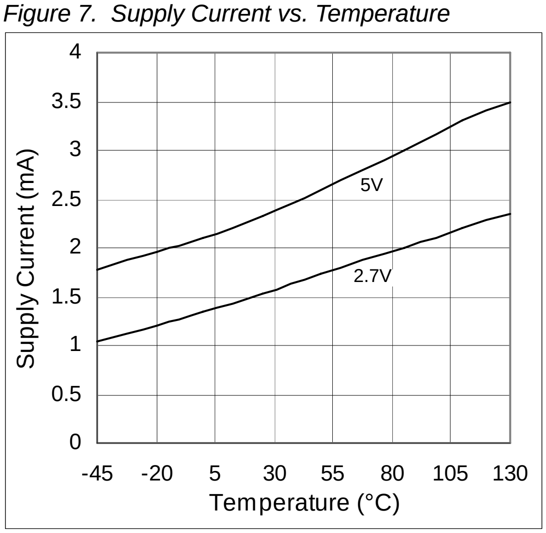


Figure 8. Shutdown Current vs. Temperature

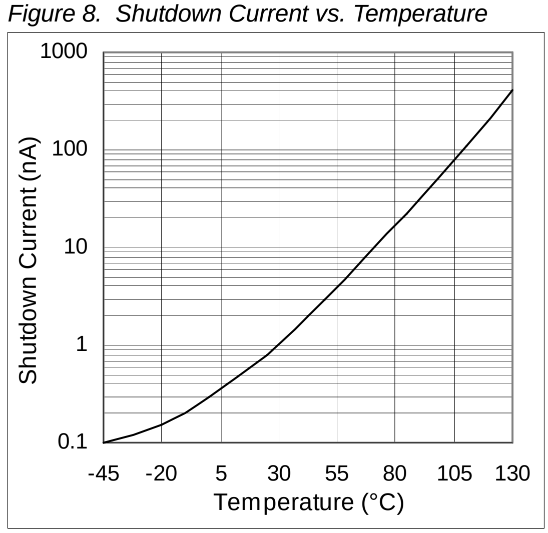


Figure 9. Supply Current vs. Common-Mode Voltage

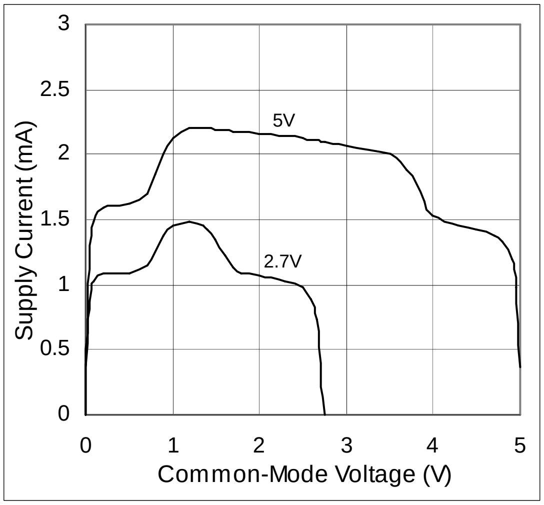


Figure 10. Input Voltage Noise vs. Frequency

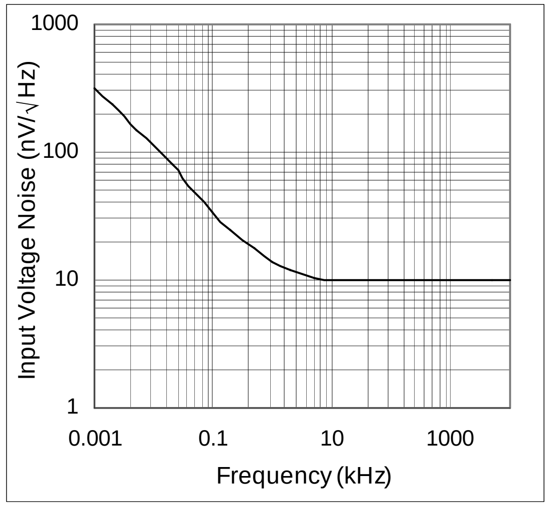


Figure 11. Output Voltage vs. Output Current, sourcing

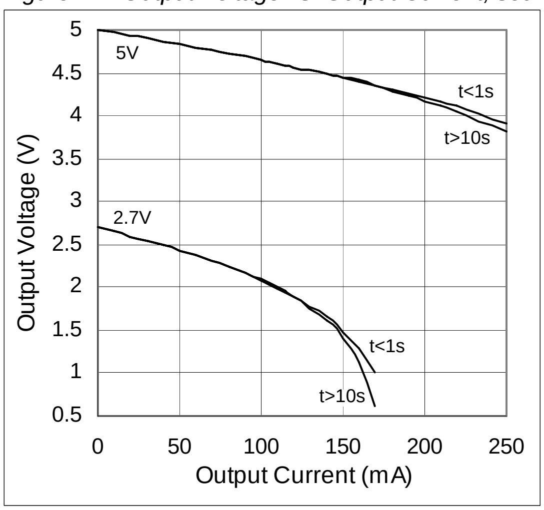


Figure 12. Output Voltage vs. Output Current, sinking

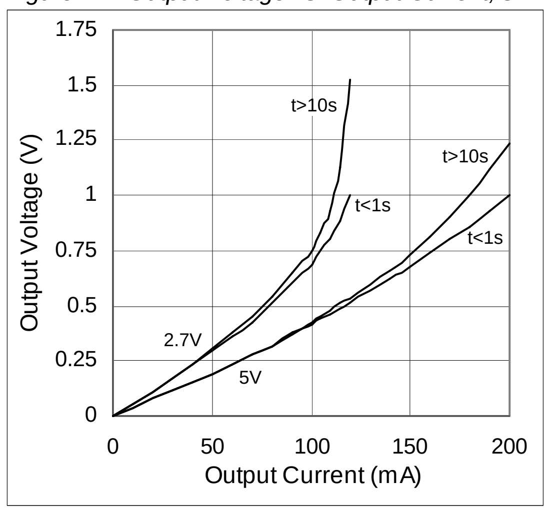


Figure 13. Output Swing High vs. Temperature

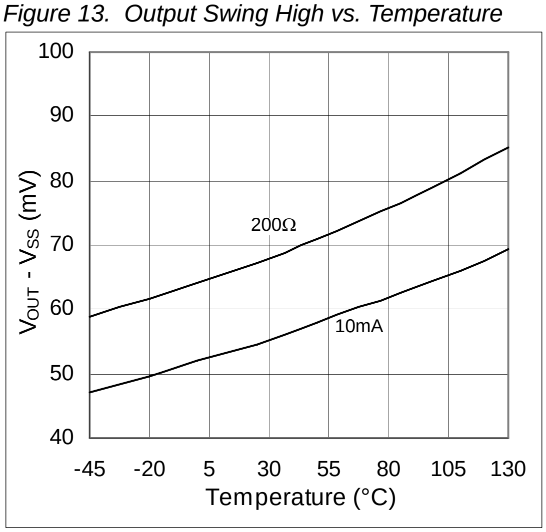


Figure 14. Output Swing Low vs. Temperature

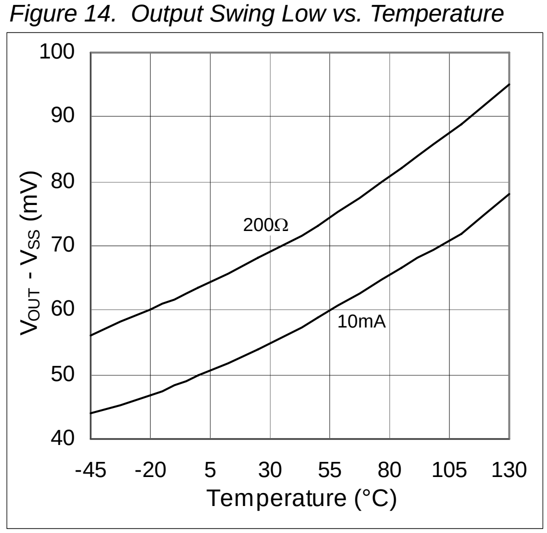


Figure 15. Transient Response, 100mV, 10pF load

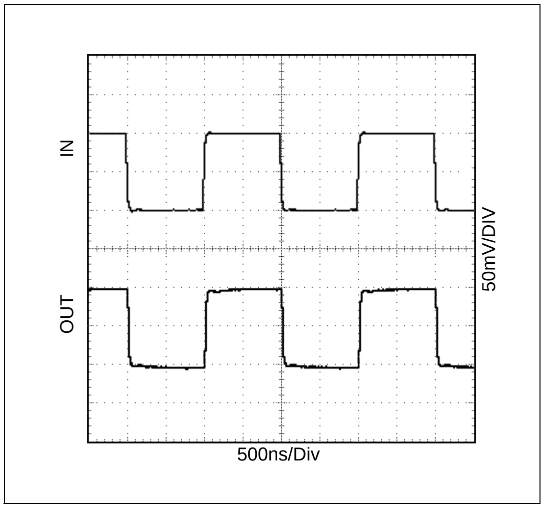


Figure 16. Transient Response, 100mV, 100pF load

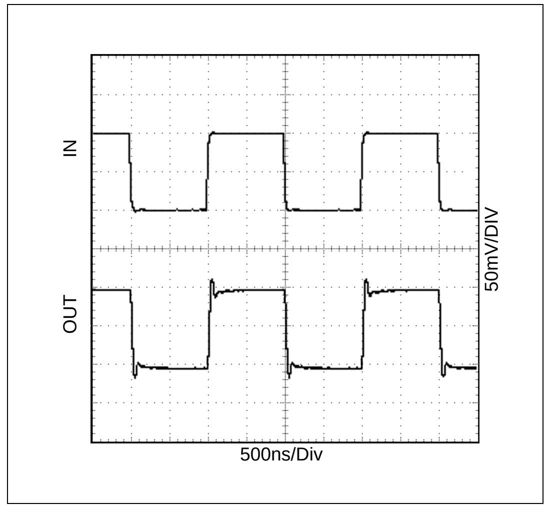


Figure 17. Transient Response, 1V, 10pF load

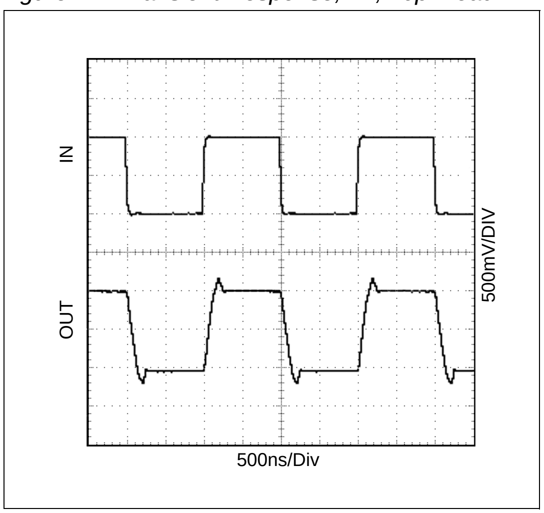


Figure 18. Transient Response, 1V, 100pF load

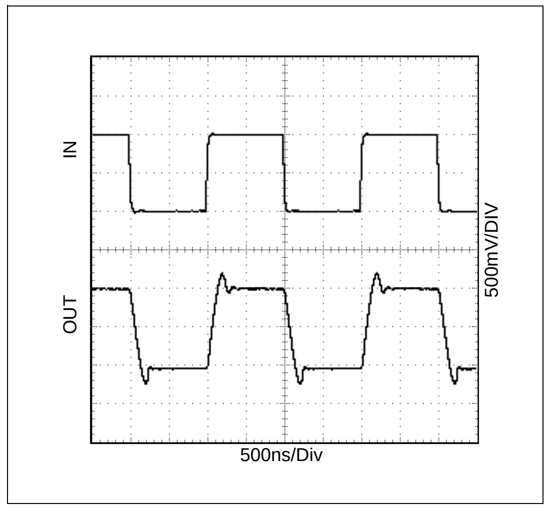


Figure 19. Transient Response, 2V, 10pF load

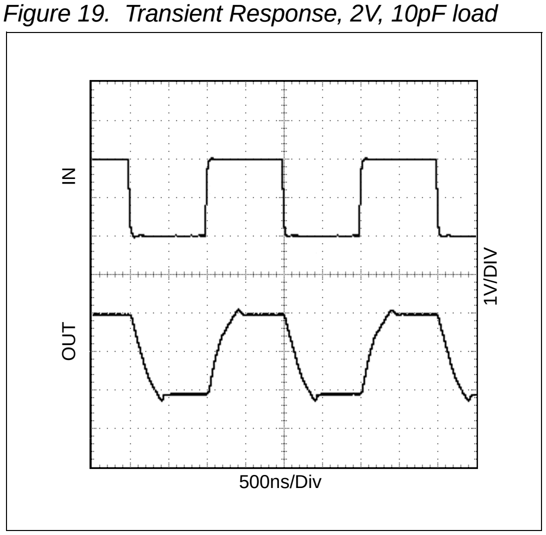
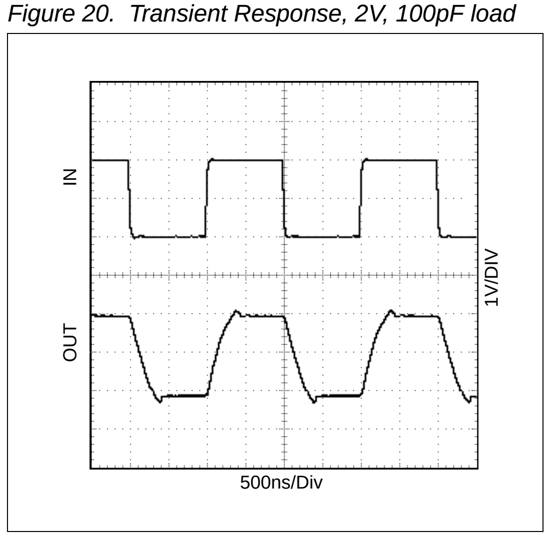


Figure 20. Transient Response, 2V, 100pF load



8 Application Information

Package Power Dissipation

Caution: Due to the high output current drive, this op amp can exceed the absolute maximum power-dissipation rating. Normally, when peak current is less than or equal to 40mA the maximum package power dissipation is not exceeded for any of the package types offered.

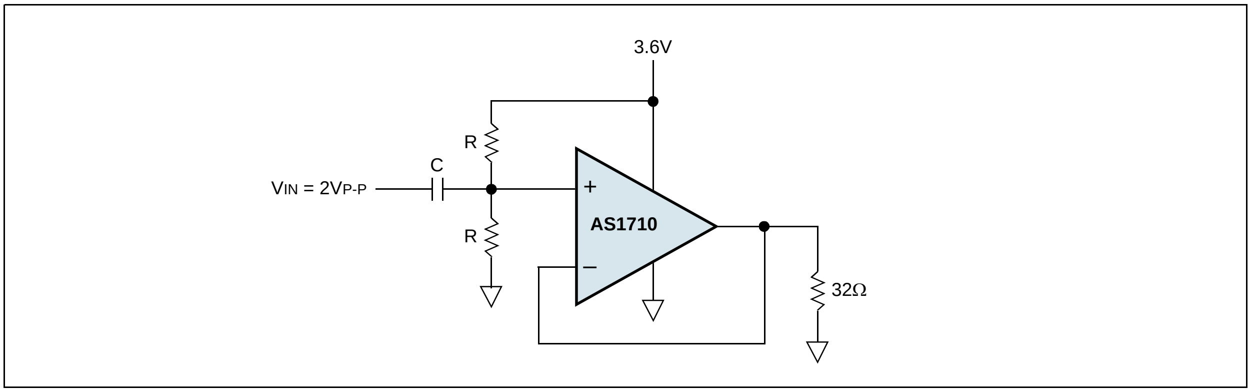
The absolute maximum power-dissipation rating of each package should always be verified. (EQ 1) gives an approximation of the package power dissipation:

$$P_{PACKAGEDISS} \cong V_{RMS} I_{RMS} COS\theta \quad \text{(EQ 1)}$$

Where:

V_{RMS} is the RMS voltage from V_{DD} to V_{OUT} when sourcing current, and from V_{OUT} to V_{SS} when sinking current.
I_{RMS} is the RMS current flowing in or out of the op amp and the load.
θ is the phase difference between the voltage and the current. For resistive loads, $COS\theta = 1$.

Figure 21. Typical AS1710/AS1712 Single-Supply Application



V_{RMS} can be calculated as:

$$V_{RMS} \cong (V_{DD} - V_{DC}) + V_{PEAK} / \sqrt{2} \quad \text{(EQ 2)}$$

Where:

V_{DC} is the DC component of the output voltage.
V_{PEAK} is the highest positive excursion of the AC component of the output voltage.

For the circuit shown in Figure 21:

$$V_{RMS} = (3.6V - 1.8V) + 1.0V/\sqrt{2} = 2.507V_{RMS}$$

I_{RMS} can be calculated as:

$$I_{RMS} \cong I_{DC} + (I_{PEAK}/\sqrt{2}) \quad \text{(EQ 3)}$$

Where:

I_{DC} is the DC component of the output current.
I_{PEAK} is the highest positive excursion of the AC component of the output current.

For the circuit shown in Figure 21:

$$I_{RMS} = (1.8V/32\Omega) + (1.0V/32\Omega)/\sqrt{2} = 78.4mA_{RMS}$$

Therefore, for the circuit in Figure 21 the package power dissipation can be calculated as:

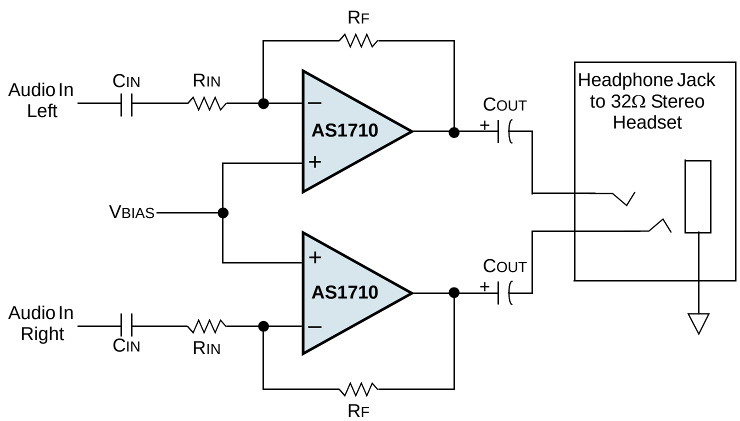
$$P_{PACKAGEDISS} = V_{RMS} I_{RMS} COS\theta = 196mW$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 22 on page 10.

60mW Single-Supply Stereo Headphone Driver

Two AS1710 amplifiers can be used as a single-supply, stereo headphone driver. The circuit shown in Figure 22 can deliver 60mW per channel with 1% distortion from a single 5V supply.

Figure 22. Stereo Headphone Driver Application (with Coupling Capacitor)



In Figure 22, C_{IN} and R_{IN} form a high-pass filter that removes the DC bias from the incoming signal. The -3dB point of the high-pass filter is given by:

$$f_{-3dB} = 1/(2\pi R_{IN} C_{IN}) \quad \text{(EQ 4)}$$

Choose gain-setting resistors R_{IN} and R_F according to the amount of desired gain, keeping in mind the maximum output amplitude.

C_{OUT} blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a high-pass filter with the -3dB point determined by:

$$f_{-3dB} = 1/(2\pi R_{LOAD} C_{OUT}) \quad \text{(EQ 5)}$$

For a 32Ω load, a 100µF aluminum electrolytic capacitor gives a low-frequency pole at 50Hz.

Rail-to-Rail Input Stage

The AS1710/AS1712 CMOS op amps have parallel connected N- and P-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The N-channel stage is active for common-mode input voltages typically greater than (V_{SS} + 1.2V), and the p-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.2V).

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single- supply operation, where the load is referenced to ground (V_{SS}). Figure 23 shows the input voltage range and the output voltage swing of an AS1710 connected as a voltage follower. The maximum output voltage swing is load dependent although it is guaranteed to be within 500mV of the positive rail (V_{DD} = 2.7V) even with maximum load (32Ω to ground).

Figure 23. Rail-to-Rail Input/Output Range, 100kΩ

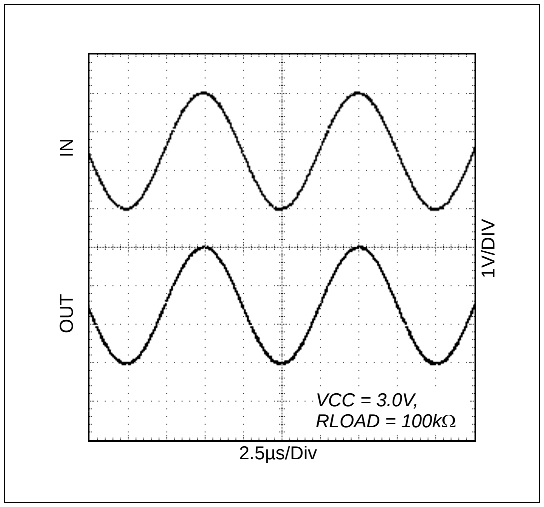
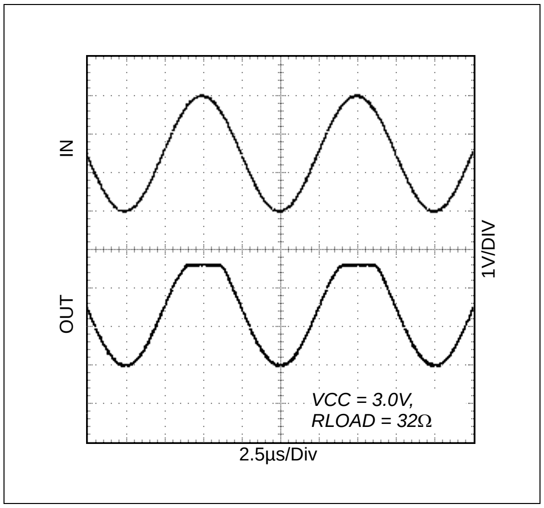


Figure 24. Rail-to-Rail Input/Output Range, 32Ω

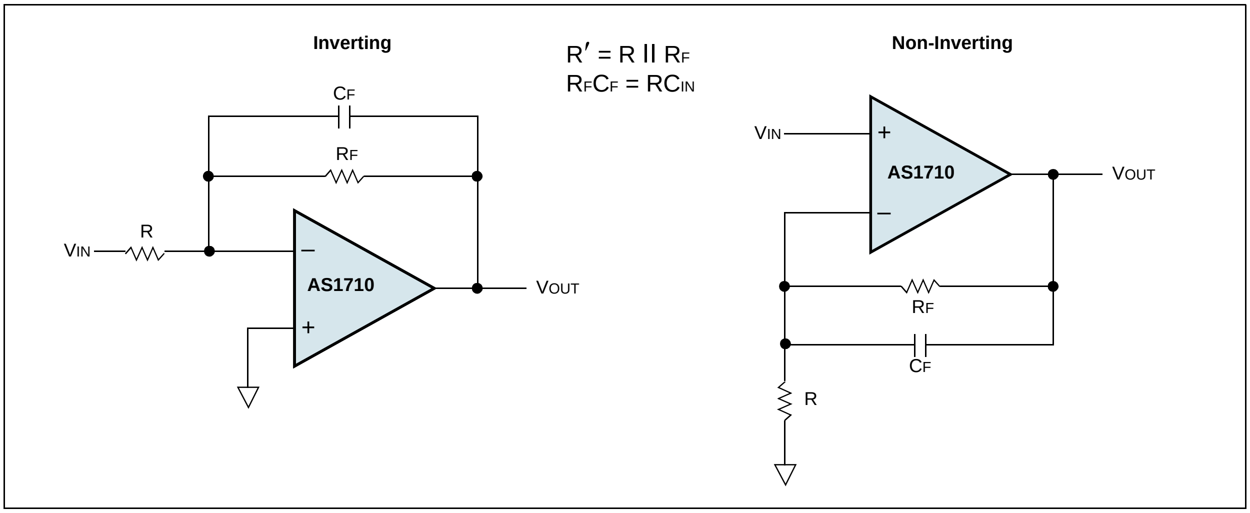


Note: The absolute maximum ratings (see page 3) for power dissipation and output short-circuit duration (10s, max) must be adhered to since the output current can exceed 200mA (see Typical Operating Characteristics on page 6).

Input Capacitance

The parallel-connected differential input stages for rail-to-rail operation results in relatively large input capacitance C_{IN} (6pF typ). This introduces a pole at frequency $(2\pi R' C_{IN})$-1, where R′ is the parallel combination of the gain-setting resistors for the inverting or non-inverting amplifier configuration (Figure 25). If the pole frequency is less than or comparable to the unity-gain bandwidth (10MHz), the phase margin is reduced, and the amplifier exhibits degraded AC performance through either ringing in the step response or sustained oscillations.

Figure 25. Inverting and Non-inverting Amplifiers with Feedback Compensation



The pole frequency is 10MHz when R′ = 2kΩ. To maximize stability, R′ << 2kΩ is recommended.

To improve step response when R′ > 2kΩ, connect a small capacitor (C_F) between the inverting input and output. C_F can be calculated by:

$$C_F = 6(R/R_F)\ [pf] \qquad \text{(EQ 6)}$$

Where:

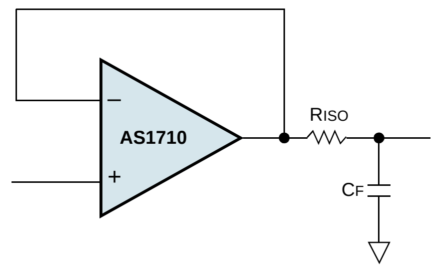
R_F is the feedback resistor.
R is the gain-setting resistor.

Driving Capacitive Loads

The AS1710/AS1712 amplifiers have a high tolerance for capacitive loads, and are stable with capacitive loads up to 100pF.

Figure 26 shows a typical non-inverting capacitive-load driving circuit in the unity-gain configuration.

Figure 26. Capacitive-Load Driving Circuit



Note: Resistor R_{ISO} improves the circuit's phase margin by isolating the load capacitor from the AS1710/AS1712 output.

Power-Up

The AS1710/AS1712 typically settle within 5µs after power-up.

Shutdown

When SHDNN (not included in B versions) is pulled low, supply current drops to 0.5µA (per amplifier, V_{DD} = 2.7V), the amplifiers are disabled, and their outputs are driven to V_{SS}. Because the outputs are actively driven to V_{SS} in shutdown, any pullup resistor on the output causes a current drain from the supply.

Note: Pulling SHDNN high enables the amplifier. In the AS1712 the amplifiers shutdown in pairs.

When exiting shutdown, there is a 6µs delay before the amplifier output becomes active.

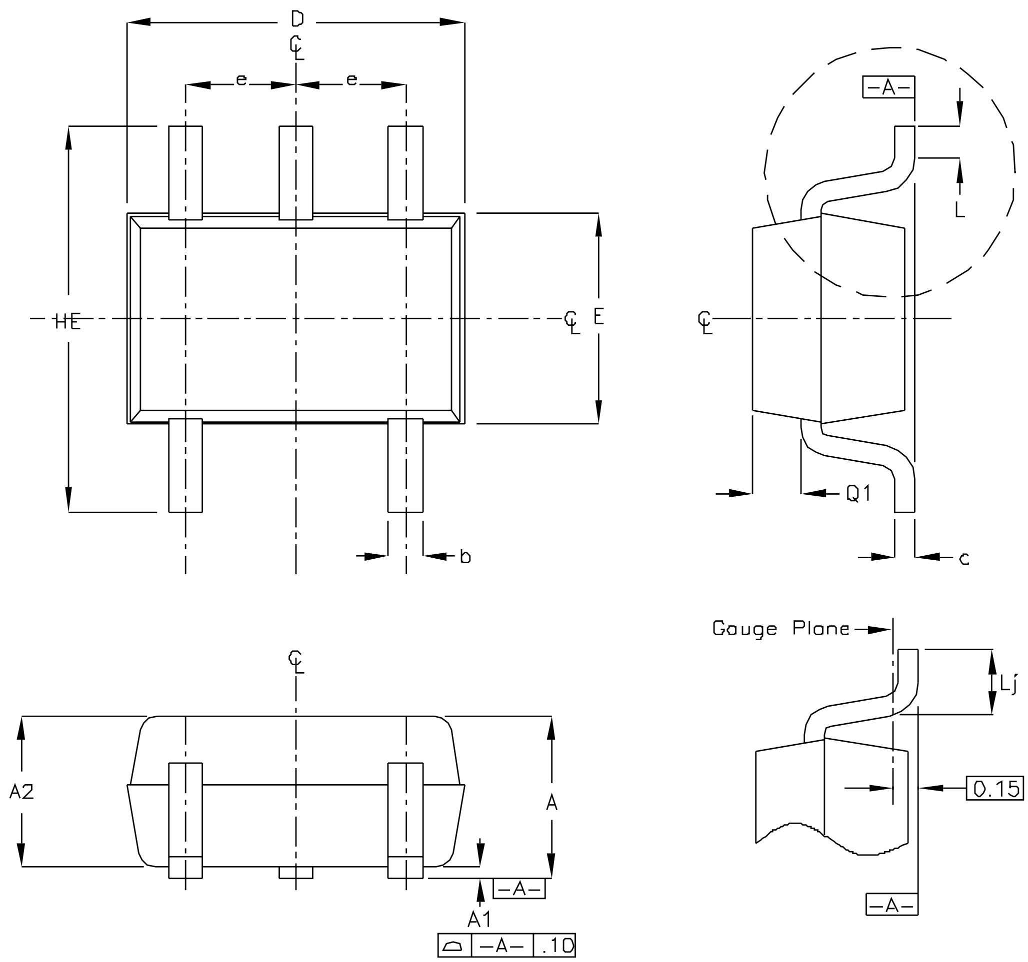
Power Supplies and Layout

The AS1710/AS1712 can operate from a single 2.7 to 5.5V supply or from dual ±1.35 to ±2.5V supplies. Good design improves device performance by decreasing the amount of stray capacitance at the op amp inputs/outputs.

- For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor.
- For dual-supply operation, bypass each supply to ground.
- Decrease stray capacitance by placing external components close to the op amp pins, minimizing trace and lead lengths.

9 Package Drawings and Markings

Figure 27. SC70-5 Package

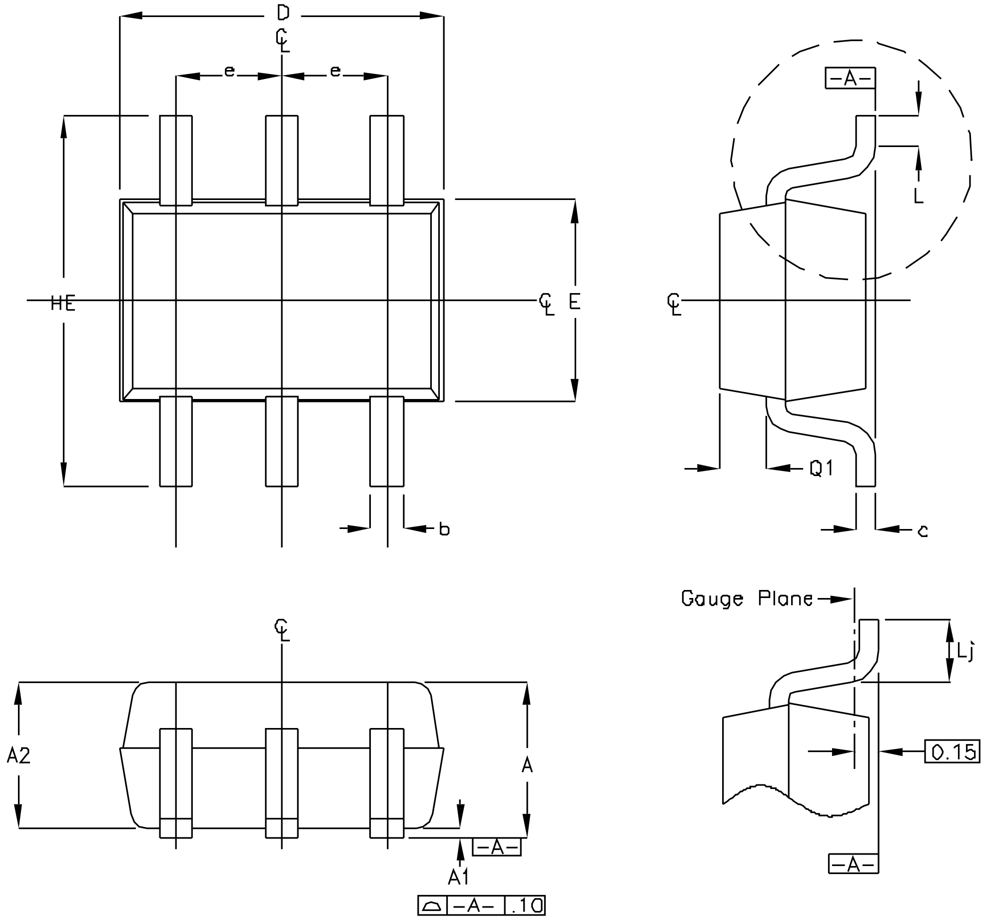


Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash and metal burr.
4. All specifications comply with *JEITA SC88A* and *JEDEC MO203*.

Symbol	Min	Max
e	0.65BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
Lj	0.26	0.46

Figure 28. SC70-6 Package

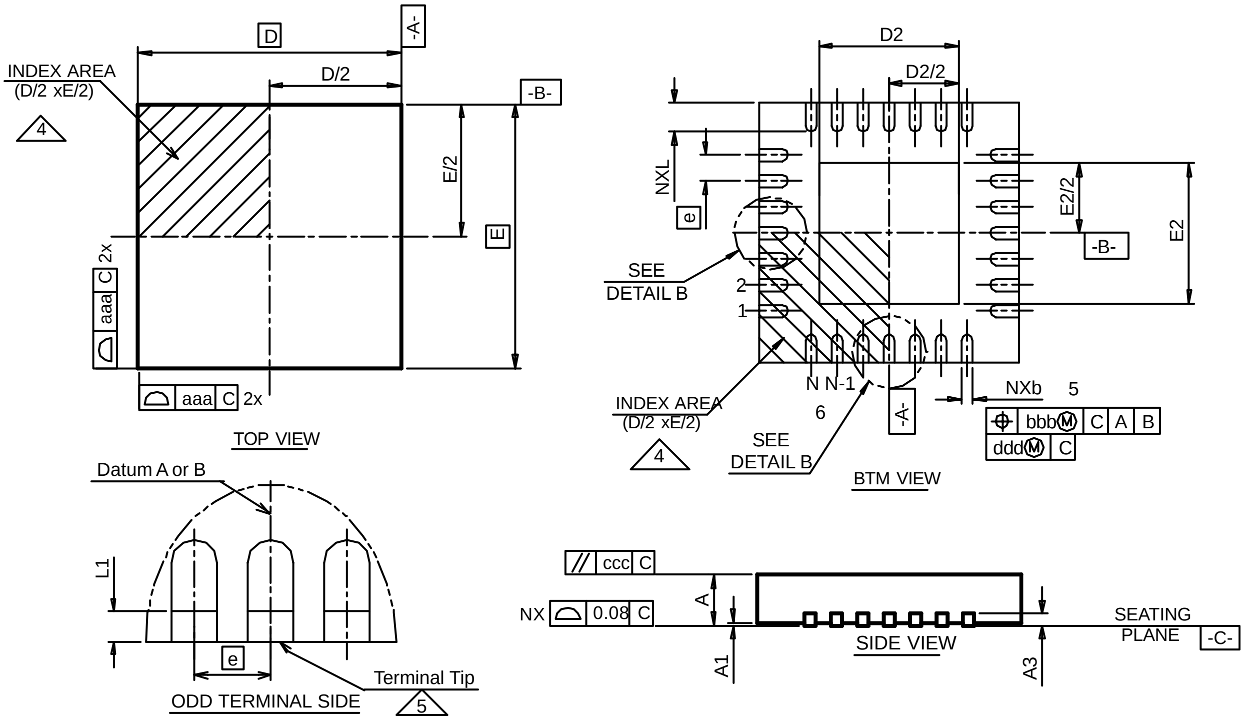


Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Dimensions are exclusive of mold flash and metal burr.
4. All specifications comply with *JEITA SC88* and *JEDEC MO203.*

Symbol	Min	Max
e	0.65BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
Lj	0.26	0.46

Figure 29. TQFN-16 3x3mm Package



Symbol	Min	Typ	Max	Notes
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
b	0.18	0.25	0.30	1, 2
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		0.20REF		1, 2
e			0.50	

Symbol	Min	Typ	Max	Notes
L1	0.03		0.15	1, 2
D BSC		3.00		1, 2, 8
E BSC		3.00		1, 2, 8
D2	1.30	1.45	1.55	1, 2, 8
E2	1.30	1.45	1.55	1, 2, 8
L	0.30	0.40	0.50	1, 2, 8
N		16		1, 2, 8
ND		4		1, 2, 8
NE		4		

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5m-1994*.
2. All dimensions are in millimeters while angle is in degrees (°).
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95, SPP-002*. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
6. Depopulation is possible in a symmetrical fashion.
7. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
8. ND and NE refer to the number of terminals on sides D and E respectively.

10 Ordering Information

The device is available as the standard products shown in Table 6.

Table 6. Ordering Information

Model	Description	Delivery Form	Package
AS1710A-ASCT	Single Op Amp with Shutdown	Tape and Reel	SC70-6
AS1710B-ASCT	Single Op Amp	Tape and Reel	SC70-5
AS1712A-AQFT	Quad Op Amp with Shutdown	Tape and Reel	TQFN-16 3x3mm

All devices are RoHS compliant and free of halogene substances.

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