# Mixed Signal Digital Predistortion Evaluation Platform

# AD-MSDPD-EVB

## FEATURES

**High performance RF and mixed signal transmit and observation signal chains seamlessly integrated on one board**
**Full implementation of 16-bit I/Q data to 18 dBm RF output with 12 dB of fine analog gain control and 122.88 MHz of complex bandwidth**
**Observation receiver from RF to bits, 12 bits, 250 MSPS**
**SERDES clock clean-up, up to 307.2 MHz**
**Full clock synthesis including SERDES Tx clock synthesis**
**Full LO synthesis for ZIF or CIF Tx as well as IF sampling receive**
**Optional on-board reference clock for standalone operation**
**USB interface with intuitive user interface**
**Interfaces for both the Altera HSMC and the Xilinx FMC mezzanine connectors**

## APPLICATIONS

**Transmitter development for TDD and FDD applications MC-GSM, W-CDMA, CDMA2000, TD-SCDMA, and LTE**

## AD-MSDPD-EVB SYSTEM BOARD

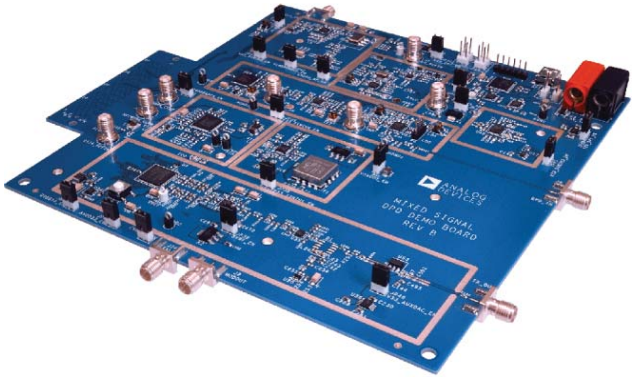


*Figure 1.*

## GENERAL DESCRIPTION

The AD-MSDPD-EVB system board provides a turnkey evaluation platform for the development of the linear and mixed signal content for high performance transmit data. The MSDPD board takes baseband I and Q data and generates an RF output signal up to 18 dBm, which can be passed to an external power amplifier (PA) for transmit. Spectral purity is targeted up to MC-GSM Class 1 levels of performance when coupled with a suitable digital predistortion algorithm.

A full observation path is also included that accepts the sampled RF output up to 16 dBm and mixes it down to a suitable IF frequency that is digitized with a 12-bit, 250 MSPS analog-to-digital converter (ADC).

The board can accept a SERDES network recovered clock of both n times 30.72 MHz and n times 38.4 MHz up to 307.2 MHz. If no external reference is available, an on-board 30.72 MHz reference can be used. Regardless of which reference is used, the board provides dual-loop PLL clean-up, and clock synthesis of ADC, DAC, FPGA, and network transmit clocks.

The board also synthesizes local oscillators for both zero IF and complex IF transmit, as well as the local oscillator for the IF sampling observation path.

Control of the board is via a USB port using an intuitive user interface or by direct access from the FPGA interface when needed. Power is 5.3 V up to 3 A, depending on the exact configuration. An internationally compliant 6 V, 3 A switching power supply and a power supply unit (PSU) adapter board are shipped with the AD-MSDPD-EVB board. The PSU adapter board interfaces the 6 V wall plug to the 5.3 V banana jack input required by the AD-MSDPD-EVB board.

The AD-MSDPD-EVB highlights usage of the following leading technology products: AD9122, ADL5375, ADL5541, ADL5320/ADL5321, AD9230, AD8375, AD5611, ADL5365/ADL5367, AD9516, ADF4002 (2), ADF4350, ADCLK925, and ADCLK905.

Numerous other parts are showcased including regulators and control loop products.

**Rev. 0**


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## REVISION HISTORY

**11/10—Revision 0: Initial Version**

# AD-MSDPD-EVB BLOCK DIAGRAM

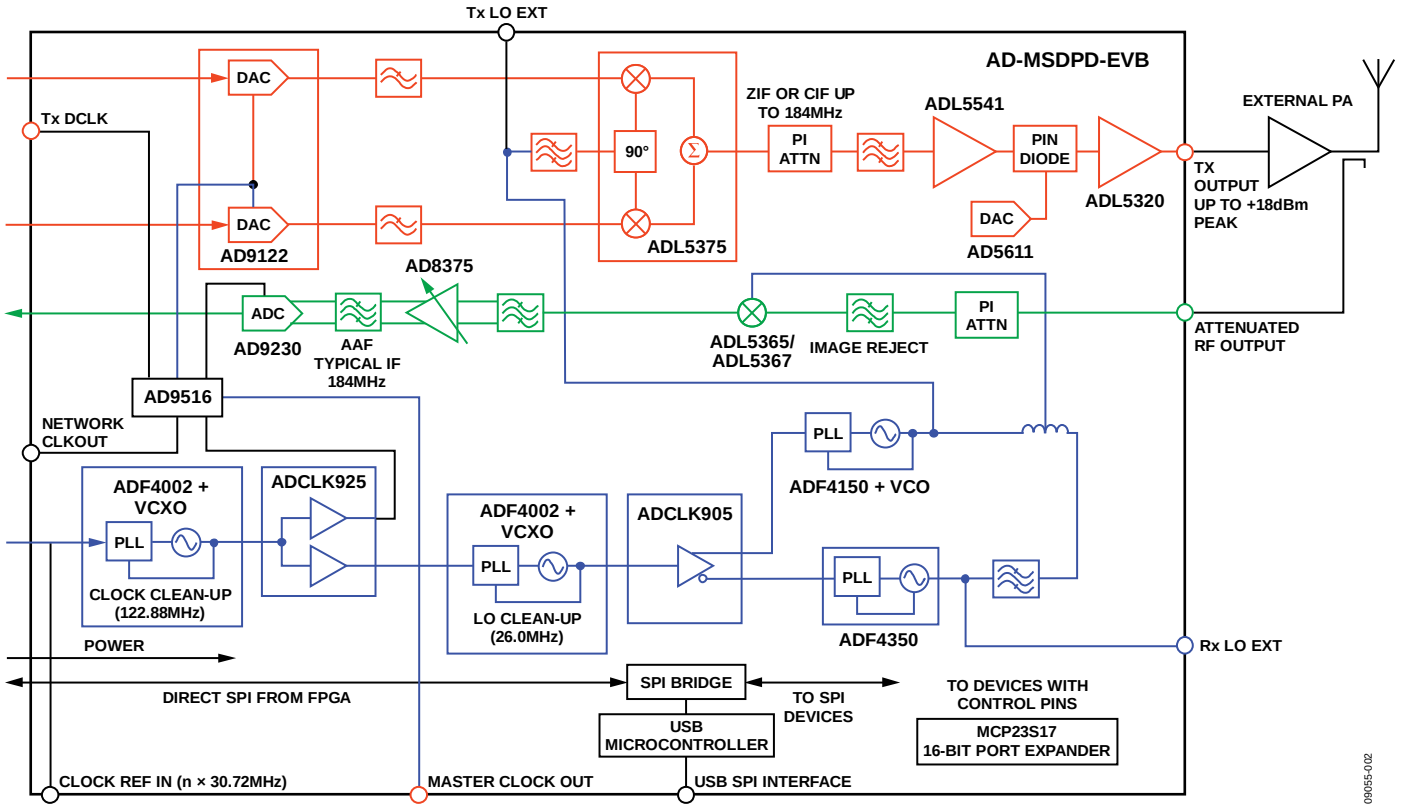



*Figure 2. MSDPD Block Diagram*

**Table 1. Connector Descriptions**

| Designation | Description |
|---|---|
| J1 | Auxiliary LO reference input |
| J2 | Auxiliary modulator RF output |
| J3 | Auxiliary Rx LO input or auxiliary PLL output |
| J4 | Auxiliary ADC input |
| J5 | Master reference clock input |
| J6 | Observation input |
| J7 | Network clock Out P (positive output) |
| J8 | Network clock Out N (negative output) |
| J26 | Auxiliary Tx LO input |
| TX_OUT | Main Tx output connector |
| DPD_IF | Auxiliary Rx IF output |
| 9516_REFIN | Auxiliary clock reference input |
| P1 | Xilinx FMC connector or Altera HSMC connector |
| P3 | 5.3 V supply input |
| P4 | Power ground |
| XP1 | Microcontroller program header |
| XP2 | Mini USB connector |

# SPECIFICATIONS

VCC = 5.3 V, master reference clock in = 30.72 MHz, 0 dBm, $RF_{OUT}$ = 2.14 GHz, $P_{OUT}$ = 5 dBm, $Z_{OUT}$ = 50 Ω, temperature = 25°C, unless otherwise noted.

## POWER SPECIFICATIONS

**Table 2.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| POWER SUPPLIES | | | | |
| Supply Voltage | | | | |
| VCC | | 5.3 | | V |
| Supply Current | | | | |
| IVCC | 1.6 | | 2.9 | A |
| POWER CONSUMPTION | | | | |
| Operating Power | 8.48 | | 15.37 | W |

## TRANSMIT SPECIFICATIONS

**Table 3.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| OVERALL FUNCTION | | | | |
| Output Frequency Range[1] | 700 | | 2700 | MHz |
| $Z_{OUT}$ | | 50 | | Ω |
| Resolution (Complex) | | 16 | | Bits |
| DAC Sample Rate[2] | | 983.04 | | MSPS |
| DAC IF Output Frequency[3] | −200 | | +200 | MHz |
| Baseband Bandwidth | | 122.88 | | MHz |
| Frequency Range[4] | −50 | | +50 | MHz |
| OUTPUT FREQUENCY = 2140 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 18.5 | | dBm |
| Analog Gain Adjustment | | 12.5 | | dB |
| Pass-Band Flatness | | ±0.6 | | dB |
| Output Noise Floor (1-Tone, $P_{OUT}$ = 5 dBm) | | −142 | | dBm/Hz |
| Output IMD (2-Tone, 1 MHz Spacing, −3 dBFS, $P_{OUT}$ = 9.8 dBm/Tone) | | −66.5 | | dBc |
| Output 1 dB Compression Point | | 24 | | dBm |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −2.2 dBm) | | −70.5 | | dBc |
| OUTPUT FREQUENCY = 900 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 23 | | dBm |
| Analog Gain Adjustment | | 15.5 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −1.1 dBm) | | −71 | | dBc |
| OUTPUT FREQUENCY = 1850 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 20.5 | | dBm |
| Analog Gain Adjustment | | 13.5 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −2.1 dBm) | | −70 | | dBc |
| OUTPUT FREQUENCY = 2000 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 18.5 | | dBm |
| Analog Gain Adjustment | | 12.5 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −2.4 dBm) | | −70 | | dBc |
| OUTPUT FREQUENCY = 2350 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 18 | | dBm |
| Analog Gain Adjustment | | 12.5 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −1.7 dBm) | | −67 | | dBc |

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| OUTPUT FREQUENCY = 2550 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 16.5 | | dBm |
| Analog Gain Adjustment | | 10 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −1.4 dBm) | | −68.5 | | dBc |
| OUTPUT FREQUENCY = 2630 MHz | | | | |
| Maximum $P_{OUT}$ (1-Tone, 0 dBFS) | | 16 | | dBm |
| Analog Gain Adjustment | | 10 | | dB |
| 4-Carrier W-CDMA ACLR ($P_{OUT}$ = −2.3 dBm) | | −66.5 | | dBc |

[1] Exact RF output frequency is determined by VCO selection. See the Ordering Guide section for details.
[2] 921.6 MSPS and other frequencies are also supported.
[3] The board supports zero IF as well as complex IF. The default is complex IF with an IF frequency of 184.32 MHz.
[4] The frequency range is determined by the installed VCO. See the Ordering Guide section for details.

## OBSERVATION SPECIFICATIONS

**Table 4.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| OVERALL FUNCTION | | | | |
| Resolution (Real) | | 12 | | Bits |
| ADC Sample Rate[1] | | 245.76 | | MSPS |
| ADC IF Input Frequency[2] | | 184.32 | | MHz |
| Bandwidth | | 122.88 | | MHz |
| $Z_{IN}$ | | 50 | | Ω |
| Analog Gain Adjustment | | 24 | | dB |
| INPUT FREQUENCY = 2140 MHz | | | | |
| Pass-Band Flatness | | ±1 | | dB |
| Maximum $P_{IN}$ | | 10 | | dBm |
| Input Referred Noise Floor | | −143 | | dBFS/Hz |
| Input IMD (−7 dBFS/Tone) | | −62 | | dBc |

[1] 184.32 MSPS and other frequencies are also supported up to 491.52 MSPS.
[2] The default IF is 184.32 MHz but can be changed based on application requirements.

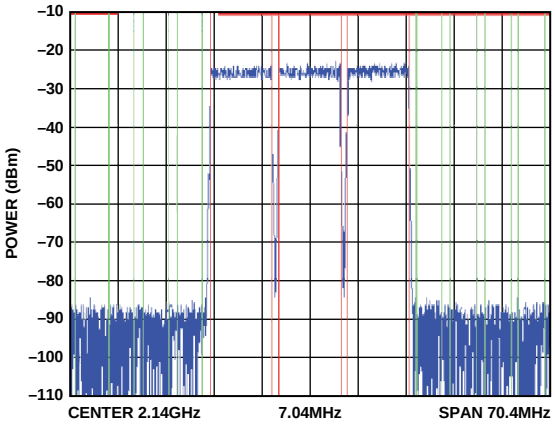
## CLOCK SPECIFICATIONS

**Table 5.**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Reference Frequency[1] | 30.72 | | 307.2 | MHz |
| Clean-Up Clock Reference Frequency[2] | | 122.88 | | MHz |
| LO Reference Frequency[3] | | 26.0 | | MHz |
| Clock Synthesizer Reference Frequency[4] | | 1966.08 | | MHz |
| ADC Sample Rate[5] | | 245.76 | | MSPS |
| DAC Sample Rate[6] | | 983.04 | | MSPS |
| Tx LO Frequency[7] | | 2324.32 | | MHz |

[1] Supported frequencies include n times 30.72 MHz as well as n times 38.4 MHz.
[2] 122.88 MHz is the installed reference; 61.44 MHz is also supported.
[3] 26.0 MHz is the installed reference; 13.0 MHz is also supported.
[4] 1843.2 MHz is also available to support systems developed in China. Other frequencies can also be used.
[5] 184.32 MHz is also available to support systems developed in China. Other frequencies can also be used.
[6] 921.6 MHz is also available to support systems developed in China. Other frequencies can also be used.
[7] See the Ordering Guide section for frequency bands supported. Each band uses a unique LO frequency.

# TYPICAL PERFORMANCE CHARACTERISTICS




| STANDARD: X-UTRA/LTE SQUARE/RRC | | | LOWER | UPPER |
|---|---|---|---|---|
| Tx CHANNELS | | ADJACENT | –68.20dB | –68.67dB |
| CH1 (REF) | –2.05dBm | ALTERNATE | –69.37dB | –69.22dB |
| CH2 | –1.73dBm | 2ND ALT | –69.21dB | –68.18dB |
| CH3 | –1.53dBm | 3RD ALT | –69.45dB | –69.20dB |
| TOTAL | 3.01dBm | | | |

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*Figure 3. Three-Carrier LTE Output*

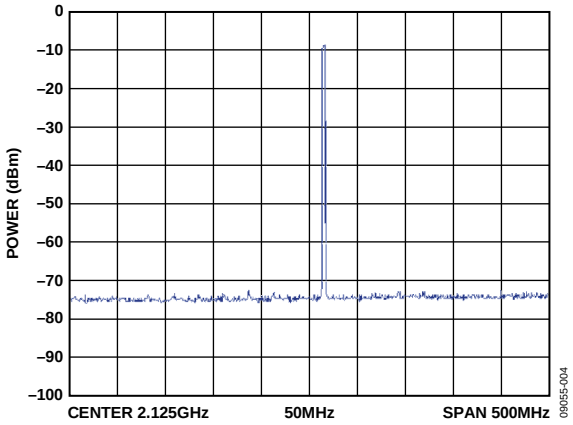


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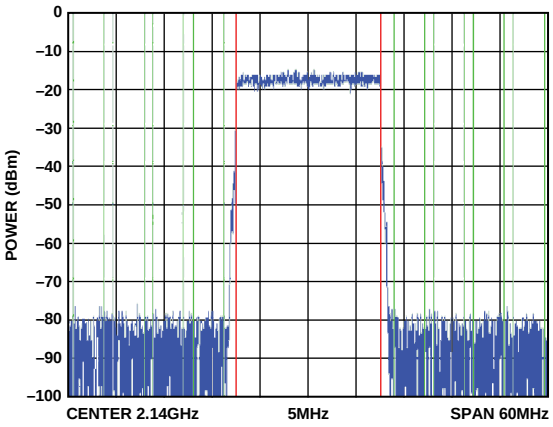
*Figure 4. Six-Carrier GSM Wideband Output*




| CHANNEL | BANDWIDTH | SPACING | LOWER | UPPER |
|---|---|---|---|---|
| Tx CHANNELS | 18.03MHz | | 3.15dBm | |
| ADJACENT | 3.840MHz | 12.500MHz | –72.92dB | –73.47dB |
| ALTERNATE | 3.840MHz | 17.500MHz | –73.03dB | –74.05dB |
| 2ND ALT | 3.840MHz | 22.500MHz | –73.20dB | –73.57dB |
| 3RD ALT | 3.840MHz | 37.500MHz | –72.73dB | –74.14dB |

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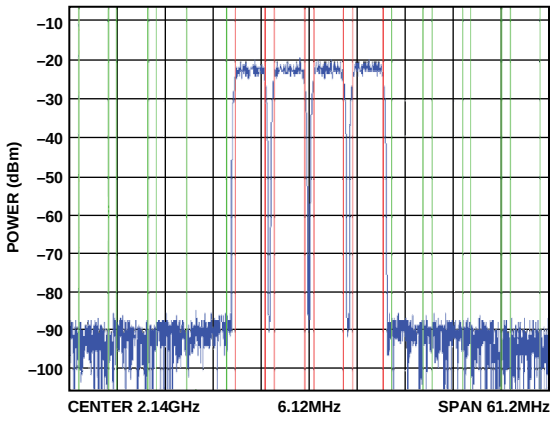
*Figure 5. 20 MHz LTE Output*




| STANDARD: W-CDMA SGFF FWD | | | LOWER | UPPER |
|---|---|---|---|---|
| Tx CHANNELS | | ADJACENT | –67.00dB | –67.34dB |
| CH1 (REF) | –2.39dBm | ALTERNATE | –67.81dB | –67.79dB |
| CH2 | –2.20dBm | 2ND ALT | –68.73dB | –69.01dB |
| CH3 | –2.11dBm | 3RD ALT | –69.15dB | –69.87dB |
| CH4 | –1.74dBm | | | |
| TOTAL | 3.92dBm | | | |

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*Figure 6. Four-Carrier W-CDMA Output*

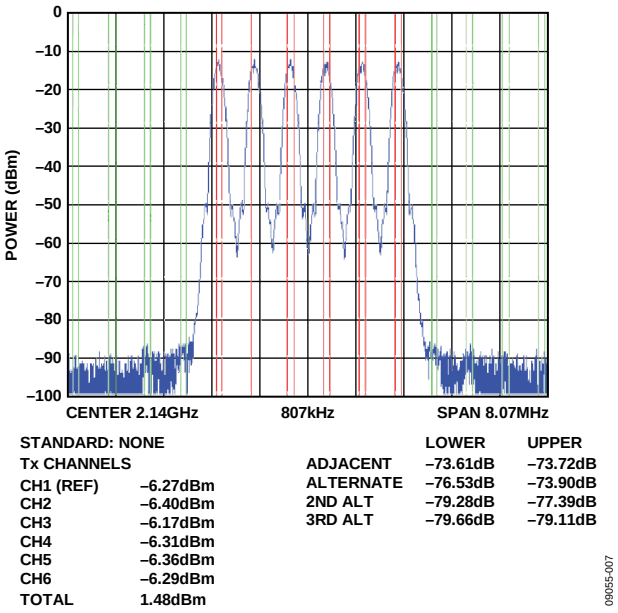


*Figure 7. Six-Carrier GSM Output*

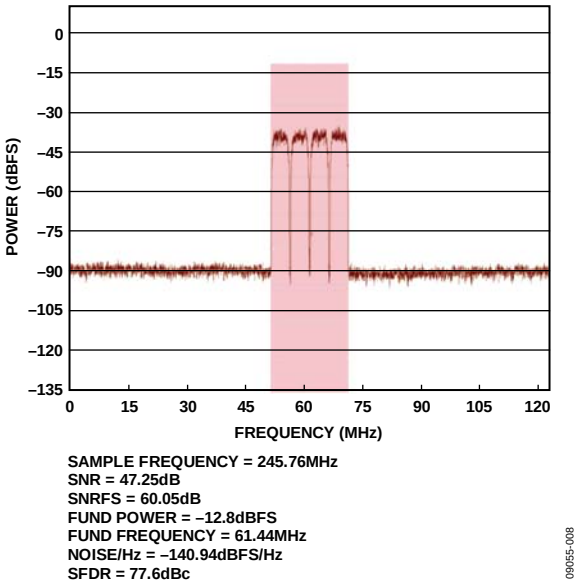


*Figure 8. Four-Carrier W-CDMA Loopback Performance*

# THEORY OF OPERATION

## MAIN Tx PATH

The transmit path is responsible for taking complex I and Q signals and converting them into an appropriate RF signal. This is accomplished by using the modulation capabilities built into the AD9122 high speed digital-to-analog converter (DAC). The DAC upsamples the data to 983.04 MSPS and applies a frequency translation of 184.32 MHz to the data stream. Although zero IF can be used, using complex IF shifts the main signal away from dc where LO feedthrough and images can be easily filtered and otherwise mitigated.

The complex analog output from the DAC feeds an ADL5375 quadrature modulator via an appropriate filter and matching stage, where it is translated to the specified RF output frequency. This signal is then passed through an image rejection filter to an ADL5541 for gain followed by a PIN diode for power control, and, finally, to an ADL532x to drive the output. RF output power control is accomplished either by adjusting the baseband data or by controlling the voltage on the PIN diode.

RF outputs up to 2.7 GHz can be synthesized with this board at power levels up to 18 dBm. Analog power control of up to 12 dB can be achieved with analog gain control depending on the RF output. Additional control is achieved with baseband data control.

## OBSERVATION Rx PATH

The observation path consists of an ADL536x mixer, which is responsible for directly mixing the observed RF signal to a suitable IF. The typical IF frequency is 184.32 MHz but can be changed based on application requirements. The IF signal is filtered and then passed to an AD8375 DVGA, which provides 24 dB of gain range. An antialias filter is used to remove harmonics and other out-of-band signals before the signal is digitized with an AD9230 12-bit, 250 MSPS ADC.

## CLOCK CLEAN-UP

An ADF4002 with a 122.88 MHz VCXO is used to provide clock clean-up facilities. The reference input comes from the on-board 30.72 MHz reference crystal or from an external reference of n times 30.72 MHz or n times 38.4 MHz. Because a narrow loop filter and VCXO are used, much of the wideband noise on the reference clock is attenuated. The output of the clock clean-up function is used as a reference for the clock synthesis and LO synthesis.

## CLOCK SYNTHESIS

An AD9516 uses the 122.88 MHz reference from the clock clean-up to synthesize the ADC sample clock, the DAC sample clock, and all other system clocks, including any signaling needed to interface to the FPGA and SERDES Tx signals. The AD9516 includes an on-chip VCO that runs nominally at 1966.08 MHz and is divided down to achieve the individual clock signals used. Other VCO frequencies can be used to support other clock rates, including those typically used in China.

## LO SYNTHESIS

A number of options exist for local oscillator synthesis, including the option to use external LOs for both the Tx and Rx paths. The on-board synthesis is accomplished by first synthesizing a 26.0 MHz reference from the 122.88 MHz reference clock. This frequency is used because of the ease of generating 200 kHz rasters for some air standards. This is not strictly required and can be bypassed if desired; however, bypassing can result in odd frequency steps that may need to be accounted for by shifting the baseband data. Although shifting the baseband data is not difficult, many customers prefer not to shift their baseband data.

The 26.0 MHz reference is passed to a fractional N PLL and selected external VCO, which is used to generate the Tx local oscillator. An external VCO was chosen because of its superior phase noise characteristics, making it suitable for multicarrier GSM applications. In applications where the Tx and Rx IF frequencies are the same, this local oscillator may be shared. The MSDPD board supports this sharing as the primary option. A secondary synthesizer, the ADF4350, is provided and may be used when the Rx IF is different from the Tx IF. This PLL includes an on-chip VCO. In applications where the ADF4350 is not required for the Rx LO, this synthesizer can be used to synthesize other signals needed elsewhere in the design.

# USER INTERFACE

The AD-MSDPD-EVB includes two integrated user interfaces. The primary interface is a graphical user interface (GUI) that provides simplified access to all key registers on the board. This GUI takes high level input from the user and computes the required low level register values. With the GUI, the user is not required to compute complicated equations to determine which values must be written for board operation. In addition, the GUI simplifies analog interfacing by providing controls that simplify alignment of analog functions including LO feedthrough rejection and image rejection.

The secondary interface is a complete interface to the low level bit maps of each device on the board. This interface is not required but is provided for customers who choose to change the low level settings to optimize performance for their application. This secondary interface enables automation with external processes, such as Python, MATLAB, and LabVIEW, when communications between an external process and the MSDPD controller are required.

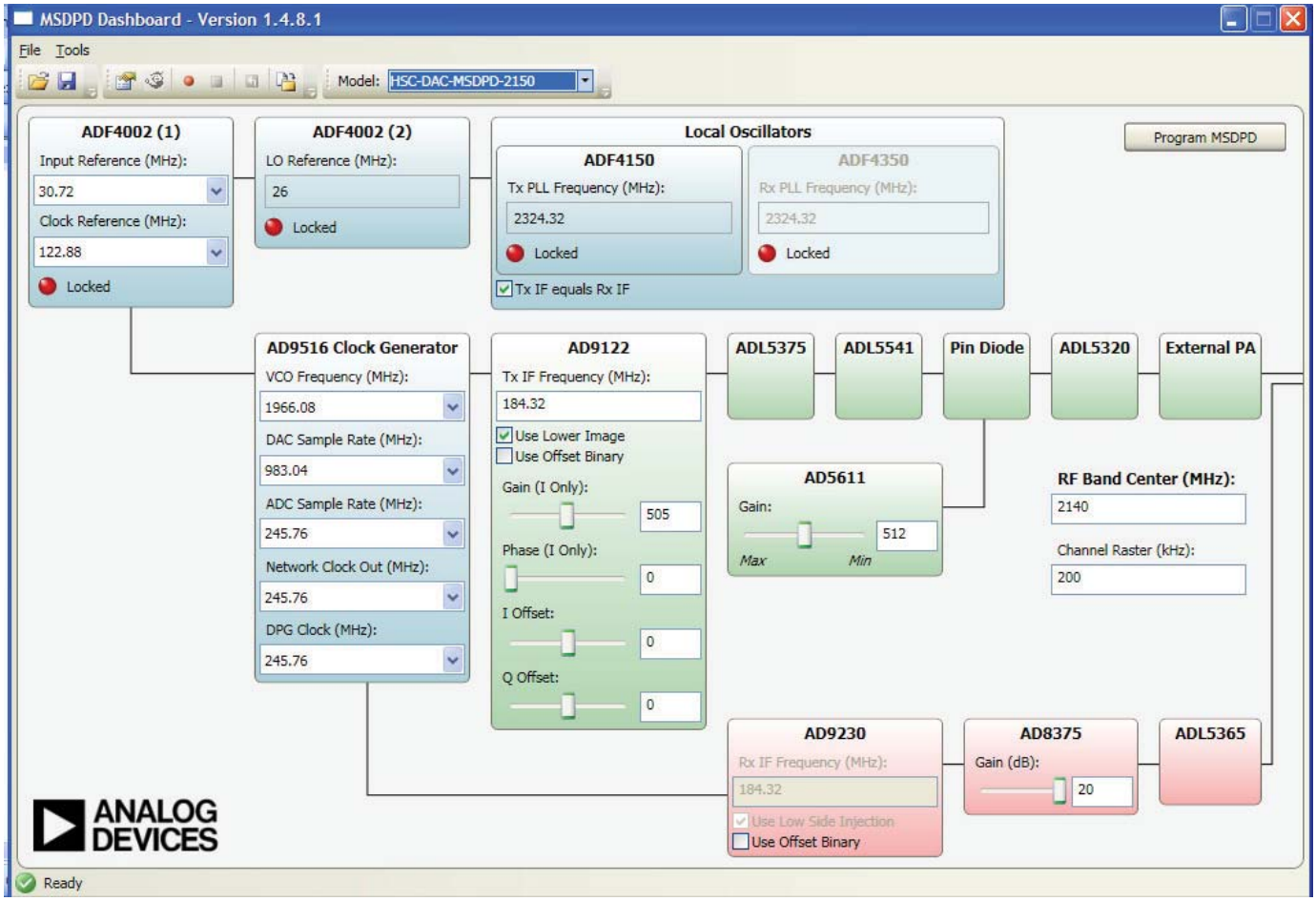


*Figure 9. Simplified User Interface*

# OUTLINE DIMENSIONS

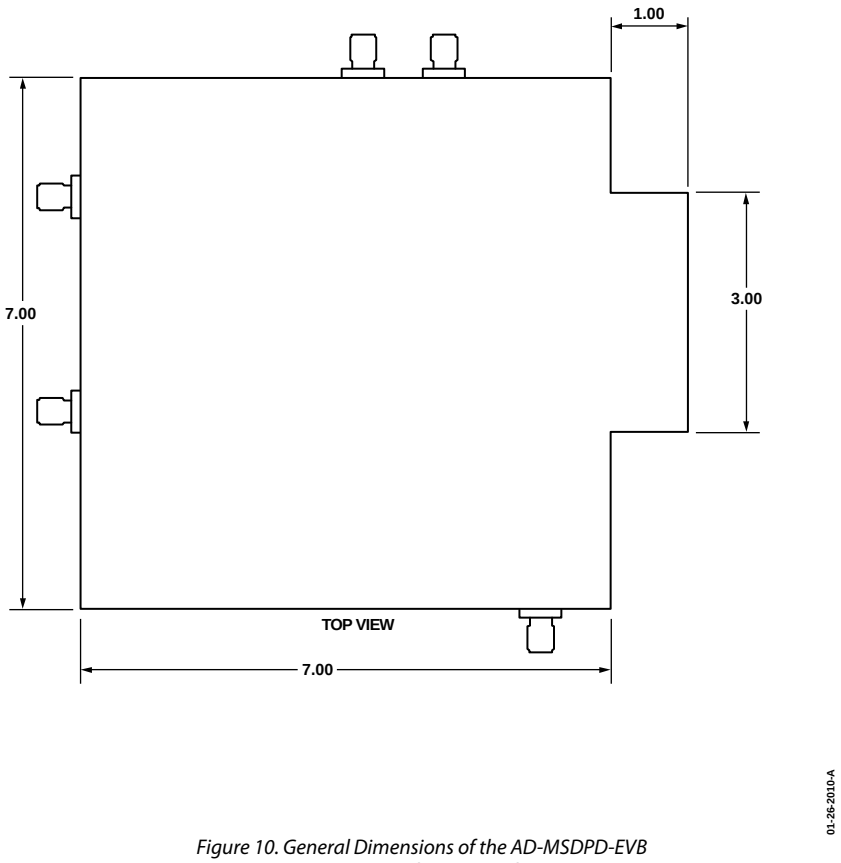


*Figure 10. General Dimensions of the AD-MSDPD-EVB*
*Dimensions Shown in Inches*

## ORDERING GUIDE

| Model | RF Frequency Range[1] | Package Option |
|---|---|---|
| AD-MSDPDX900-EVB | 820 MHz to 1050 MHz | Xilinx FMC Interface |
| AD-MSDPDX1850-EVB | 1820 MHz to 1920 MHz | Xilinx FMC Interface |
| AD-MSDPDX2000-EVB | 1920 MHz to 2100 MHz | Xilinx FMC Interface |
| AD-MSDPDX2150-EVB | 2110 MHz to 2210 MHz | Xilinx FMC Interface |
| AD-MSDPDX2350-EVB | 2300 MHz to 2400 MHz | Xilinx FMC Interface |
| AD-MSDPDX2500-EVB | 2480 MHz to 2580 MHz | Xilinx FMC Interface |
| AD-MSDPDX2600-EVB | 2580 MHz to 2680 MHz | Xilinx FMC Interface |
| AD-MSDPDA900-EVB | 820 MHz to 1050 MHz | Altera HSMC Interface |
| AD-MSDPDA1850-EVB | 1820 MHz to 1920 MHz | Altera HSMC Interface |
| AD-MSDPDA2000-EVB | 1920 MHz to 2100 MHz | Altera HSMC Interface |
| AD-MSDPDA2150-EVB | 2110 MHz to 2210 MHz | Altera HSMC Interface |
| AD-MSDPDA2350-EVB | 2300 MHz to 2400 MHz | Altera HSMC Interface |
| AD-MSDPDA2500-EVB | 2480 MHz to 2580 MHz | Altera HSMC Interface |
| AD-MSDPDA2600-EVB | 2580 MHz to 2680 MHz | Altera HSMC Interface |

[1] Assumes a complex IF output of ~184.32 MHz.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# NOTES

# NOTES


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