DATA SHEET

SKY12343-364LF: 0.1 – 4.0 GHz Seven-Bit Digital Attenuator with Serial and Parallel Drivers

Applications

- Cellular and 3G infrastructure
- WiMAX, LTE, 4G infrastructure

Features

- Broadband operation: 0.1 to 4.0 GHz
- Attenuation range: 31.75 dB with 0.25 dB LSB
- TTL/CMOS-compatible serial, parallel, or latched parallel control interface
- Single supply voltage: +3.3 or +5 V
- Small, QFN (32-pin, 5 x 5 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)

NEW

Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

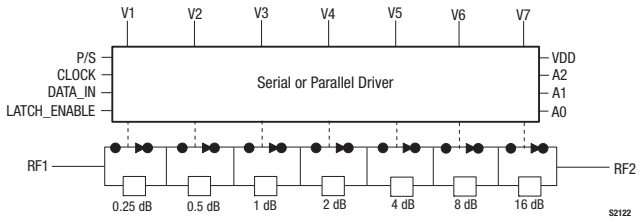


Figure 1. SKY12343-364LF Block Diagram

Description

The SKY12343-364LF is a GaAs broadband seven-bit pHEMT digital attenuator with a 0.25 dB Least Significant Bit (LSB). A TTL/CMOS-compatible, dual mode serial or parallel programming interface (SPI) controller is integrated into the device.

The SKY12343-364LF attenuator features low insertion loss, excellent attenuation accuracy, a 31.75 dB attenuation range, and high linearity performance. The device is an ideal choice for a wide variety of 3G and 4G cellular infrastructure applications.

Attenuation is controlled by an SPI controller. Depending on the SPI sequence applied to the DATA_IN pin, the attenuation state between the RF1 and RF2 pins is programmed between a low insertion loss state or up to 31.75 dB. The V1 through V7 DC control pins determine the attenuation state if parallel mode is enabled.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

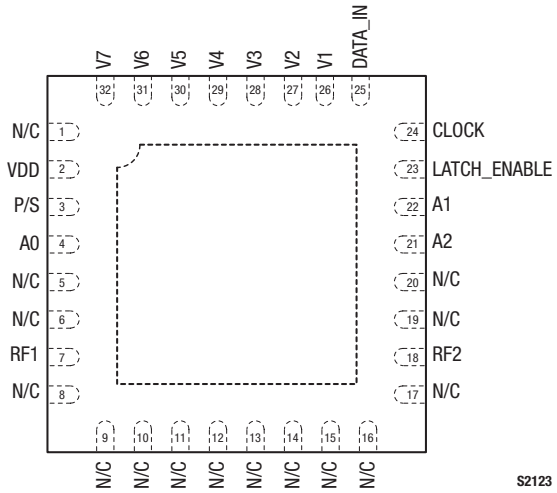


Figure 2. SKY12343-364LF Pinout – 32-Pin QFN (Top View)

Table 1. SKY12343-364LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	N/C	No connection (Note 1)	17	N/C	No connection (Note 1)
2	VDD	DC power supply	18	RF2	RF input/output to digital attenuator
3	P/S	Serial or parallel operation select. Logic low enables parallel mode.	19	N/C	No connection (Note 1)
4	A0	Address bit A0	20	N/C	No connection (Note 1)
5	N/C	No connection (Note 1)	21	A2	Address bit A2
6	N/C	No connection (Note 1)	22	A1	Address bit A1
7	RF1	RF input/output to digital attenuator	23	LATCH_ENABLE	On rising edge of pulse, shifts six most recent bits clocked in to set the attenuation state. In parallel mode, if this signal is logic high, changes to the V1 through V7 signals occur directly. If this signal is logic low, the attenuator does not change states until this signal is raised.
8	N/C	No connection (Note 1)	24	CLOCK	Clock input
9	N/C	No connection (Note 1)	25	DATA_IN	Serial data input
10	N/C	No connection (Note 1)	26	V1	Parallel attenuation control input
11	N/C	No connection (Note 1)	27	V2	Parallel attenuation control input
12	N/C	No connection (Note 1)	28	V3	Parallel attenuation control input
13	N/C	No connection (Note 1)	29	V4	Parallel attenuation control input
14	N/C	No connection (Note 1)	30	V5	Parallel attenuation control input
15	N/C	No connection (Note 1)	31	V6	Parallel attenuation control input
16	N/C	No connection (Note 1)	32	V7	Parallel attenuation control input

Note 1: May be connected to ground with no change in performance.

Functional Description

The SKY12343-364LF is a seven-bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by a serial or parallel interface. Attenuation is set by a stream of data that is clocked into the shift registers of the silicon chip by the CLOCK signal.

Pin 3 (P/S) selects the input mode of the attenuator. A logic low signal applied to pin 3 enables parallel mode; a logic high enables serial mode.

Serial Data Programming

Serial input data (DATA_IN pin) is shifted into the register on the rising edge of the clock signal (CLOCK pin), Least Significant Bit (LSB) first. The attenuator changes states on the rising edge of the latch enable signal (LATCH_ENABLE pin) according to the most recent seven bits of shifted data accepted since the previous falling edge of the latch enable signal.

Refer to the timing diagram in Figure 3 and timing parameters in Table 2.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12343-364LF are provided in Table 3. Electrical specifications are provided in Table 4.

Typical performance characteristics of the SKY12343-364LF are illustrated in Figures 4 through 17.

The state of the SKY12343-364LF is determined by the logic provided in Table 5.

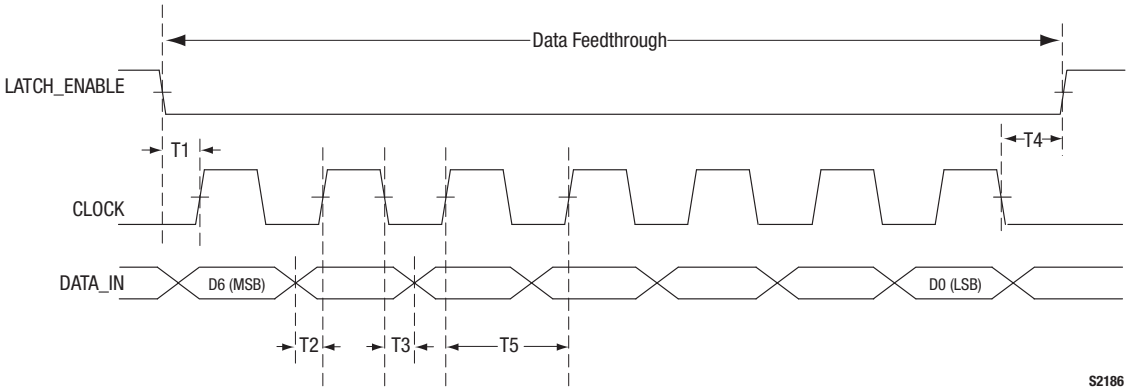


Figure 3. Power-Up/Power-Down Timing

Table 2. Power-Up/Power-Down Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
LATCH ENABLE setup time	T1	7.5	15		ns
DATA_IN setup time	T2	7.5	15		ns
DATA_IN hold time	T3	5	10		ns
LATCH ENABLE hold time	T4	5	10		ns
CLOCK frequency	f_{CLK}		16	100	MHz
CLOCK period	T5		$1/f_{CLK}$		

Table 3. SKY12343-364LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{DD}	3.3	5.0	+6.0	V
Control voltage	V_{CTL}	0	5	V_{DD}	V
Input voltage	V_I	–0.5 – V_{DD}		+0.5	V
RF input power	P_{IN}			+25	dBm
Storage temperature	T_{STG}	–65		+150	°C
Operating temperature	T_{OP}	–40		+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. SKY12343-364LF Electrical Specifications (Note 1)
(T_{OP} = +25 °C, V_{DD} = 5 V, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss	IL	0.1 to 1.5 GHz		1.8	2.0	dB
		1.5 to 3.0 GHz		1.9	3.0	dB
Attenuation range	Attn	0.1 to 4.0 GHz		0.25	31.75	dB
Attenuation accuracy		0.1 to 3.0 GHz:				
		0 dB to 7.75 dB Attn			±(0.20 + 1.5%)	dB
		8 dB to 31.75 dB Attn			±(0.15 + 5%)	dB
		3.0 to 4.0 GHz:				
		0 dB to 31.75 dB Attn			±(0.25 + 4.5%)	dB
Return loss	RL	0.1 to 4.0 GHz		18		dB
Relative phase	PH	0.1 to 4.0 GHz		44		deg
1 dB Input Compression Point	IP1dB	0.5 MHz to 3.0 GHz, insertion loss state		+35		dBm
0.1 dB Input Compression Point	IP0.1dB	0.5 MHz to 3.0 GHz:				
		Insertion loss state		+32		dBm
		Attenuation states		+25		dBm
3rd Order Input Intercept Point	IIP3	Two tones @ +18 dBm, 20 MHz spacing		+50		dBm
DC Specifications						
On/Off switching time	t_{ON}/t_{OFF}	50% V_{CTL} to 90%/10% RF		650		ns
Rise/fall switching time	t_{RISE}/t_{FALL}	50% V_{CTL} to 90%/10% RF		400		ns
Video feedthrough	V_{FD}			20		mVpp

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

(TOP = +25 °C, VDD = 3.3 V, VCTL = 3.3 V, Characteristic Impedance [Zo] = 50 Ω, VDD = 5 V, Unless Otherwise Noted)

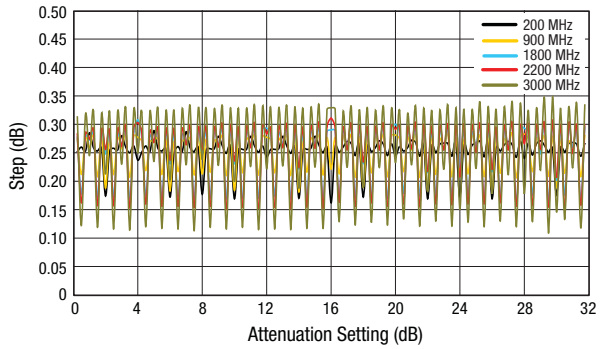


Figure 4. Attenuation Setting vs Step Error

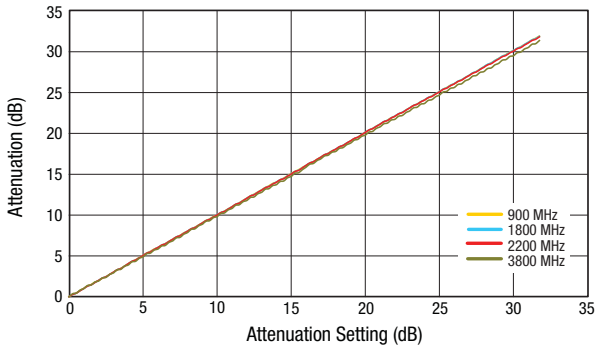


Figure 5. Attenuation vs Attenuation Setting

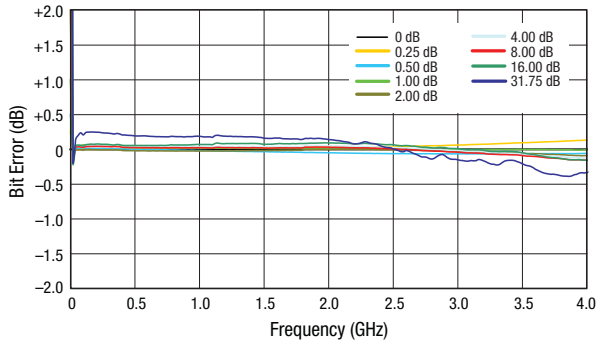


Figure 6. Major State Bit Error vs Frequency

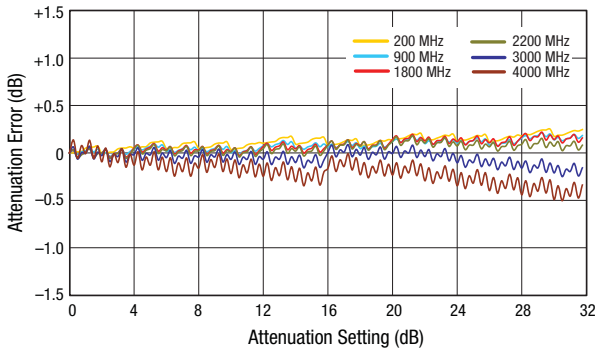


Figure 7. Attenuation Error vs Attenuation Setting

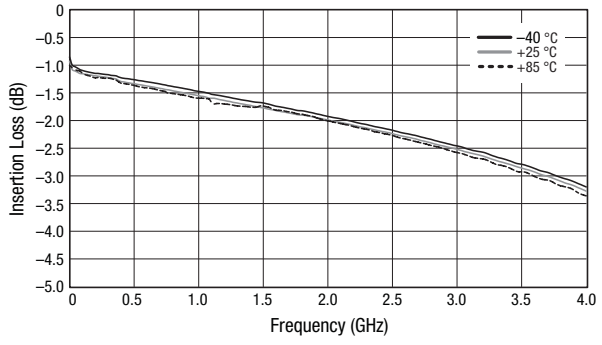


Figure 8. Insertion Loss vs Frequency

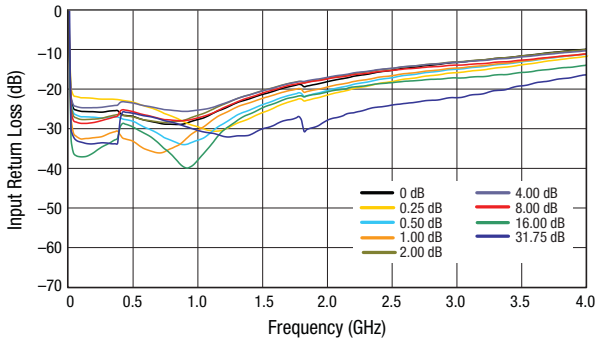


Figure 9. Input Return Loss vs Frequency

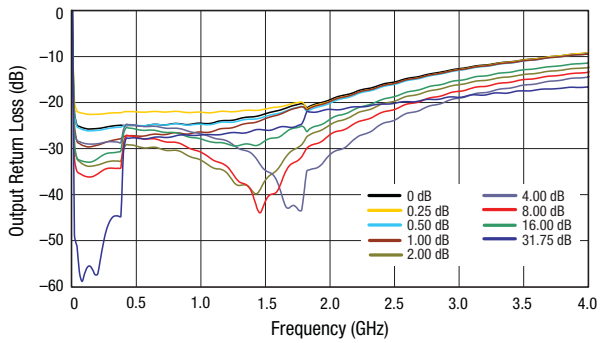


Figure 10. Output Return Loss vs Frequency

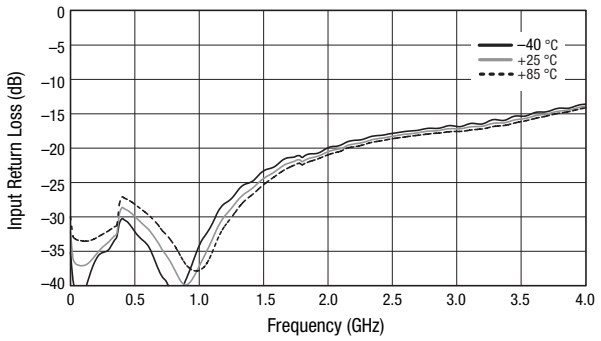


Figure 11. Input Return Loss (16 dB State) vs Frequency

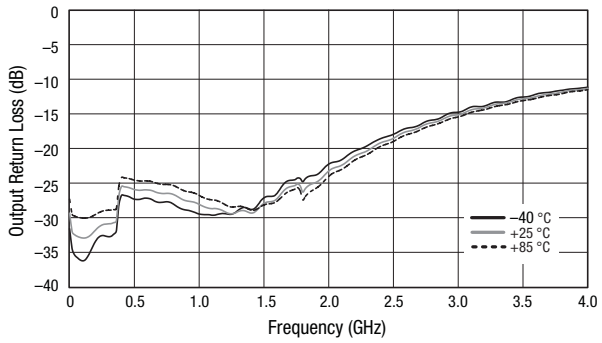


Figure 12. Output Return Loss (16 dB State) vs Frequency

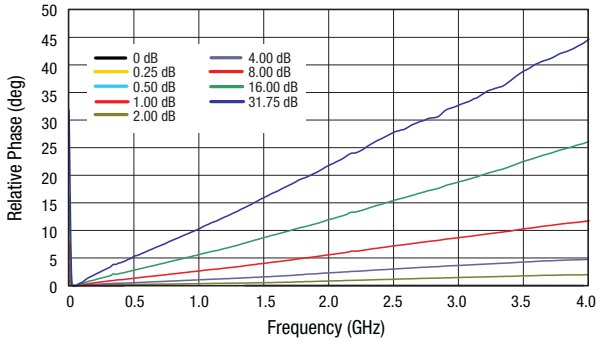


Figure 13. Relative Phase vs Frequency

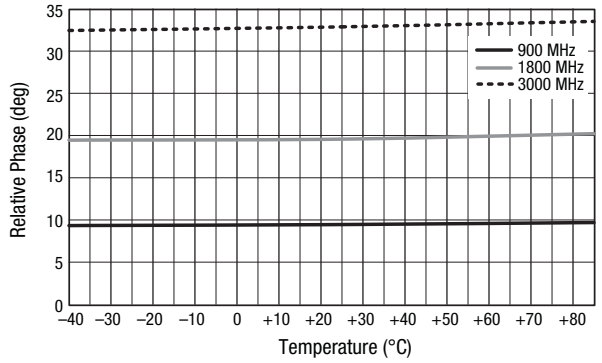


Figure 14. Relative Phase (31.75 dB State) vs Temperature

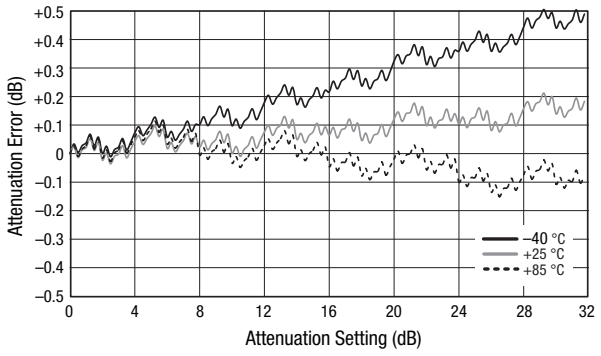


Figure 15. Attenuation Error vs Attenuation Setting @ 900 MHz

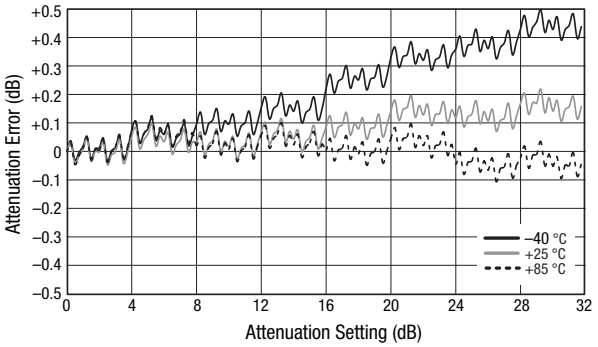


Figure 16. Attenuation Error vs Attenuation Setting @ 1800 MHz

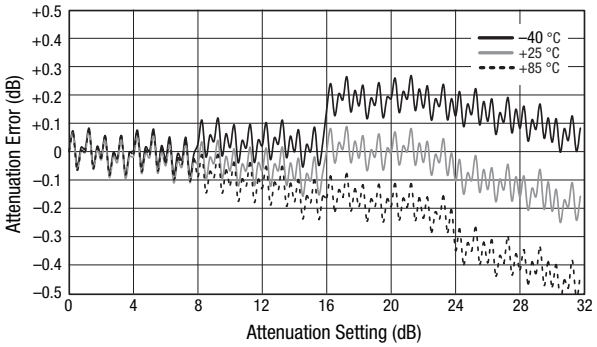


Figure 17. Attenuation Error vs Attenuation Setting @ 3000 MHz

Table 5. SKY12343-364LF Truth Table

Attenuation Setting (RF1 and RF2)	V1 (Pin 26)	V2 (Pin 27)	V3 (Pin 28)	V4 (Pin 29)	V5 (Pin 30)	V6 (Pin 31)	V7 (Pin 32)
Insertion loss	0	0	0	0	0	0	0
0.25 dB	1	0	0	0	0	0	0
0.50 dB	0	1	0	0	0	0	0
1.0 dB	0	0	1	0	0	0	0
2.0 dB	0	0	0	1	0	0	0
4.0 dB	0	0	0	0	1	0	0
8.0 dB	0	0	0	0	0	1	0
16 dB	0	0	0	0	0	0	1
31.75 dB	1	1	1	1	1	1	1

Evaluation Board Description

The SKY12343-364LF Evaluation Board is used to test the performance of the SKY12343-364LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 18 and an Evaluation Board schematic diagram is shown in Figure 19. Table 6 provides the Evaluation Board Bill of Materials (BOM) list.

Package Dimensions

The PCB layout footprint for the SKY12343-364LF is shown in Figure 20. Typical case markings are noted in Figure 21. Package dimensions for the 32-pin QFN are shown in Figure 22, and tape and reel dimensions are provided in Figure 23.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY12343-364LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

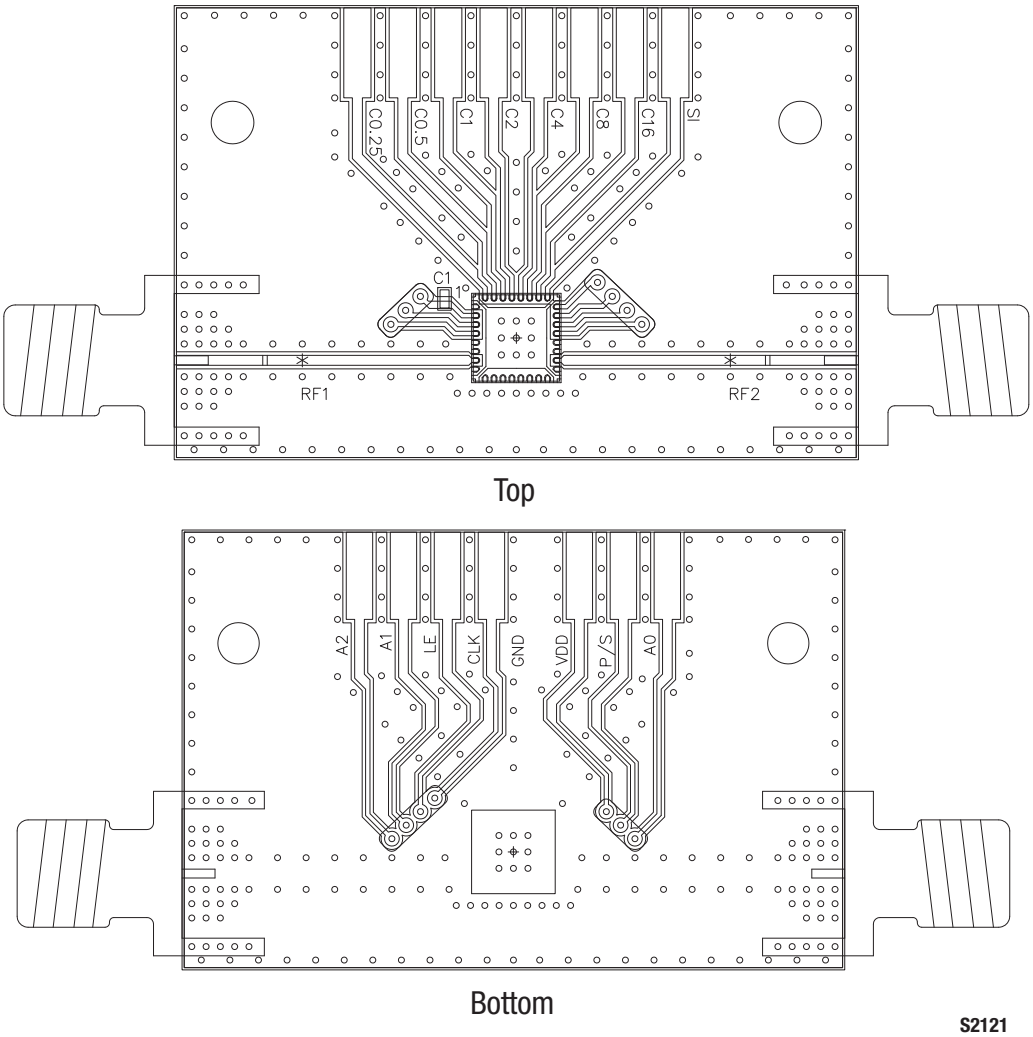


Figure 18. SKY12343-364LF Evaluation Board Assembly Diagram

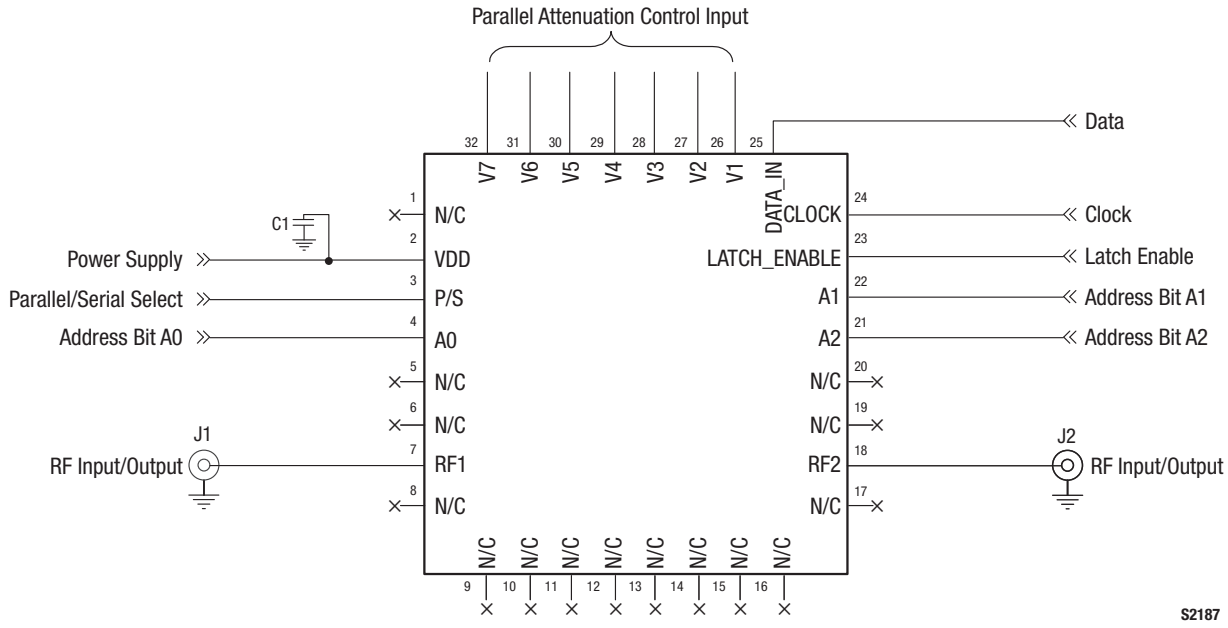


Figure 19. SKY12343-364LF Evaluation Board Schematic Diagram

Table 6. Recommended Evaluation Board Bill of Materials

Component	Value	Size	Manufacturer
C1	0.01 µF	0402	Murata

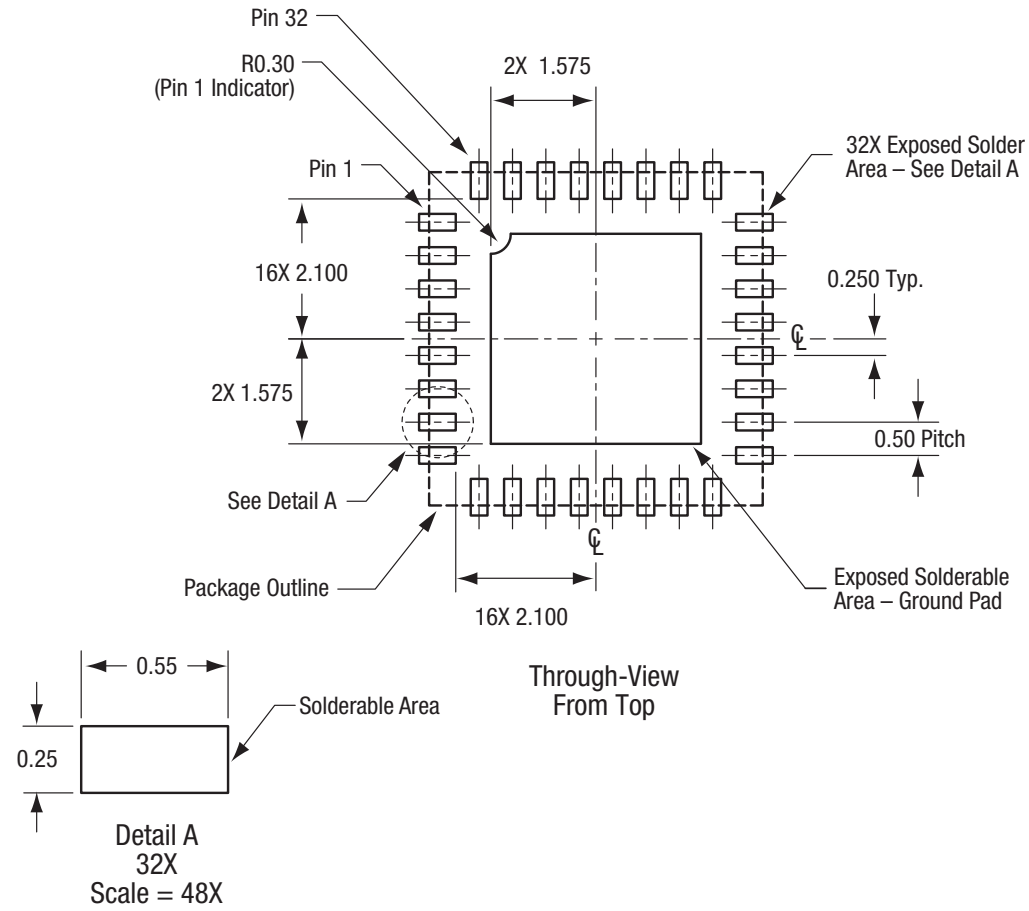


Figure 20. SKY12343-364LF PCB Layout Footprint

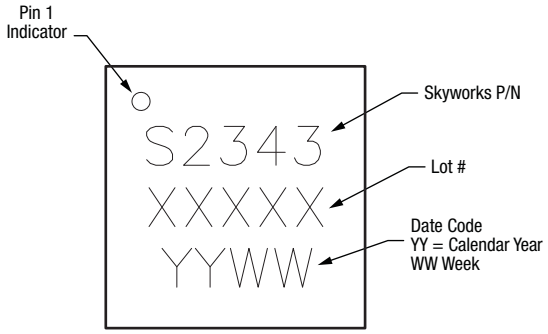
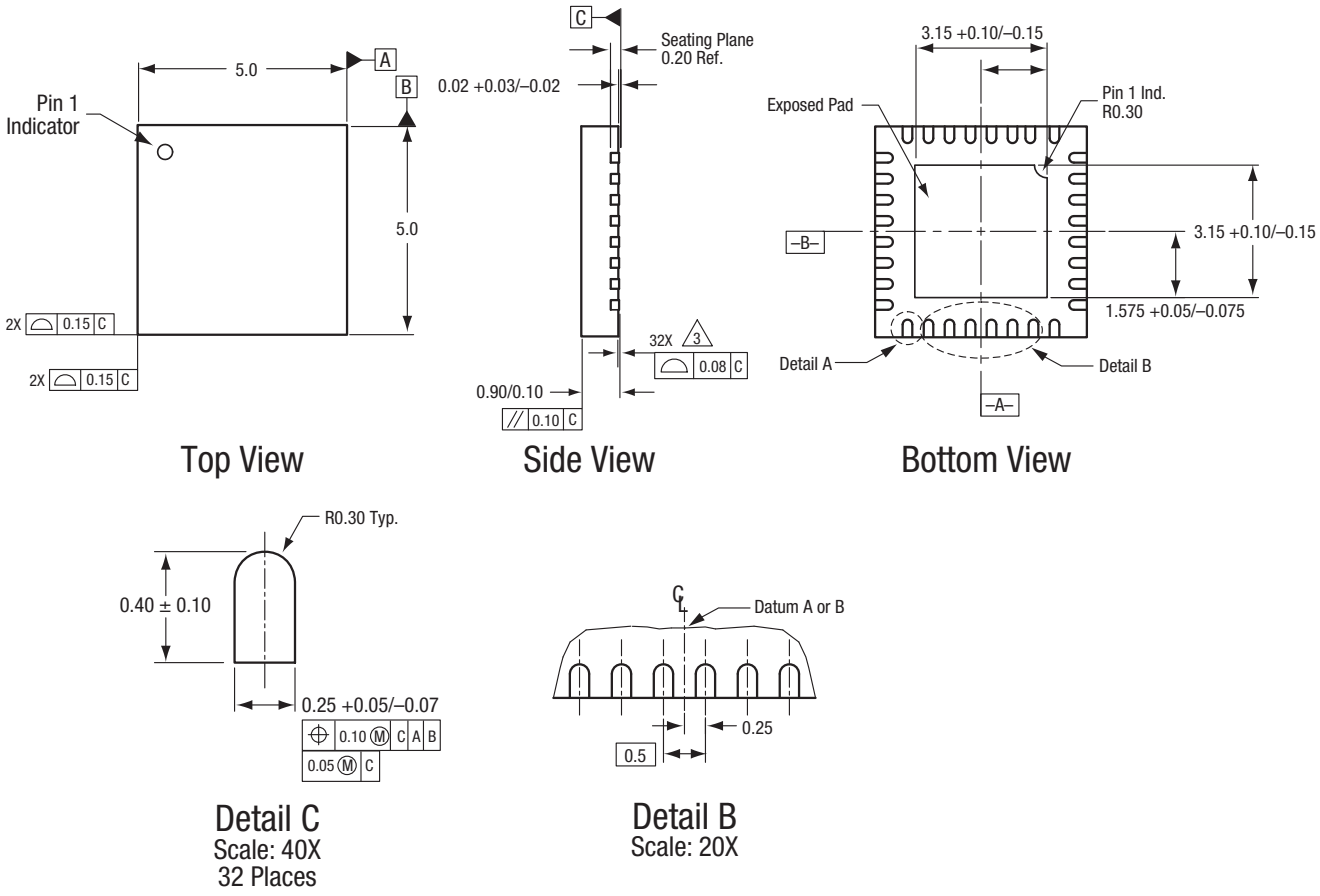


Figure 21. Typical Part Markings



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals..
Plating requirement per source control drawing (SCD) 2504.

S1583

Figure 22. SKY12343-364LF 32-Pin QFN Package Dimensions

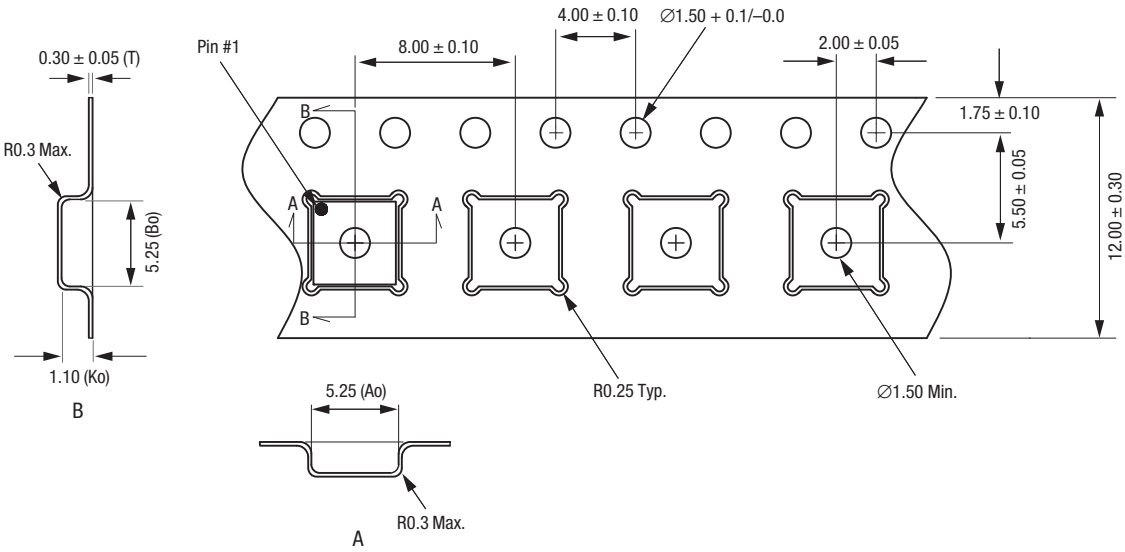


Figure 23. SKY12343-364LF Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Numbers
SKY12343-364LF Digital Attenuator	SKY12343-364LF	SKY12343-364LF-EVB