DATASHEET

AX5043

Advanced high performance ASK and FSK narrow-band transceiver for 70-1050 MHz range

Version 0.2

Preliminary

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Document	Status	PRELIMINARY/CONFIDENTIAL
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Product		AX5043

Table of Contents

1. Overview

1.1. Features

Advanced multi-channel narrow-band single chip UHF transceiver (FSK/MSK/4-FSK/GFSK/GMSK/ASK)

- Data rates from 1 kbps to 100 kbps
- Configurable for usage in 70 MHz -1050 MHz bands in 1 Hz steps
- QFN28 package

Low-Power

- RX 10.5 mA
- TX 12 mA @ 0 dBm, 22mA @ 10dBm, 51mA @ 15dBm
- Power-down with low frequency duty cycle clock running <500nA
- Standby with crystal clock running 230 µA
- 1.8 V - 3.6 V single supply

Receiver

- Sensitivity down to –126 dBm @ 1.2 kbps
- High selectivity receiver with 45 dB neighbor channel rejection
- 0 dBm maximum input power
- +/- 10% data-rate error tolerance
- Short preamble modes allow the receiver to work with as little as 16 preamble bits
- Automatic frequency control (AFC)
- Digital RSSI with 1 dB step resolution

Transmitter

- High efficiency, high linearity integrated power amplifier
- Max. 20 dBm
- Power level programmable in 0.5 dB steps
- GFSK shaping with BT=0.3 or BT=0.5
- Unrestricted power ramp shaping

Frequency Generation

- Configurable for either fully integrated VCO, internal VCO with external inductor or fully external VCO
- Configurable for either fully integrated or external synthesizer loop filter for a large range of bandwidths
- Channel hopping up to 2000 hops/s

Flexible antenna interface

- Integrated RX/TX switching with differential antenna pins
- Extra single-ended PA

Wakeup-on-Radio

- 640 Hz or 10 kHz lowest power wake-up timer
- Wake-up time programmable between 98 µs and 102 s

Sophisticated radio controller

- Fully automatic packet reception and transmission without micro-controller intervention
- Support for antenna diversity with external antenna switch
- Supports HDLC, Raw, and Wireless M-Bus frames
- Automatic channel noise level tracking
- µs resolution timestamps for exact timing (eg. for frequency hopping systems)
- Supports also packet sizes > 256 Bytes
- Ability to store RSSI, frequency offset and data-rate offset with the packet data
- 256 bytes packet buffer or FIFO
- SPI micro-controller interface
- Extended AXSEM register set

Advanced Crystal Oscillator

- **Fast start-up and lowest power steady-state XTAL oscillator for a wide range of crystals**
- **Integrated tuning capacitors**
- **Possibility of applying an external clock reference (TCXO)**

Miscellaneous features

- **10 bit 1MS/s General Purpose ADC (GPADC)**
- **Internal power-on-reset**
- **Brown-out detection**
- **Suited for system targeting compliance to EN 300 220 V2.3.1 and FCC CFR part 15**

Applications

70 MHz – 1050 MHz licensed and unlicensed radio systems.

- **Suited for system targeting compliance to EN 300 220 V2.3.1 and FCC CFR part 90 for 6.25 kHz, 12.5 kHz and 25 kHz narrow-band standards**
- **Suited for systems targeting compliance with Wireless M-Bus standard EN 13757-4:2005**
- AMR
- Security
- Messaging / Paging
- Wireless Sensors
- Remote controls

2. Block Diagram

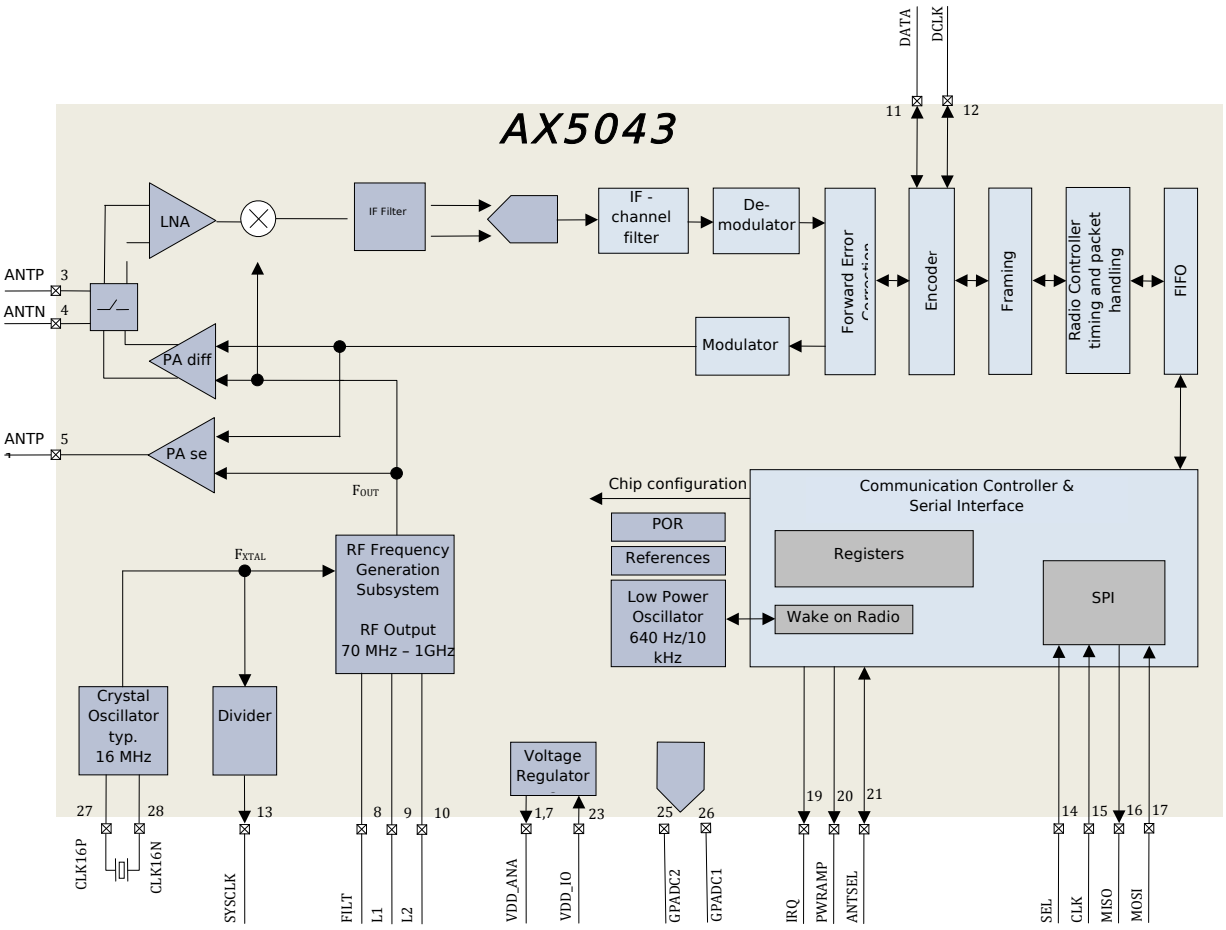


Figure 1 Functional block diagram of the AX5043

3. Pin Function Descriptions

Symbol	Pin(s)	Type	Description
VDD_ANA	1	P	Analog power output, decouple to neighboring GND
GND	2	P	Ground, decouple to neighboring VDD_ANA
ANTP	3	A	Differential antenna input/output
ANTN	4	A	Differential antenna input/output
ANTP1	5	A	Single-ended Antenna output
GND	6	P	Ground, decouple to neighboring VDD_ANA
VDD_ANA	7	P	Analog power output, decouple to neighboring GND
FILT	8	A	Optional synthesizer filter
L2	9	A	Optional synthesizer inductor
L1	10	A	Optional synthesizer inductor
DATA	11	I/O	In wire-mode: Data in-out/output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
DCLK	12	I/O	In wire-mode: Clock output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
NC	18	N	Must be left unconnected
IRQ	19	I/O	Default functionality: Transmit and receive interrupt Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
PWRAMP	20	I/O	Default functionality: Power amplifier control output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
ANTSEL	21	I/O	Default functionality: Diversity antenna selection output Can be programmed to be used as a general purpose I/O pin Selectable internal 65 kΩ pull-up resistor
NC	22	N	Must be left unconnected
VDD_IO	23	P	Power supply 1.8 V – 3.3 V
NC	24	N	Must be left unconnected
GPADC1	25	A	GPADC input
GPADC2	26	A	GPADC input
CLK16P	27	A	Crystal oscillator input/output
CLK16N	28	A	Crystal oscillator input/output
GND	Center -pad	P	Ground on center pad of QFN, must be connected

A	=	analog signal	I/O	=	digital input/output signal
I	=	digital input signal	N	=	not to be connected
O	=	digital output signal	P	=	power or ground

All digital inputs are Schmitt-trigger-inputs, digital input and output levels are LVCMOS/LVTTL compatible and 5V tolerant.

3.1. Pin-out Drawing

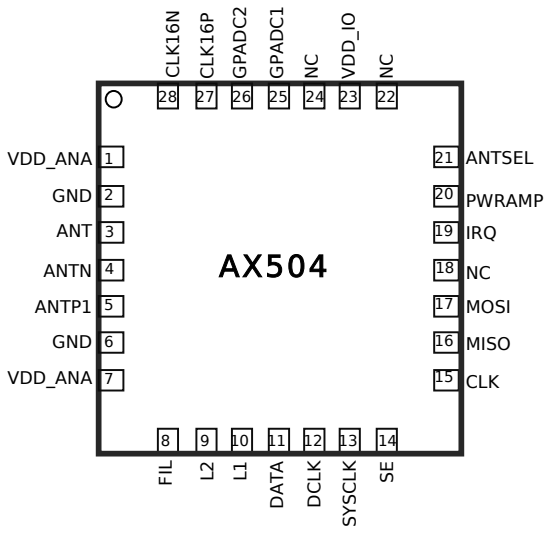


Figure 2: Pin-out drawing (Top view)

4. Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
VDD_IO	Supply voltage		-0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN, ANTP1		-10	10	mA
I_{I2}	DC current into pins ANTP, ANTN, ANTP1		-100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN , ANTP1 pins		-0.5	5.5	V
	Input voltage digital pins		-0.5	5.5	V
V_{es}	Electrostatic handling	HBM	-2000	2000	V
T_{amb}	Operating temperature		-40	85	°C
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction Temperature			150	°C

4.2. DC Characteristics

Supplies

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
T_{AMB}	Operational ambient temperature		-40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage		1.8	3.0	3.6	V
V_{BOUT}	Brown-out threshold	Note 1		1.3		V
I_{DSLEEP}	Deep-sleep current: All analog and digital functions are powered down.	PWRMODE=0x01		60		nA
I_{PDOWN}	Power-down current: Register file contents preserved.	PWRMODE=0x00		300		nA
I_{WOR}	Wakeup-on-radio mode: Low power timer and WOR state-machine are running at 640 Hz	PWRMODE=0x0B		400		nA
I_{FIFO}	FIFO access/hold current: Access to the FIFO possible and contents are preserved	PWRMODE=0x06		90		µA
$I_{STANDBY}$	Standby-current: Crystal oscillator and references are running.	PWRMODE=0x05		230		µA
I_{RX}	Current consumption RX PWRMODE=0x09 RF Frequency Subsystem: internal VCO and internal loop-filter	868 MHz, data-rate 6 kbps		10		mA
		868 MHz, data-rate 75 kbps		11		
		433 MHz, data-rate 6 kbps		tbd		
		433 MHz, data-rate 75 kbps		tbd		
$I_{TX-DIFF}$	Current consumption TX PWRMODE=0x0D RF Frequency Subsystem: Internal VCO and loop-filter Antenna configuration: Differential PA, internal RX/TX switching	868 MHz, 16 dBm, FSK		51		mA
		868 MHz, 10 dBm, FSK		28		
		868 MHz, 0 dBm, FSK		14		
		868 MHz, 16 dBm, ASK		54		
		868 MHz, 10 dBm, ASK		31		
		868 MHz, 0 dBm, ASK		17		
I_{TX-SE}	Current consumption TX PWRMODE=0x0D RF Frequency Subsystem: Internal VCO and loop-filter Antenna configuration: Single ended PA, 125 Ω load , internal RX/TX switching	868 MHz, 10 dBm, FSK		22		mA
		868 MHz, 0 dBm, FSK		12		
		868 MHz, -10 dBm, FSK		7		
		868 MHz, 10 dBm, ASK		25		
		868 MHz, 0 dBm, ASK		15		

Notes: 1. Digital circuitry is functional down to typically 1 V.

Logic

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		-10		10	µA
R_{pullup}	Pull-up resistors Pins DATA, DCLK, SYSCLK, IRQ, PWRAMP, ANTSEL	Pull-ups enabled in the relevant pin configuration registers		65		kΩ
Digital Outputs						
I_{OH}	Output Current, high	VDD_IO=3V V_{OH}= 2.4V	4			mA
I_{OL}	Output Current, low	VDD_IO=3V V_{OL}= 0.4V	4			mA
I_{OZ}	Tri-state output leakage current		-10		10	µA

4.3. AC Characteristics

Crystal Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{XTAL}	Crystal frequency	Note 1		16		MHz
gm_{osc}	Oscillator transconductance control range	Self-regulated see note 2	0.2		20	mS
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 0x00 default		3		pF
		XTALCAP = 0x01		8.5		pF
		XTALCAP = 0xFF		40		pF
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP	XTALCAP = 0x01 – 0xFF		0.5		pF
f_{ext}	External clock input	Note 3		16		MHz
V_{ext}	External clock amplitude				0.9	V
RIN_{osc}	Input DC impedance		10			kΩ
$NDIV_{SYSCLK}$	Divider ratio $f_{SYSCLK} = f_{XTAL} / NDIV_{SYSCLK}$		2^0	2^4	2^{10}	

Notes

1. Tolerances and start-up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ
2. The oscillator transconductance is regulated for fastest start-up time during start-up and for lowest power during steady state oscillation. This means that values will depend on the crystal used.
3. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and XTALCAP=0x00

Low-power Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
$f_{osc-slow}$	Oscillator frequency slow mode	LPOSC FAST=0	608	640	672	Hz
$f_{osc-fast}$	Oscillator frequency fast mode	LPOSC FAST=1 Internal calibration vs. crystal clock has been performed	9.8	10.2	10.8	kHz

RF Frequency Generation Subsystem (Synthesizer)

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{REF}	Reference frequency			16		MHz
Dividers						
$NDIV_{ref}$	Reference divider ratio range	Controlled directly with register REFDIV	2^0		2^3	
$NDIV_{main}$	Main divider ratio range	Controlled indirecty with register FREQ	4		67	
$NDIV_{RF}$	RF divider range	Controlled directly with register RFDIV	1		2	
Charge Pump						
I_{CP}	Charge pump current	Programmable in increments of 8.5 µA via register PLLCPI	8.5		2168	µA
Internal VCO (VCOSEL=0)						
f_{RF}	RF frequency range	RFDIV=1	400		525	MHz
		RFDIV=0	800		1050	
f_{step}	RF frequency step	RFDIV=1, fxtal=16.000000 MHz		0.98		Hz
BW_1	Synthesizer loop bandwidth	Loop filter configuration: FLT=01 Charge pump current: 68 µA		100		kHz
BW_2		Loop filter configuration: FLT=10 Charge pump current: 272 µA		200		
BW_3		Loop filter configuration: FLT=11 Charge pump current: 1.7 mA		500		
T_{start1}	Synthesizer start-up time if crystal oscillator and reference are running	Loop filter configuration: FLT=01 Charge pump current: 68 µA		25		µs
T_{start2}		Loop filter configuration: FLT=10 Charge pump current: 272 µA		12		
T_{start3}		Loop filter configuration: FLT=11 Charge pump current: 1.7 mA		5		
PN868	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: 68 µA	868 MHz, 100 kHz from carrier		-100		dBc/Hz
		868 MHz, 300 kHz from carrier		-110		
		868 MHz, 1 MHz from carrier		-125		
PN433	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: 68 µA	433 MHz, 100 kHz from carrier		-112		dBc/Hz
VCO with external inductors (VCOSEL=1, VCO2INT=1)						
f_{RFrng_lo}	RF frequency range	RFDIV=1	70		400	MHz
f_{RFrng_hi}		RFDIV=0	140		800	

f_{mid}	Mid frequency	L_{ext}=15 nH, Q = 54, RFDIV=0 For other values of L_{ext} see Figure 3 and Figure 4		380		MHz
Kvco	VCO gain			7.5		MHz/V
PN380	VCO phase noise	380 MHz, 100 kHz from carrier L_{ext}=15 nH, Q = 54, RFDIV=0		-120		dBc/Hz
		868 MHz, 300 kHz from carrier L_{ext}=15 nH, Q = 54, RFDIV=0		-130		
External VCO (VCOSEL=1, VCO2INT=0)						
f_{RF}	RF frequency range fully external VCO	Note: The external VCO frequency needs to be 2xf_{RF}	70		1000	MHz
Z_{in}	Input impedance			tbd		Ω
V_{amp}	Differential input amplitude at L1, L2 terminals			0.7		V
V_{inL}	Input voltage levels at L1, L2 terminals		0		1.8	V
V_{ctrl}	Control voltage range	Available at FILT in external loop filter mode	0		1.8	V

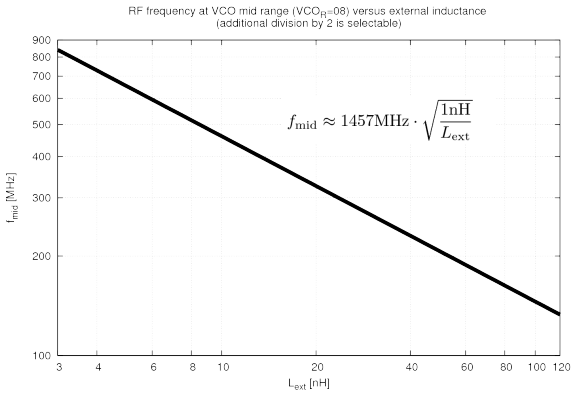


Figure 3 VCO with external inductors: frequency vs L_{ext}

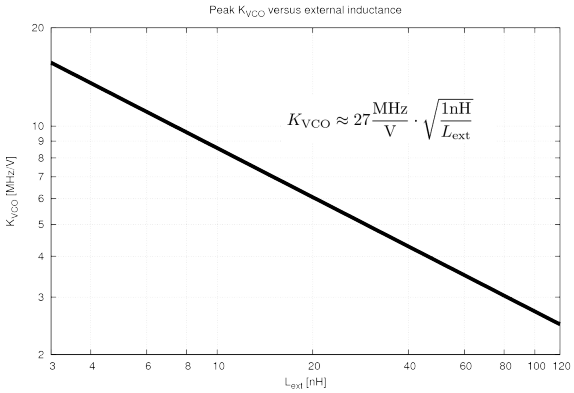


Figure 4 VCO with external inductors: K_{vco} vs L_{ext}

Transmitter

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate		1		75	kbps
PTX_{868}	Transmitter power @ 868 MHz		-10		15	dBm
$PTX_{868\text{-}step}$	Programming step size output power	Note 1			0.5	dB
$PTX_{868\text{-}harm2}$	Emission @ 2nd harmonic	Note 2		-50		dBc
$PTX_{868\text{-}harm3}$	Emission @ 3rd harmonic			-55		

Notes

1. $P_{out} = \frac{TXPWRCOEFFB}{2^{12}-1} \bullet P_{\max}$
2. Additional low-pass filtering was applied to the antenna interface, see section 7: Application Information.

Receiver

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate		1		100	kbps
IS_{868_HS}	Input sensitivity at BER $= 10^{-3}$ for 868 MHz operation	FSK, h = 0.5, 100 kbps		-106		dBm
		FSK, h = 0.5, 10 kbps		-116		
		FSK, h = 0.5, 1 kbps		-126		
IL	Maximum input level				-20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		-35		dBm
IIP3	Input referred IP3			tbd		
RSSIR	RSSI control range			90		dB
RSSIS	RSSI step size	reading register RSSI		1		dB
SEL_{868}	Adjacent channel suppression	FSK 4.8 kbps, h= 0.5, 25 kbps channels Note 1		40		dB
BLK_{868}	Blocking at +/- 1MHz offset	FSK 4.8 kbps, Note 2		tbd		dB
	Blocking at +/- 10MHz offset			tbd		
	Blocking at +/- 100MHz offset			tbd		

Notes

1. Interferer/Channel @ BER $= 10^{-3}$, channel level is +3 dB above the typical sensitivity, the interfering signal is a random data signal; both channel and interferer are modulated with shaping
2. Channel/Blocker @ BER $= 10^{-3}$, channel level is +3 dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated with shaping

SPI Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high-Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	Note 1	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

Notes

1. For SPI access during power-down mode the period should be relaxed to 100ns.

For a figure showing the SPI timing parameters see section 5.16: Serial Peripheral Interface (SPI).

Wire-Mode Interface Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tdck	DCLK period	Depends on bit-rate programming	1.6		10000	µs
Tdcl	DCLK low duration		25		75	%
Tdch	DCLK high duration		25		75	%
Tds	DATA setup time relative to active DCLK edge		10			ns
Tdh	DATA hold time relative to active DCLK edge		10			ns
Tdco	DATA output change relative to active DCLK edge				10	ns

For a figure showing the wire-mode interface timing parameters see section 5.17: Wire-Mode Interface.

General Purpose ADC (GPADC)

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Res	Nominal ADC resolution			10		bit
F_{conv}	Conversion rate				1	MS/s
DR	Dynamic range			60		dB
INL	Integral non linearity			3	5	LSB
DNL	Differential non linearity			0.75	1	LSB
Z_{in}	Input Impedance			50		kΩ
V_{DC-IN}	Input DC level			0.8		V
$V_{IN-DIFF}$	Input signal range in differential mode		0		2	V
V_{IN-SE}	Input signal range in single-ended mode		0		1	V

5. Circuit Description

The AX5043 is a true single chip low-power narrow-band CMOS transceiver primarily for use in SRD bands. The on-chip transceiver consists of a fully integrated RF front-end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user-friendly communication via the SPI interface.

AX5043 can be operated from a 1.8 V to 3.6 V power supply over a temperature range of -40°C to 85°C, it consumes 7 - 70 mA for transmitting, depending on the output power, and 9 - 11 mA for receiving.

The AX5043 features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 and the US Federal Communications Commission (FCC) standard Title 47 CFR part 15 as well as Part 90. AX5043 is compliant with the respective narrow-band regulations.

AX5043 supports any data rate from 1 kbps to 100 kbps for FSK, GFSK, GMSK , MSK and ASK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AX5043 are necessary. To calculate the optimal settings use the AXSEM AX5043 configuration software.

The AX5043 can be operated in two fundamentally different modes.

In **frame-mode** data is sent and received via the SPI port in frames. Pre- and post-ambles as well as checksums can be generated automatically. Interrupts control the data flow between a micro-controller and the AX5043.

In **wire-mode** the IC behaves as an extension of any wire. The internal communication controller is disabled and the modem data is directly available on a dedicated pin (DATA). The bit clock is also output on a dedicated pin (DCLK). In this mode, the user can connect the data pin to any port of a micro-controller or to a UART, but has to control coding, checksums, pre and post ambles. The user can choose between synchronous and asynchronous wire-mode, asynchronous wire-mode performs RS232 start bit recognition and re-synchronization for transmit.

Both modes can be used both for transmit and receive. In both cases, the AX5043 behaves as a SPI slave interface. Configuration of the AX5043 is always done via the SPI interface.

The receiver and the transmitter support multi-channel operation for all data rates and modulation schemes.

5.1. Voltage Regulators

The **AX5043** uses an on-chip voltage regulator system to create stable supply voltages for the internal circuitry from the primary supply VDD_IO. The I/O level of the digital pins is VDD_IO.

Pins VDD_ANA are supplied for external decoupling of the power supply used for the on-chip PA.

The voltage regulator system must be set into the appropriate state before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the ***PWRMODE*** register.

Register ***POWSTAT*** contains status bits that can be read to check if the regulated voltages are ready (bit SVIO) or if VDD_IO has dropped below the brown-out level of 1.3V (bit SSUM).

In power-down mode the core supply voltages for digital and analog functions are switched off to minimize leakage power. Most register contents are preserved but access to the FIFO is not possible and FIFO contents are lost. SPI access to registers via SPI is possible, but at lower speed.

In deep-sleep mode all supply voltages are switched off. All digital and analog functions are disabled. All register contents are lost. To leave deep-sleep mode the pin SEL has to be pulled low. This will initiate startup and reset of the **AX5043**. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation.

5.2. Crystal Oscillator

The **AX5043** is normally operated with an external TCXO, which is required by most narrow-band regulation with a tolerance of 0.5 ppm to 1.5 ppm depending on the regulation. The on-chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference when regulatory and technical possible. The crystal oscillator circuit can handle a wide range of crystal frequencies, it is recommended to use 16 MHz as reference frequency since this choice allows all the typical SRD band RF frequencies to be generated with the internal VCO.

Programming the PWRMODE register enables the oscillator circuit. At power-up it is enabled.

To adjust the circuit's characteristics to the quartz crystal being used, without using additional external components, the tuning capacitance of the crystal oscillator can be programmed. The transconductance of the oscillator is automatically regulated, to allow for fastest start-up times together with lowest power operation during steady-state oscillation.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register ***XTALCAP***.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub-system together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TXCO, CXO) may be used. The CMOS levels should be applied to CLK16P via an AC coupling with the crystal oscillator enabled.

5.3. Low Power Oscillator and Wake on Radio (WOR) Mode

The **AX5043** features an internal lowest power fully integrated oscillator. In default-mode, the frequency of oscillation is 640 Hz +/- 3%, in fast mode it is 10.2 kHz +/- 3%.

The low power oscillator makes a WOR mode with a power consumption of 400nA possible.

If Wake on Radio Mode is enabled, the receiver wakes up periodically at a user selectable interval, and checks for a radio signal on the selected channel. If no signal is detected, the receiver shuts down again. If a radio signal is detected, and a valid packet is received, the micro-controller is alerted by asserting an interrupt.

The **AX5043** can thus autonomously poll for radio signals, while the micro-controller can stay powered down, and only wakes up once a valid packet is received. This allows for very low average receiver power, at the expense of longer preambles at the transmitter.

5.4. GPIO Pins

Pins DATA, DCLK, SYSCLK, IRQ, PWRAMP, ANTSEL can be used as general purpose I/O pins by programming pin configuration registers ***PINFUNCSYSCLK***, ***PINFUNCDCLK***, ***PINFUNCDATA***, ***PINFUNCIRQ***, ***PINFUCNANTSEL***, ***PINFUNCPWRAMP***. Pin input values can be read via register ***PINSTATE***. Pull-ups are disabled if output data is programmed to the GPIO pin

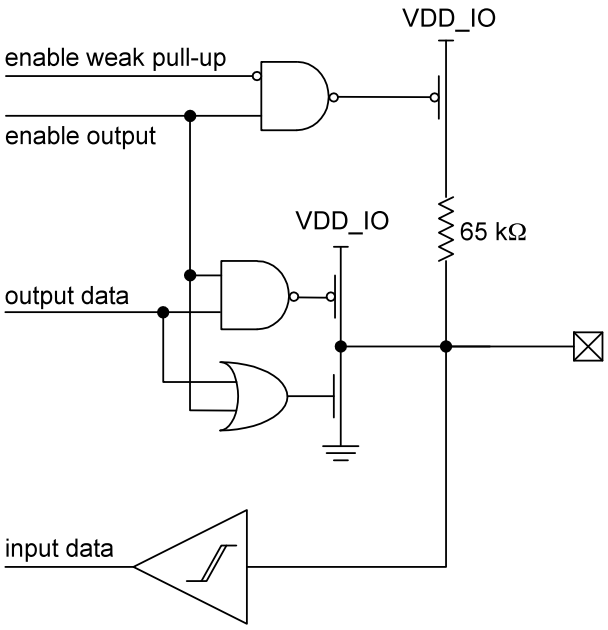


Figure 5 GPIO pin

5.5. SYSCLK Output

The SYSCLK pin outputs either the reference clock signal divided by a programmable integer or the low power oscillator clock. Divisions from 1 to 1024 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[4:0] in the ***PINFUNCSYSCLK*** register set the divider ratio. The SYSCLK output can be disabled.

After power-up SYSCLK outputs 1/16 of the crystal oscillator clock, making it possible to use this clock to boot a micro-controller.

5.6. Power-on-reset (POR)

AX5043 has an integrated power-on-reset block. No external POR circuit is required.

After POR, the **AX5043** can be reset by first setting the SPI SEL pin to high for at least 100ns, then setting followed by resetting the bit RST in the ***PWRMODE*** register.

After POR or reset all registers are set to their default values.

5.7. RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 µs depending on the settings (see section 4.3: AC Characteristics). Fast settling times mean fast start-up and fast RX/TX switching, this enables low-power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power-amplifier.

The frequency must be programmed to the desired carrier frequency.

The synthesizer loop-bandwidth can be programmed.

VCO

An on-chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the ***FREQ*** registers. For operation in the 433 MHz band, the REFDIV bit in the ***PLLVCODIV*** register must be programmed.

The fully integrated VCO allows operating the device in the frequency ranges 800 – 1040 MHz and 400 – 520 MHz.

The carrier frequency range can be extended to 140 – 800 MHz and 70 – 400 MHz by using an appropriate external inductor between device pins L1 and L2. The bit VCO2INT in the ***PLLVCODIV*** register must be set high to enter this mode. See the Synthesizer Application Note for details on how to set-up the synthesizer characteristics in this mode.

It is also possible to use a fully external VCO by setting bits VCO2INT=0 and VCOSEL=1 in the ***PLLVCODIV*** register. A differential input at a frequency of double the desired RF frequency must be input at device pins L1 and L2. The control voltage for the VCO can be output at device pin FILT when using external filter mode. The voltage range of this output pin is 0 – 1.8 V.
This mode of operation is recommended for special applications where the phase noise requirements are not met when using the fully internal VCO or the internal VCO with external inductor.

VCO Auto-Ranging

The **AX5043** has an integrated auto-ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power-up. The function is initiated by setting the RNG_START bit in the ***PLLRANGINGA*** or ***PLLRANGINGB*** register. The bit is readable and a 0 indicates the end of the ranging process. Setting RNG_START in the ***PLLRANGINGA*** register ranges the frequency in ***FREQA***, while setting RNG_START in the ***PLLRANGINGB*** register ranges the frequency in ***FREQB***. The RNGERR bit indicates the correct execution of the auto-ranging.

VCO auto-ranging works with the fully integrated VCO and with the internal VCO with external inductor.

Loop Filter and Charge Pump

The **AX5043** internal loop filter configuration together with the charge pump current sets the synthesizer loop bandwidth. The internal loop-filter has three configurations that can be programmed via the register bits FLT[1:0] in register ***PLLLOOP*** the charge pump current can be programmed using register bits PLLCPI[7:0]. Synthesizer bandwidths are typically 50 - 500 kHz..

Setting bits FLT[1:0]=00 bypasses the internal loop filter and the VCO control voltage is output to an external loop filter at pin FILT. This mode of operation is recommended for achieving lower bandwidths than with the internal loop filter and for usage with a fully external VCO.

5.8. RF Input and Output Stage (ANTP/ANTN/ANTP1)

The **AX5043** has two main antenna interface modes:

1. Both RX and TX use differential pins ANTP and ANTN. RX/TX switching is handled internally. This mode is recommended for highest output powers, highest sensitivities and for direct connection to dipole antennas.

2. RX uses the differential antenna pins ANTP and ANTN. TX uses the single ended antenna pin ANTP1. RX/TX switching is handled externally. This can be done either with an external RX/TX switch or with a direct tie configuration. This mode is recommended for low output powers at high efficiency and for usage with external power amplifiers.

Pin PWRAMP can be used to control an external RX/TX switch when operating the device together with an external PA. Pin ANTSEL can be used to control an external antenna switch when receiving with two antennas.

When antenna diversity is enabled, the radio controller will, when not in the middle of receiving a packet, periodically probe both antennas and select the antenna with the highest signal strength. The radio controller can be instructed to periodically write both RSSI values into the FIFO. Antenna diversity mode is fully automatic.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to GND must be provided at the antenna pins.

I/Q Mixer

The RF signal from the LNA is mixed down to a low IF which depends on the selected data rate.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to either the differential antenna terminals or to the single ended antenna pin. The antenna terminals are chosen via the bits TXDIFF and TXSE in register ***MODECFGA***.

The output power of the PA is programmed via the register ***TXPWRCOEFFB***.

The output amplitude can be shaped (raised cosine), this mode is selected with bit AMPLSHAPE in register ***MODECFGA.*** PA ramping is programmable in increments of the bit time and can be set to 1 – 8 bit times via bits SLOWRAMP in register ***MODECFGA.***

Output power as well as harmonic content will depend on the external impedance seen by the PA.

5.9. IF-Channel-Filter and Demodulator

The IF-channel-filter and the demodulator extract the data bit-stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data-rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 995 Hz up to 221 kHz. To calculate the optimal settings use the AXSEM **AX5043** configuration software.

5.10. Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit-stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received as either transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform spectral shaping (also know as whitening). Spectral shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self-synchronizing feedback shift register.

The encoder is programmed using the register ***ENCODING***. To calculate the optimal settings use the AXSEM **AX5043** configuration software.

5.11. Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit-stream suitable for the modulator, and to extract packets from the continuous bit-stream arriving from the demodulator.

The Framing unit supports two different modes:

- Packet modes
- Raw modes

The micro-controller communicates with the framing unit through a 256 byte FIFO. Data in the FIFO is organized in Chunks. The chunk header encodes the length and what data is contained in the payload. Chunks may contain packet data, but also RSSI, Frequency offset, Timestamps, etc.

The **AX5043** contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the micro-controller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. The **AX5043** signals interrupts by asserting (driving high) its IRQ line. The interrupt line is level triggered, active high. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Underrun, FIFO fill level above threshold, FIFO free space above threshold) are also provided during each SPI access on MISO while the micro- controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary during transmit and receive.

Packet Modes

The **AX5043** offers different packet modes. For arbitrary packet-sizes HDLC is recommended since the flag and bit-stuffing mechanism. The **AX5043** also offers packet modes with fixed packet length with a byte indicating the length of the packet.

In packet-modes a CRC can be computed automatically.

HDLC[1] Mode is the main framing mode of the **AX5043**. In this mode, the **AX5043** performs automatic packet-delimiting and optional packet-correctness-check by inserting and checking a cyclic redundancy check (CRC) field.

The packet structure is given in the following table.

Flag	Address	Control	Information	FCS	(Optional Flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In **AX5043** the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC-CCITT, CRC-16 or CRC-32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

To calculate the optimal settings for HDLC communication as well as Wireless M-Bus use the AXSEM **AX5043** configuration software.

[1] **Note:** HDLC mode follows High-Level Data Link Control (HDLC, ISO 13239) protocol.

RAW Modes

In Raw mode, the **AX5043** does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de-serializes the received bit-stream and groups it into bytes. This mode is ideal for implementing legacy protocols in software.

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit-stream. When it detects the preamble, it aligns the de-serialization to it.

The preamble can be between 4 and 32 bits long.

5.12. RX AGC and RSSI

The **AX5043** features a digital receiver signal strength indicator (RSSI). The RSSI can be read in the RSSI register and has a resolution of 1 dB steps.

5.13. Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bit-rate
ASK	PA off	PA on	BW=BIT-RATE	75 kBit/s
FSK/MSK/GFSK/GMSK	$\Delta f=-f_{deviation}$	$\Delta f=+f_{deviation}$	BW=(1+h) ·BIT-RATE	75 kBit/s
PSK	$\Delta\Phi=0^0$	$\Delta\Phi=180^0$	BW=BIT-RATE	75 kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit-rate; $f_{deviation}$ = 0.5·h·BIT-RATE, **AX5043** can demodulate signals with h < 32.

ASK = amplitude shift keying

FSK = frequency shift keying

MSK = minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation}$ = 0.25·BIT-RATE; the advantage of MSK over FSK is that it can be demodulated more robustly.

PSK = phase shift keying

OQPSK = offset quadrature shift keying. The **AX5043** supports OQPSK. However, unless compatibility to an existing system is required, MSK should be preferred.

All modulation schemes are binary.

Amplitude can be shaped using a raised cosine waveform.

Frequency shaping can either be hard (FSK, MSK), or Gaussian (GMSK, GFSK), with selectable BT=0.3 or BT=0.5.

5.14. Automatic Frequency Control (AFC)

The **AX5043** features an automatic frequency-tracking loop, which is capable of tracking the transmitter frequency within the RX-filter bandwidth. On top of that, the **AX5043** has a frequency tracking register ***TRKRFFREQ*** to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKRFFREQ}{2^{32}} f_{XTAL}.$$

5.15. Power-modes

The ***PWRMODE*** register controls, which parts of the chip are operating. Power-modes are the following:

Name	Description
POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltages are switched off to conserve leakage power. Register contents are preserved and accessible registers via SPI, but at a slower speed. Access to the FIFO is not possible and the contents are not preserved. POWERDOWN mode is only entered once the FIFO is empty.
DEEPSLEEP	**AX5043** is fully turned off. All digital and analog functions are disabled. All register contents are lost. To leave DEEPSLEEP mode the pin SEL has to be pulled low. This will initiate startup and reset of the **AX5043**. Then the MISO line should be polled, as it will be held low during initialization and will rise to high at the end of the initialization, when the chip becomes ready for operation.
STANDBY	The crystal oscillator and the reference are powered on; receiver and transmitter are off. Register contents are preserved and accessible registers via SPI. Access to the FIFO is not possible and the contents are not preserved. STANDBY is only entered once the FIFO is empty.
FIFO	The reference is powered on. Register contents are preserved and accessible registers via SPI. Access to the FIFO is possible and the contents are preserved.
SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.
FULLRX	Synthesizer and receiver are running.
WOR	Receiver wakeup-on-radio mode. The mode the same as powerdown, but the 640 Hz internal low power oscillator is running.
SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.
FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.

For the corresponding currents see table in section 4.2.

A typical ***PWRMODE*** sequence for a transmit session:

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	FULLTX	Data transmission
4	POWERDOWN	

A typical ***PWRMODE*** sequence for a receive session:

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms
3	FULLRX	Data reception
4	POWERDOWN	

5.16. Serial Peripheral Interface (SPI)

The **AX5043** can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the **AX5043** are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...Dx, A0...Ax, R_N/W. Data read from the interface appears on MISO.

Figure 6 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0], data D[7..0] can be written via MOSI or read at the pin MISO. R_N/W = 0 means read mode, R_N/W = 1 means write mode.

Most registers are 8 bits wide and accessed using the waveforms as detailed in Figure 7. The most important registers are at the beginning of the address space, i.e. at addresses less than 0x70. These registers can be accessed more efficiently using the short address form, which is detailed in Figure 6.

Some registers are longer than 8 bits. These registers can be accessed more quicly than by reading and writing individual 8 bit parts. This is illustrated in Figure 8. Accesses are not limited by 16 bits either, reading and writing data bytes can be continued as long as desired. After each byte, the address counter is incremented by one. Also, this access form works with long addresses.

During the address phase of the access, the **AX5043** outputs the most important status bits. This feature is designed to speed up the software decision on what to do in an interrupt handler.

The status bits contain the following information:

SPI bit cell	Status	Meaning / Register Bit
0	-	1 (when transitioning out of deep sleep mode, this bit transitions from 0 → 1 when the power becomes ready)
1	S14	PLL LOCK
2	S13	FIFO OVER
3	S12	FIFO UNDER
4	S11	FIFO FULL
5	S10	FIFO EMPTY
6	S9	FIFOSTAT(1)
7	S8	FIFOSTAT(0£)
8	S7	PWRGOOD (not BROWNOUT)
9	S6	PWR INTERRUPT PENDING
10	S5	RADIO EVENT PENDING
11	S4	XTAL OSCILLATOR RUNNING
12	S3	WAKEUP INTERRUPT PENDING
13	S2	LPOSC INTERRUPT PENDING
14	S1	GPADC INTERRUPT PENDING
15	S0	DSP INTERFACE INTERRUPT PENDING

Note: Bit cells 8-15 (S7...S0) are only available in two address byte SPI access formats.

SPI Timing

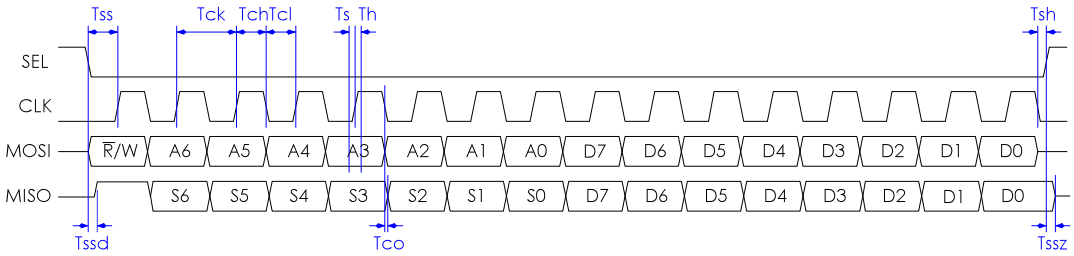


Figure 6 SPI 8 bit read/write access with timing

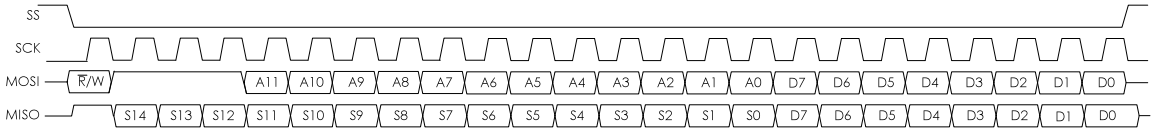


Figure 7 SPI 8 bit long address read/write access

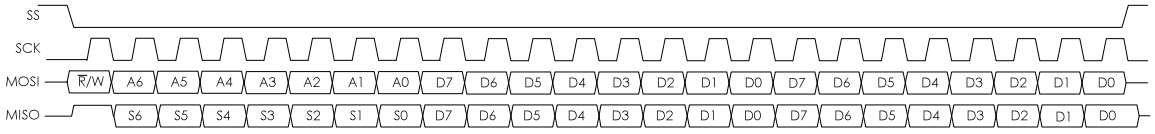


Figure 8 SPI 16 bit long read/write access

5.17. Wire-Mode Interface

In wire-mode the transmitted or received data are transferred from and to the **AX5043** using the pins DATA and DCLK. DATA is an input when transmitting and an output when receiving.

The direction can be chosen by programming the ***PWRMODE*** register.

Wire-mode offers two variants: synchronous or asynchronous.

In synchronous wire-mode the, the **AX5043** always drives DCLK. Transmit data must be applied to DATA synchronously to DCLK, and receive data must be sampled synchronously to DCLK. Timing is given in Figure 9. In asynchronous wire-mode, a low voltage RS232 type UART can be connected to DATA. DCLK is optional in this mode. The UART must be programmed to send two stop bits, but must be able to accept only one stop bit. Both the UART data rate and the **AX5043** transmit and receive bit rate must match. The **AX5043** synchronizes the RS232 signal to its internal transmission clock, by inserting or deleting a stop bit.

Wire-mode is also available in 4-FSK-mode. The two bits that encode one symbol are serialized on the DATA pin. The PWRAMP pin can be used as a synchronization pin to allow symbol (dibit) boundaries to be reconstructed. Gray coding is used to reduce the number of bit errors in case of a wrong decision.

Registers for setting up the **AX5043** are programmed via the serial peripheral interface (SPI).

Wire-Mode Timing

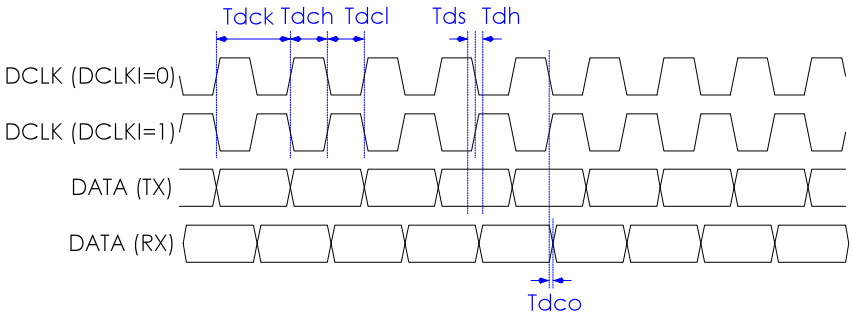


Figure 9 Wire-mode interface timing

General Purpose ADC (GPADC)

The **AX5043** features a general purpose ADC. The ADC input pins are GPADC1 and GPADC2. The ADC can be used either in differential (GPADC13) or single-ended mode (GPADC1 and GPADC2).

To start a single conversion, write 1 to the BUSY bit in the ***GPADCCTRL*** register. Then wait for the BUSY bit to clear, or the GPADC Interrupt to be asserted. Each channel, whose corresponding enable bit in register ***GPADCCTRL*** is set (GPADC13, GPADC1, GPADC2, GPADC3) is sampled in sequence. The results are stored in the corresponding result-registers. If CHISOL is set in register ***GPADCCTRL***, a dummy conversion with zero voltage is performed between each enabled channel. This may improve channel isolation at the expense of double the conversion time. The GPADC Interrupt is cleared by reading any result register. The GPADC can only be used if the receiver or transmitter are disabled.

If continuous sampling is desired, set the CONT bit in register ***GPADCCTRL***. The desired sampling rate can be specified in the ***GPADCPERIOD*** register.

6. Register Bank Description

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

An R in the retention column means that this register's contents are not lost during power-down mode.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

Note Whole registers or register bits marked as reserved should be kept at their default values.

Note All addresses not documented here must not be accessed, neither in reading nor in writing.

Note The retention column indicates if the register contents are preserved in power-down mode.

Note To calculate the optimal settings use the AXSEM AX5043 configuration software.

6.1. Control Register Map

Add	Name	Dir	Ret	Reset	Bit								Description
					7	6	5	4	3	2	1	0	
Revision & Interface Probing													
000	REVISION	R	R	00000110	SILICONREV(7:0)								Silicon Revision
001	SCRATCH	RW	R	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode													
002	PWRMODE	RW	R	011-0000	RST	REFEN	XOEN	-	PWRMODE(3:0)				Power Mode
Voltage Regulator													
003	POWSTAT	R	R	--------	SSUM	SREF	SVREF	SVANA	SVMODEM	SBEVANA	SBEVMODEM	SVIO	Power Management Status
004	POWSTICKYSTAT	R	R	--------	SSSUM	SREF	SSVREF	SSVANA	SSVMODEM	SSBEVANA	SSBEVMODEM	SSVIO	Power Management Sticky Status
005	POWIRQMASK	RW	R	00000000	MPWR GOOD	MSREF	MSVREF	MS VANA	MS VMODEM	MSBE VANA	MSBE VMODEM	MSVIO	Power Management Interrupt Mask
Interrupt Control													
006	IRQMASK1	RW	R	--000000	-	-	IRQMASK(13:8)						IRQ Mask
007	IRQMASK0	RW	R	00000000	IRQMASK(7:0)								IRQ Mask
008	RADIOEVENTMASK1	RW	R	-------0	-	-	-	-	-	-	-	RADIO EVENT MASK(8)	Radio Event Mask
009	RADIOEVENTMASK0	RW	R	00000000	RADIO EVENT MASK(7:0)								Radio Event Mask
00A	IRQINVERSION1	RW	R	--000000	-	-	IRQINVERSION(13:8)						IRQ Inversion
00B	IRQINVERSION0	RW	R	00000000	IRQINVERSION(7:0)								IRQ Inversion
00C	IRQREQUEST1	R	R	--------	-	-	IRQREQUEST(13:8)						IRQ Request
00D	IRQREQUEST0	R	R	--------	IRQREQUEST(7:0)								IRQ Request
00E	RADIOEVENTREQ1	R		--------	-	-	-	-	-	-	-	RADIO EVENT REQ(8)	Radio Event Request
00F	RADIOEVENTREQ0	R		--------	RADIO EVENT REQ(7:0)								Radio Event Request
Modulation & Framing													
010	MODULATION	RW	R	---01000	-	-	-	RX HALF SPEED	MODULATION(3:0)				Modulation

011	ENCODING	RW	R	---00010	-	-	-	ENC NOSYNC	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings
012	FRAMING	RW	R	-0000000	FRMRX	CRCMODE(2:0)			FRMMODE(2:0)			FABORT	Framing settings
014	CRCINIT3	RW	R	11111111	CRCINIT(31:24)								CRC Initialisation Data
015	CRCINIT2	RW	R	11111111	CRCINIT(23:16)								CRC Initialisation Data
016	CRCINIT1	RW	R	11111111	CRCINIT(15:8)								CRC Initialisation Data
017	CRCINIT0	RW	R	11111111	CRCINIT(7:0)								CRC Initialization Data
Forward Error Correction													
018	FEC	RW	R	00000000	SHORT MEM	RSTVI TERBI	FEC NEG	FEC POS	FECINPSHIFT(2:0)			FEC ENA	FEC (Viterbi) Configuration
019	FECSYNC	RW	R	01100010	FECSYNC(7:0)								Interleaver Synchronization Threshold
01A	FECSTATUS	R	R	--------	FEC INV	MAXMETRIC(6:0)							FEC Status
Status													
01C	RADIOSTATE	R	-	----0000	-	-	-	-	RADIOSTATE(3:0)				Radio Controller State
Pin Configuration													
020	PINSTATE	R	R	--------	-	-	PS PWR AMP	PS ANT SEL	PS IRQ	PS DATA	PS DCLK	PS SYS CLK	Pin-state
021	PINFUNCSYSCLK	RW	R	0--01000	PU SYSCLK	-	-	PFSYSCLK(4:0)					SYSCLK Pin Function
022	PINFUNCDCLK	RW	R	0----100	PU DCLK	-	-	-	-	PFDCLK(2:0)			DCLK Pin Function
023	PINFUNCDATA	RW	R	1----111	PU DATA	-	-	-	-	PFDATA(2:0)			DATA Pin Function
024	PINFUNCIRQ	RW	R	0----011	PU IRQ	-	-	-	-	PFIRQ(2:0)			IRQ Pin Function
025	PINFUNCANTSEL	RW	R	0----110	PU ANTSEL	-	-	-	-	PFANTSEL(2:0)			ANTSEL Pin Function
026	PINFUNCPWRAMP	RW	R	0---0110	PU PWRAMP	-	-	-	PFPWRAMP(3:0)				PWRAMP Pin Function
027	PWRAMP	RW	R	-------0	-	-	-	-	-	-	-	PWRAMP	PWRAMP Control
FIFO													
028	FIFOSTAT	R	R	0-------	FIFO AUTO COMMIT	-	FIFO FREE THR	FIFO CNT THR	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFO Control
		W	R				FIFOCMD(5:0)						
029	FIFODATA	RW		--------	FIFODATA(7:0)								FIFO Data
02A	FIFOCOUNT1	R	R	-------0	-	-	-	-	-	-	-	FIFO COUNT(8)	Number of Words currently in FIFO

02B	FIFOCOUNT0	R	R	00000000	FIFOCOUNT(7:0)									Number of Words currently in FIFO
02C	FIFOFREE1	R	R	-------1	-	-	-	-	-	-	-	FIFO FREE(8)		Number of Words that can be written to FIFO
02D	FIFOFREE0	R	R	00000000	FIFOFREE(7:0)									Number of Words that can be written to FIFO
02E	FIFOTHRESH1	RW	R	-------0	-	-	-	-	-	-	-	FIFO THRESH(8)		FIFO Threshold
02F	FIFOTHRESH0	RW	R	00000000	FIFOTHRESH(7:0)									FIFO Threshold
Synthesizer														
030	PLLLOOP	RW	R	0---1001	FREQB	-	-	-	-	FILT EN	FLT(1:0)			PLL Loop Filter Settings
031	PLLCPI	RW	R	00001000	PLLCPI									PLL Charge Pump Current (Boosted)
032	PLLVCODIV	RW	R	-000-000	-	-	VCO2INT	VCOSEL	-	RFDIV	REFDIV(1:0)			PLL Divider Settings
033	PLLRANGINGA	RW	R	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCORA(3:0)					PLL Auto-ranging
034	FREQA3	RW	R	00111001	FREQA(31:24)									Synthesizer Frequency
035	FREQA2	RW	R	00110100	FREQA(23:16)									Synthesizer Frequency
036	FREQA1	RW	R	11001100	FREQA(15:8)									Synthesizer Frequency
037	FREQA0	RW	R	11001101	FREQA(7:0)									Synthesizer Frequency
038	PLLLOOPBOOST	RW	R	0---1011	FREQB	-	-	-	-	FILT EN	FLT(1:0)			PLL Loop Filter Settings (Boosted)
039	PLLCPIBOOST	RW	R	11001000	PLLCPI									PLL Charge Pump Current
03B	PLLRANGINGB	RW	R	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCORB(3:0)					PLL Auto-ranging
03C	FREQB3	RW	R	00111001	FREQB(31:24)									Synthesizer Frequency
03D	FREQB2	RW	R	00110100	FREQB(23:16)									Synthesizer Frequency
03E	FREQB1	RW	R	11001100	FREQB(15:8)									Synthesizer Frequency
03F	FREQB0	RW	R	11001101	FREQB(7:0)									Synthesizer Frequency
Signal Strength														
040	RSSI	R	R	--------	RSSI(7:0)									Received Signal Strength Indicator
041	BGNDRSSI	RW	R	00000000	BGNDRSSI(7:0)									Background RSSI
042	DIVERSITY	RW	R	------00	-	-	-	-	-	-	ANT SEL	DIV ENA		Antenna Diversity Configuration
Receiver Tracking														
050	TRKFREQ1	RW	R	--------	TRKFREQ(15:8)									Frequency Tracking

051	TRKFREQ0	RW	R	--------	TRKFREQ(7:0)									Frequency Tracking
Timer														
059	TIMER2	R	-	--------	TIMER(23:16)									1MHz Timer
05A	TIMER1	R	-	--------	TIMER(15:8)									1MHz Timer
05B	TIMER0	R	-	--------	TIMER(7:0)									1MHz Timer
Wakeup Timer														
068	WAKEUPTIMER1	R	R	--------	WAKEUPTIMER(15:8)									Wake-up Timer
069	WAKEUPTIMER0	R	R	--------	WAKEUPTIMER(7:0)									Wake-up Timer
06A	WAKEUP1	RW	R	00000000	WAKEUP(15:8)									Wakeup Time
06B	WAKEUP0	RW	R	00000000	WAKEUP(7:0)									Wakeup Time
06C	WAKEUPFREQ1	RW	R	00000000	WAKEUPFREQ(15:8)									Wakeup Frequency
06D	WAKEUPFREQ0	RW	R	00000000	WAKEUPFREQ(7:0)									Wakeup Frequency
06E	WAKEUPXOEARLY	RW	R	00000000	WAKEUPXOEARLY									Wakeup Crystal Oscillator Early
Physical Layer Parameters														
Receiver Parameters														
100	IFFREQ1	RW	R	00011001	IFFREQ(15:8)									2nd LO / IF Frequency
101	IFFREQ0	RW	R	10011010	IFFREQ(7:0)									2nd LO / IF Frequency
102	DECIMATION	RW	R	-0001101	-	DECIMATION(6:0)								Decimation Factor
103	RXDATARATE2	RW	R	00000000	RXDATARATE(23:16)									Receiver Data-rate
104	RXDATARATE1	RW	R	00111101	RXDATARATE(15:8)									Receiver Data-rate
105	RXDATARATE0	RW	R	10001010	RXDATARATE(7:0)									Receiver Data-rate
117	RXPARAMCURSET	R	R	--------	-	-	-	RXSI(2)	RXSN(1:0)		RXSI(1:0)			Receiver Parameter Current Set
Transmitter Parameters														
160	MODCFGF	RW	R	------00	-	-	-	-	-	-	FREQ SHAPE			Modulator Configuration F
161	FSKDEV2	RW	R	00000000	FSKDEV(23:16)									FSK Frequency Deviation
162	FSKDEV1	RW	R	00001010	FSKDEV(15:8)									FSK Frequency Deviation
163	FSKDEV0	RW	R	00111101	FSKDEV(7:0)									FSK Frequency Deviation
164	MODCFGA	RW	R	0000-101	BROWN GATE	PTTLCKG	SLOW RAMP		-	AMPL SHAPE	TX SE	TX DIFF		Modulator Configuration A
165	TXRATE2	RW	R	00000000	TXRATE(23:16)									Transmitter Bit-rate

166	TXRATE1	RW	R	00101000	TXRATE(15:8)							Transmitter Bit-rate
167	TXRATE0	RW	R	11110110	TXRATE(7:0)							Transmitter Bit-rate
16A	TXPWRCOEFFB1	RW	R	00001111	TXPWRCOEFFB(15:8)							Transmitter Output Power
16B	TXPWRCOEFFB0	RW	R	11111111	TXPWRCOEFFB(7:0)							Transmitter Output Power
PLL Parameters												
182	PLLLOCKDET	RW	R	-----011	LOCKDETDLYR	–	–	–	LOCK DET DLYM	LOCKDETDLY		PLL Lock Detect Delay
Crystal Oscillator												
184	XTALCAP	RW	R	00000000	XTALCAP(7:0)							Crystal Oscillator Load Capacitance
MAC Layer Parameters												
Packet Format												
201	PKTADDRCFG	RW	R	001–0000	MSB FIRST	CRC SKIP FIRST	FEC SYNC DIS	–	ADDR POS(3:0)			Packet Address Configuration
202	PKTADDR1	RW	R	00000000	ADDR(15:8)							Packet Address 1
203	PKTADDR0	RW	R	00000000	ADDR(7:0)							Packet Address 0
204	PKTADDRMASK1	RW	R	00000000	ADDRMASK(15:8)							Packet Address Mask 1
205	PKTADDRMASK0	RW	R	00000000	ADDRMASK(7:0)							Packet Address Mask 0
206	PKTLENCFG	RW	R	00000000	LEN BITS(3:0)				LEN POS(3:0)			Packet Length Configuration
207	PKTLENOFFSET	RW	R	00000000	LEN OFFSET(7:0)							Packet Length Offset
208	PKTMAXLEN	RW	R	00000000	MAX LEN(7:0)							Packet Maximum Length
Pattern Match												
210	MATCH0PAT3	RW	R	00000000	MATCH0PAT(31:24)							Pattern Match Unit 0, Pattern
211	MATCH0PAT2	RW	R	00000000	MATCH0PAT(23:16)							Pattern Match Unit 0, Pattern
212	MATCH0PAT1	RW	R	00000000	MATCH0PAT(15:8)							Pattern Match Unit 0, Pattern
213	MATCH0PAT0	RW	R	00000000	MATCH0PAT(7:0)							Pattern Match Unit 0, Pattern
214	MATCH0LEN	RW	R	0–-00000	MATCH0 RAW	–	–	MATCH0LEN				Pattern Match Unit 0, Pattern Length
215	MATCH0MIN	RW	R	---00000	–	–	–	MATCH0MIN				Pattern Match Unit 0, Minimum Match
216	MATCH0MAX	RW	R	---11111	–	–	–	MATCH0MAX				Pattern Match Unit 0, Maximum Match
218	MATCH1PAT1	RW	R	00000000	MATCH1PAT(15:8)							Pattern Match Unit 1, Pattern
219	MATCH1PAT0	RW	R	00000000	MATCH1PAT(7:0)							Pattern Match Unit 1, Pattern

21C	MATCH1LEN	RW	R	0---0000	MATCH1 RAW	-	-	-	MATCH1LEN				Pattern Match Unit 1, Pattern Length
21D	MATCH1MIN	RW	R	----0000	-	-	-	-	MATCH1MIN				Pattern Match Unit 1, Minimum Match
21E	MATCH1MAX	RW	R	----1111	-	-	-	-	MATCH1MAX				Pattern Match Unit 1, Maximum Match
Packet Controller													
230	PKTCHUNKSIZE	RW	R	----0000	-	-	-	-	PKTCHUNKSIZE(3:0)				Packet Chunk Size
231	PKTMISCFLAGS	RW	R	----0000	-	-	-	WOR MULTI PKT	AGC SETTL DET	BGND RSSI	RXAGC CLK	RXRSSI CLK	Packet Controller Miscellaneous Flags
232	PKTSTOREFLAGS	RW	R	-0000000	-	ST ANT RSSI	ST CRCB	ST RSSI	ST DR	ST RFOFFS	ST FOFFS	ST TIMER	Packet Controller Store Flags
233	PKTACCEPTFLAGS	RW	R	--000000	-	-	ACCPT LRGP	ACCPT SZF	ACCPT ADDRF	ACCPT CRCF	ACCPT ABRT	ACCPT RESIDUE	Packet Controller Accept Flags
Special Functions													
General Purpose ADC													
300	GPADCCTRL	RW	R	--000000	BUSY	-	GPADC3	GPADC2	GPADC1	GPADC13	CONT	CH ISOL	General Purpose ADC Control
301	GPADCPERIOD	RW	R	00111111	GPADCPERIOD(7:0)								GPADC Sampling Period
308	GPADC13VALUE1	R		--------	-	-	-	-	-	-	GPADC13VALUE(9:8)		GPADC13 Value
309	GPADC13VALUE0	R		--------	GPADC13VALUE(7:0)								GPADC13 Value
30A	GPADC1VALUE1	R		--------	-	-	-	-	-	-	GPADC1VALUE(9:8)		GPADC1 Value
30B	GPADC1VALUE0	R		--------	GPADC1VALUE(7:0)								GPADC1 Value
30C	GPADC2VALUE1	R		--------	-	-	-	-	-	-	GPADC2VALUE(9:8)		GPADC2 Value
30D	GPADC2VALUE0	R		--------	GPADC2VALUE(7:0)								GPADC2 Value
30E	GPADC3VALUE1	R		--------	-	-	-	-	-	-	GPADC3VALUE(9:8)		GPADC3 Value
30F	GPADC3VALUE0	R		--------	GPADC3VALUE(7:0)								GPADC3 Value
Low Power Oscillator Calibration													
310	LPOSCCONFIG	RW		00000000	LPOSC OSC INVERT	LPOSC OSC DOUBLE	LPOSC CALIBR	LPOSC CALIBF	LPOSC IRQR	LPOSC IRQF	LPOSC FAST	LPOSC ENA	Low Power Oscillator Configuration
312	LPOSCKFILT1	RW		00100000	LPOSCKFILT(15:8)								Low Power Oscillator Calibration Filter Constant
313	LPOSCKFILT0	RW		11000100	LPOSCKFILT(7:0)								Low Power Oscillator Calibration Filter Constant
314	LPOSCREF1	RW		01100001	LPOSCREF(15:8)								Low Power Oscillator Calibration Reference

315	LPOSCREF0	RW		10101000	LPOSCREF(7:0)						Low Power Oscillator Calibration Reference
316	LPOSCFREQ1	RW		00000000	LPOSCFREQ(9:2)						Low Power Oscillator Calibration Frequency
317	LPOSCFREQ0	RW		0000----	LPOSCFREQ(1:-2)	-	-	-	-		Low Power Oscillator Calibration Frequency
318	LPOSCPER1	RW		--------	LPOSCPER(15:8)						Low Power Oscillator Calibration Period
319	LPOSCPER0	RW		--------	LPOSCPER(7:0)						Low Power Oscillator Calibration Period

7. Application Information

7.1. Typical Application Diagrams

Using a Dipole Antenna and the internal TX/RX Switch

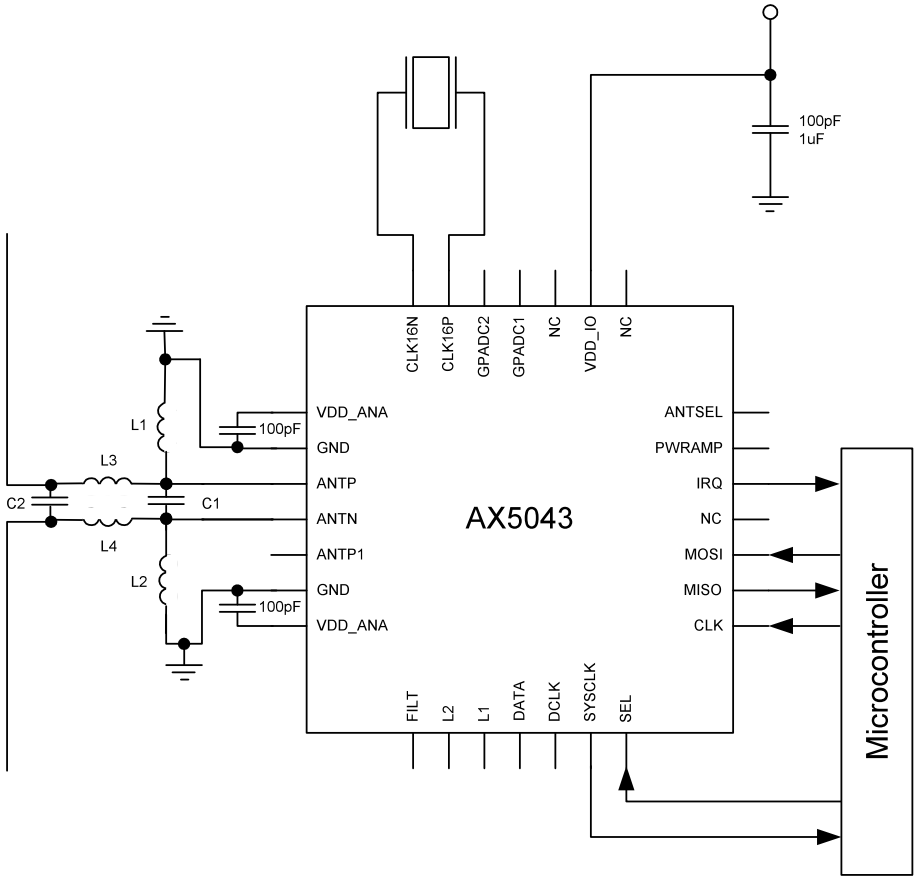


Figure 10 Application diagram: Dipole antenna and internal TX/RX switch

Using a single-ended Antenna and the internal TX/RX Switch

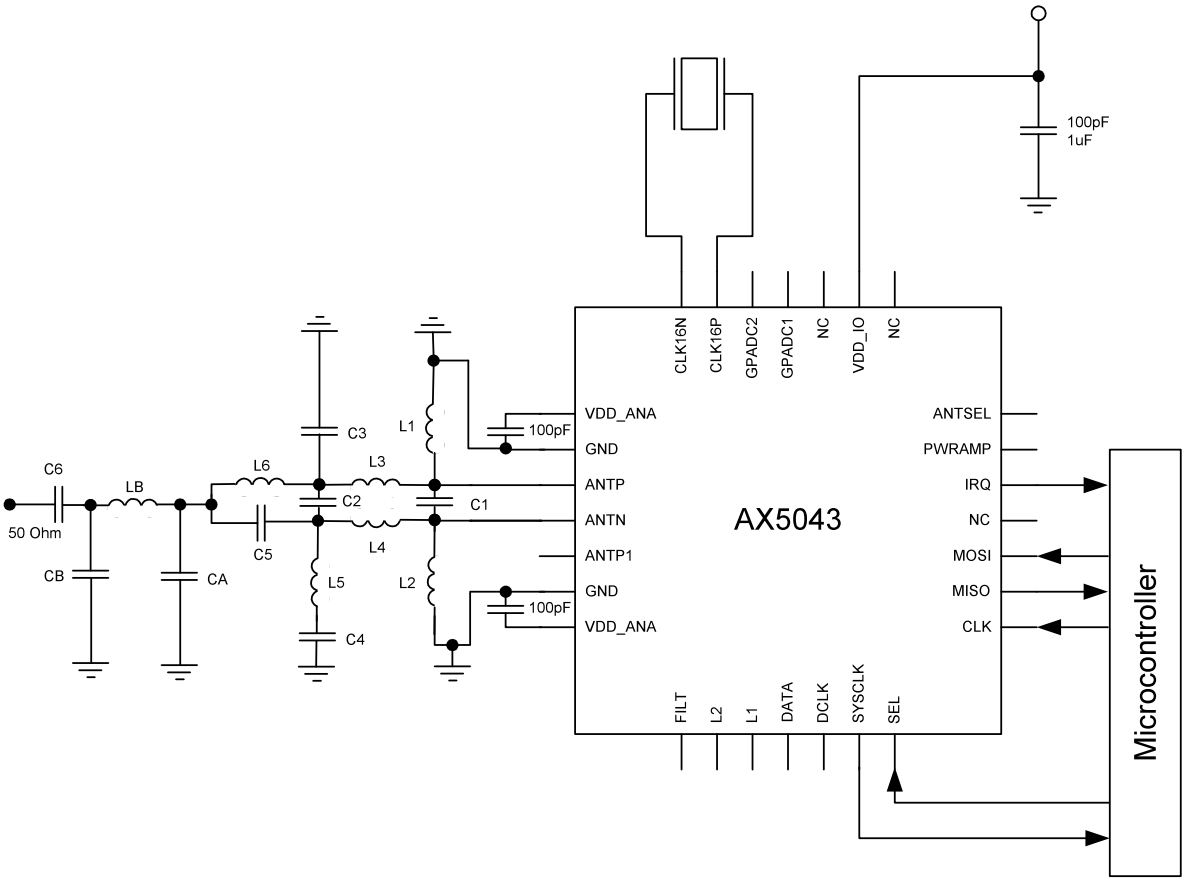


Figure 11 Application diagram: Single-ended antenna and internal TX/RX switch

Using an external high-power PA and an external TX/RX Switch

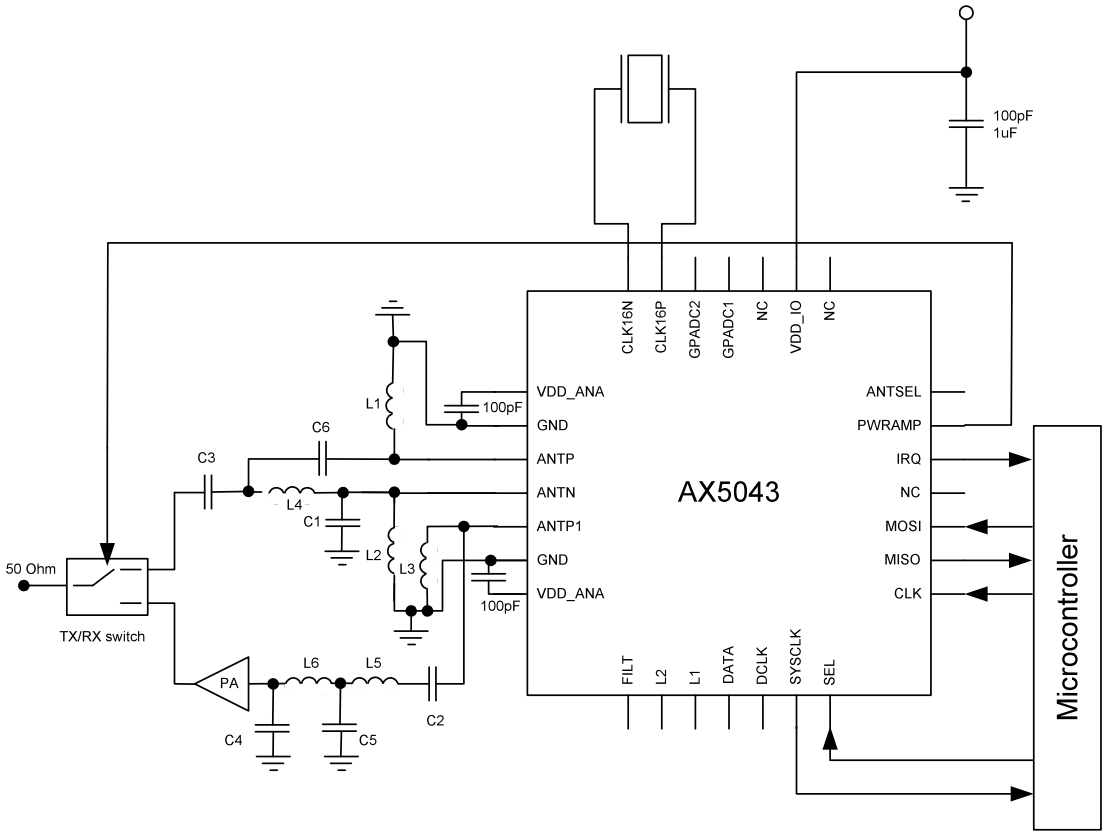


Figure 12 Application diagram: Single-ended antenna, external PA and external antenna switch

Using the single-ended PA

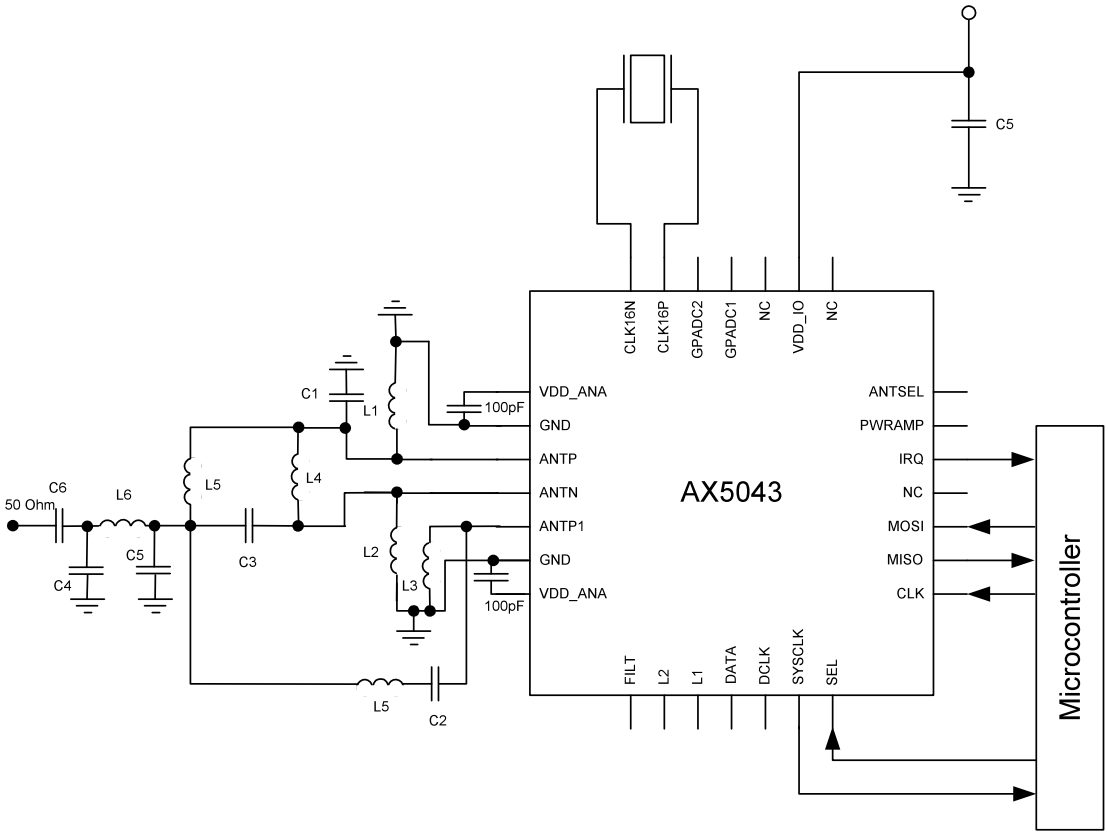


Figure 13 Application diagram: Single-ended antenna, single ended internal PA, without RX/TX switch

Using two Antenna

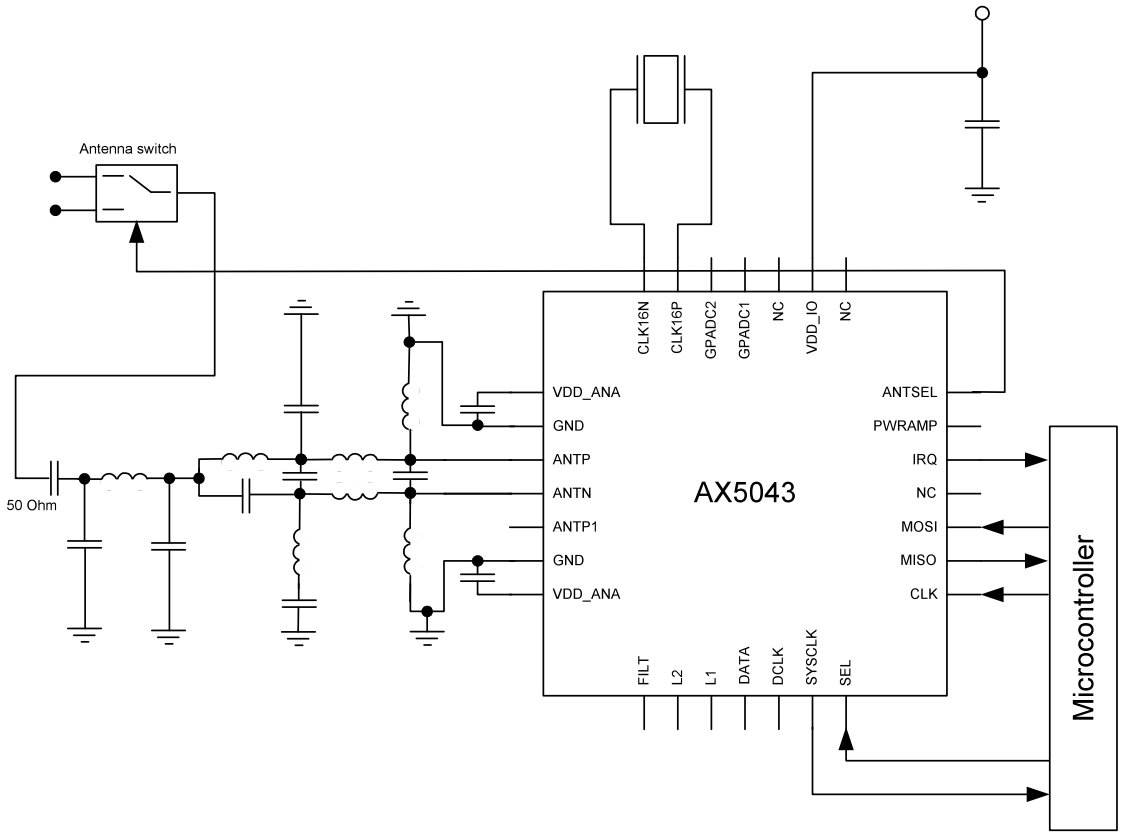


Figure 14 Application diagram: Two single-ended antenna and external antenna switch

Using an external VCO inductor

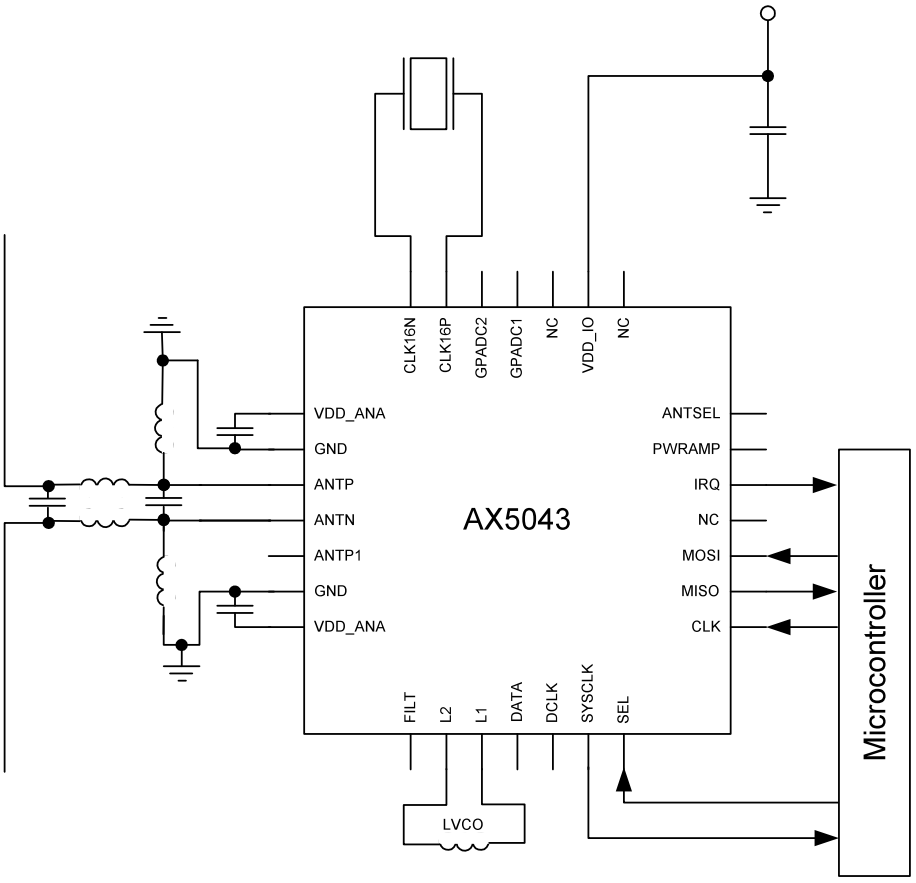


Figure 15 Application diagram: External VCO inductor

Using an external VCO

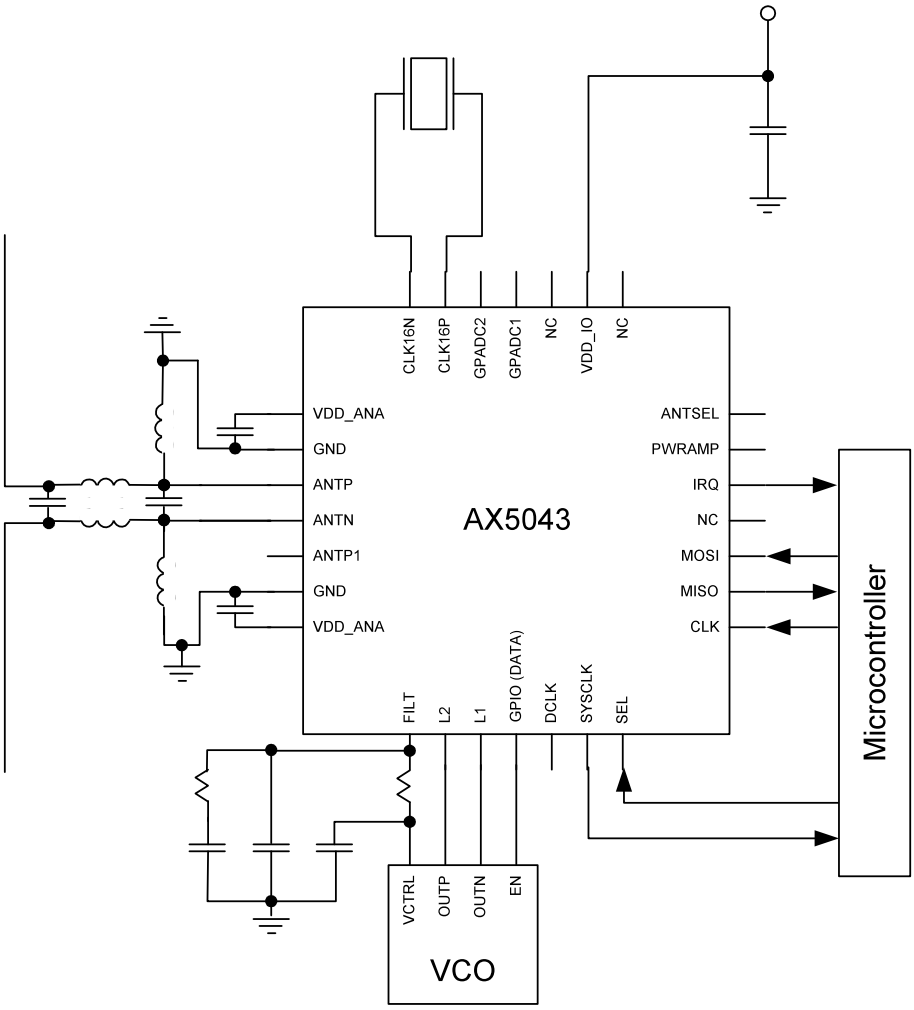


Figure 16 Application diagram: External VCO

Using a TCXO

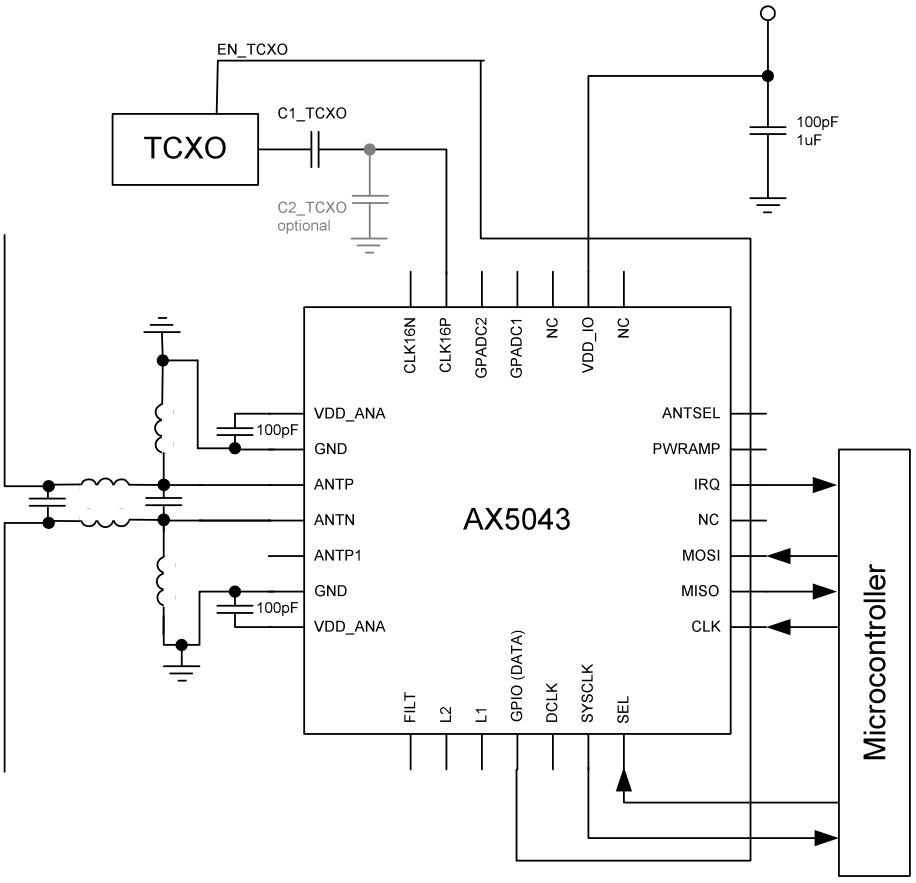
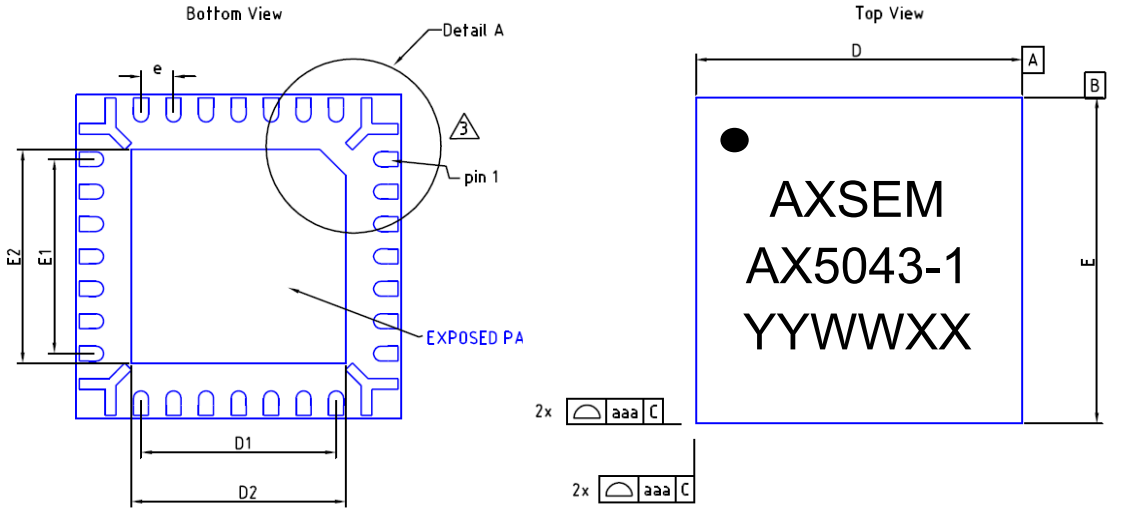


Figure 17 Application diagram: Usage with TCXO

8. QFN28 Package Information

8.1. Package Outline QFN28



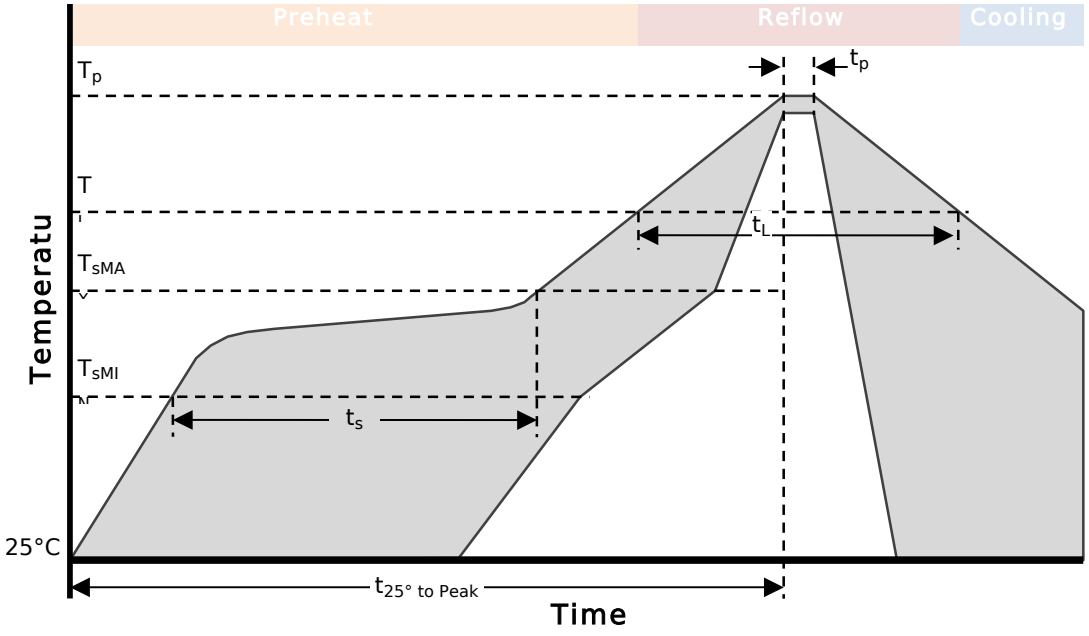
Sym.	Tolerances for Form & Position	Notes
aaa	0.15	
bbb	0.10	
ccc	0.10	

Notes

1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 is identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represent the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. There terminal pull back esists, only upper half of lead is visible on package edge du to half etching of leadframe.
8. Package warp shall be 0.050 maximum
9. Leadframe material is copper A194
10. Coplanarity applies to the exposed pad as well as the terminal
11. YYWWXX is the packaging lot code
12. RoHS compliant

Common Dimensions			
Sym.	Minimum	Nominal	Maximum
A	0.85	0.90	1.0
A1	0	0.02	0.05
A3		0.20 ref	
D	4.90	5.0	5.10
D1		3.00	
D2	3.20	3.30	3.40
E	4.90	5.0	5.10
E1		3.0	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
L1			0.1
b	0.18	0.23	0.30
N		28	
e		0.50	
k	0.20		
R	b min / 2		
T		0.15	

8.2. QFN28 Soldering Profile



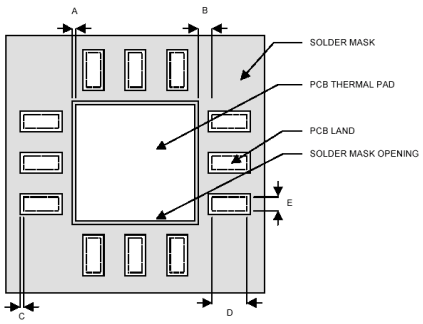
Profile Feature		Pb-Free Process
Average Ramp-Up Rate		3 °C/sec max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25\ ^\circ\ to\ Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 sec
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 sec
Cooling Phase		
Ramp-down rate		6°C/sec max.

Notes:

All temperatures refer to the top side of the package, measured on the package body surface.

8.3. QFN28 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 18.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads
D = PCB land length = QFN solder pad length + 0.1mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 18: PCB land and solder mask recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

8.4. Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 19.
4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 20.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

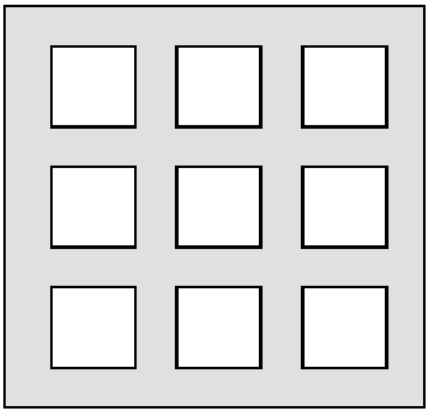


Figure 19: Solder paste application on exposed pad

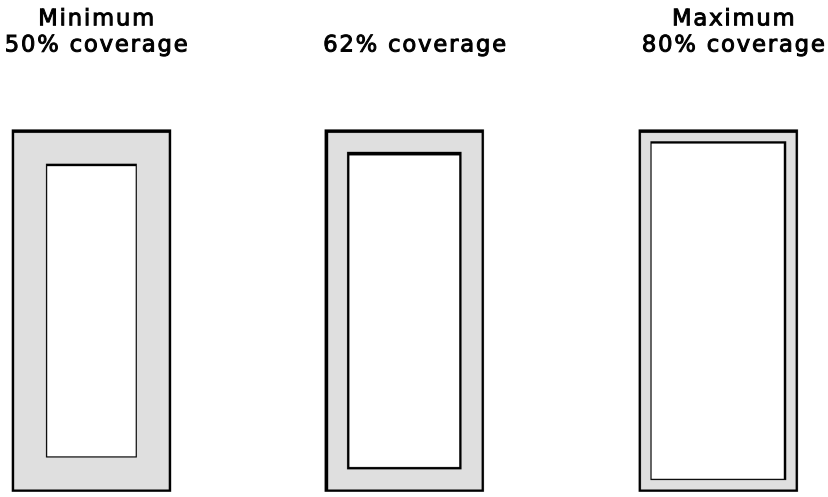


Figure 20: Solder paste application on pins

9. Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. AXSEM customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify AXSEM for any damages resulting from such improper use or sale.

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