Future Technology Devices International Ltd.

Vinculum VNC1L

Embedded USB Host Controller IC

Datasheet

VINCULUM

The VNC1L is a single chip embedded dual USB host controller with the following advanced features:

- Two independent USB 2.0 Low-speed/Full-speed USB host ports.
- Individual ports can be configured as host or slave.
- Configurable options to interface to external Command Monitor via either UART, FIFO or SPI slave interface.
- Entire USB protocol handled on the chip.
- Integrated pull-up and pull-down resistors.
- Integrated FTDI proprietary, 8/32-bit embedded MCU processor core -Vinculum MCU (VMCU) - using "enhanced CISC" technology.
- Integrated, reconfigurable, 64k bytes of embedded Flash (E-FLASH) memory to store firmware. 4k bytes data RAM.
- Field upgradeable firmware over UART or USB.
- Integrated Numeric Co-Processor (NCP) enhances 32 bit arithmetic speeds.
- Twin DMA controllers (one per USB interface) provide hardware acceleration of data transfer from USB to external IO bus.
- Operational configuration via a choice of free, downloadable firmware – no external software control required.
- Four fully configurable data and control I/O buses providing up to 28 pins of general purpose I/O.
- Integrated firmware allows read from and write to FAT format USB Flash keys.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- Programmable via UART interface.
- +3.3V single supply operation with 5V safe inputs.
- Low power operation (25mA operational, 2mA in standby).
- -40°C to +85°C extended operating temperature range.
- Available in compact Pb-free 48 Pin LQFP package (RoHS compliant).

1 Typical Applications

- Add USB host capability to embedded products.
- Interface USB Flash drive to MCU/PLD/FPGA.
- USB Flash drive to USB Flash drive file transfer interface.
- Digital camera to USB Flash drive or other USB slave device interface.
- PDA to USB Flash driver or other USB slave device interface.
- MP3 Player to USB Flash drive or other USB slave device interface.
- USB MP3 Player to USB MP3 Player.
- Mobile phone to USB Flash drive or other USB slave device interface.
- GPS to mobile phone interface.
- Instrumentation USB Flash drive or other USB slave device interfacing.
- Data-logger USB Flash drive or other USB slave device interface.
- Set Top Box - USB device interface.
- GPS tracker with USB Flash disk storage.

1.1 Firmware Support and VNC1L Programming

There are currently 6 standard firmware versions available for VNC1L:

- VDAP Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. Selectable UART, FIFO or SPI interface command monitor.
- VDPS Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. USB Slave port connection for connecting to host PC. Selectable UART, FIFO or SPI interface command monitor.
- VDFC Firmware: USB Host for two Flash Disks, Selectable UART, FIFO or SPI interface command monitor.
- VMSC1 Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. Audio playback command extensions for VLSI VS1003 series MP3 decoder ICs. Selectable UART, FIFO or SPI interface command monitor port.
- VCDC Firmware: USB Host for automatic connection to USB Communications Class Devices. UART interface command monitor.
- VDIF Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. Selectable UART, FIFO, SPI or USB interface command monitor.

General Purpose USB peripherals include Printers, Communication Class Devices, Human Interface Devices, FTDI USB Serial Devices, and USB Hubs. USB peripherals can be accessed using command monitor commands to send SETUP, DATA IN and DATA OUT packets. Flash Disk firmware supports FAT12, FAT16 and FAT32 file systems with a simple file oriented command set.

1.2 Part Numbers

Part Number	Package
VNC1L-1A	48 Pin LQFP

1.3 Programming VNC1L

1. The VNC1L is shipped as a blank device. Initial in-circuit programming (using the downloaded .rom firmware file) can **only** be done via the UART interface. (Refer to section 4.3)
2. When upgrading VNC1L in-situ, then the device can be programmed via the UART interface (.rom file). Alternatively, it can be upgraded via a USB Flash disk using a file called "ftrfb.ftd". Both file

types can be downloaded from the FTDI website. Any firmware downloaded from the FTDI website should be changed to match this filename.

3. VNC1L devices can also be programmed before being assembled in a system using the VPROG1 VNC1L stand alone programmer – see (www.ftdichip.com)

2 VNC1L Block Diagram

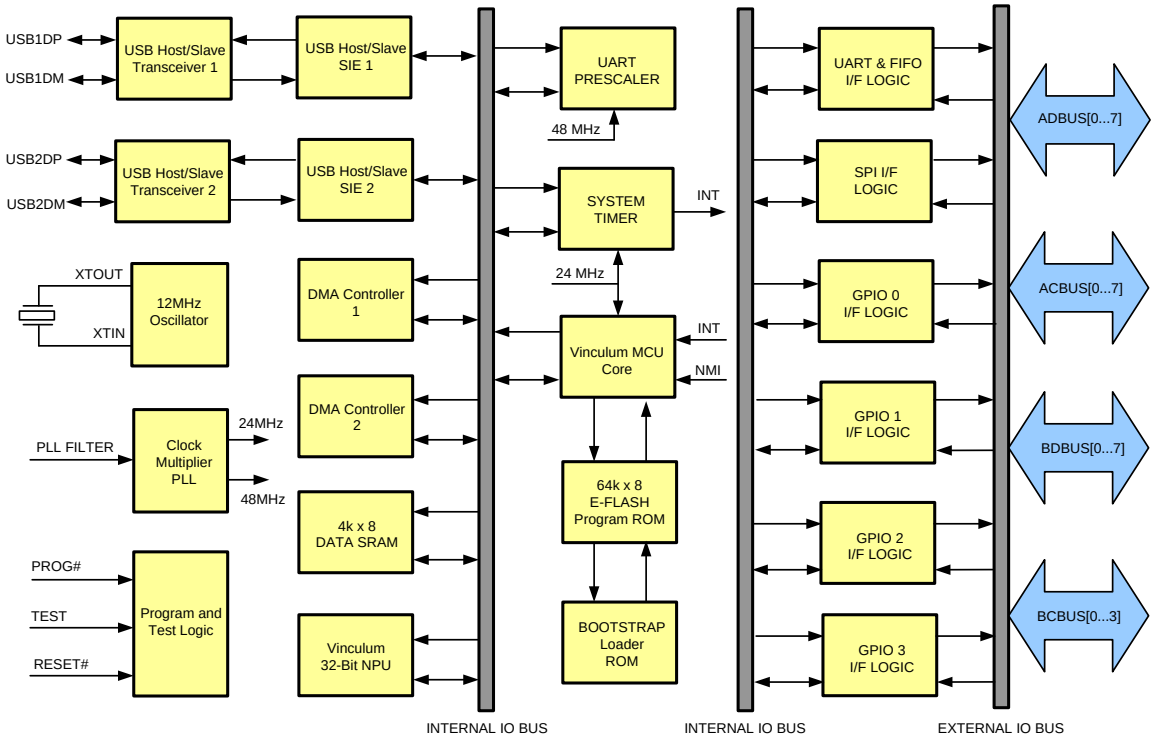

Figure 2.1 Simplified VNC1L Block Diagram

For a functional description of each block, please refer to Section 4.2

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3 Device Pin Out and Signal Description

3.1 48 Lead LQFP Pin Out

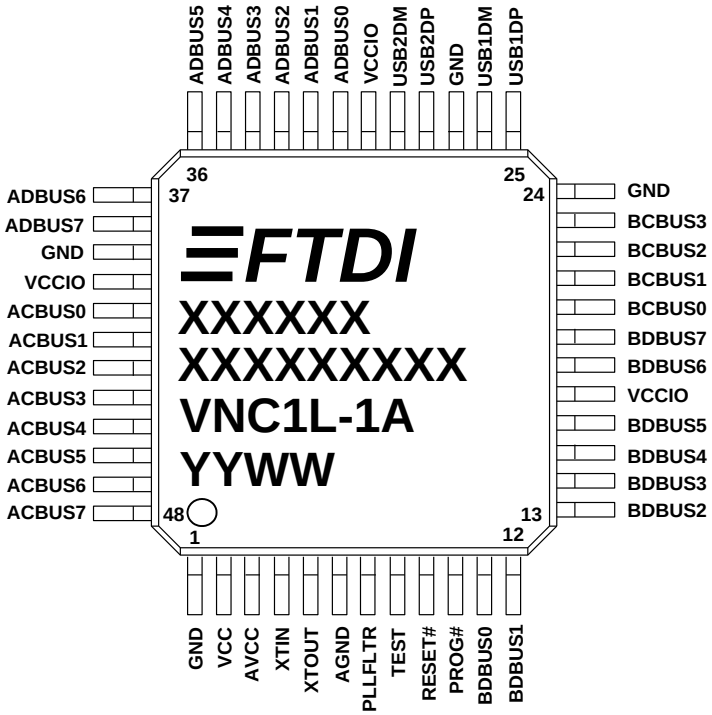

Figure 3.1 48 Lead LQFP Package Pin Out

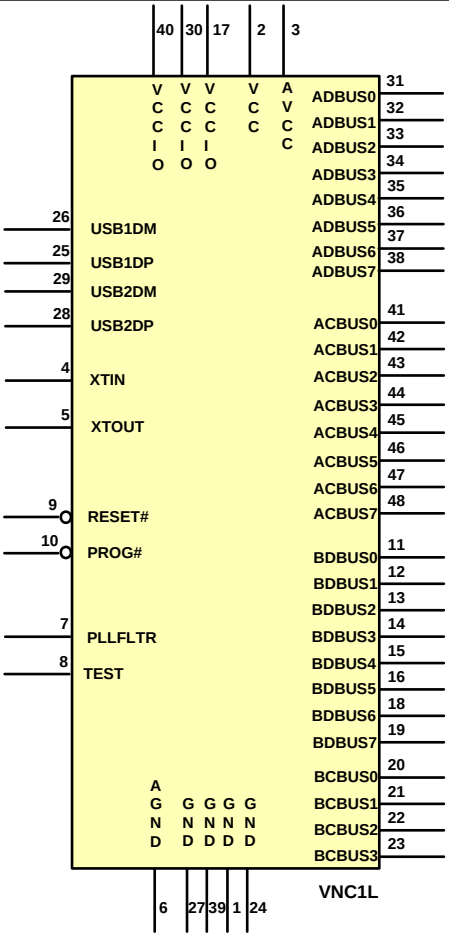

Figure 3.2 VNC1L – Schematic Symbol

3.2 48 Lead LQFP Package Pin Descriptions

Pin No.	Name	Type	Description
25	USB1DP	I/O	USB host/slave port 1 - USB Data Signal Plus with integrated pull-up/pull-down resistor
26	USB1DM	I/O	USB host/slave port 1 - USB Data Signal Minus with integrated pull-up/pull-down resistor
28	USB2DP	I/O	USB host/slave port 2 - USB Data Signal Plus with integrated pull-up/pull-down resistor
29	USB2DM	I/O	USB host/slave port 2 - USB Data Signal Minus with integrated pull-up/pull-down resistor

Table 3.1 USB Interface Group

Pin No.	Name	Type	Description
1, 24, 27, 39	GND	PWR	Device ground supply pins
2	VCC	PWR	+3.3V supply to the device core

Pin No.	Name	Type	Description
3	AVCC	PWR	+3.3V supply to the internal clock multiplier. This pin requires a 100nF decoupling capacitor
6	AGND	PWR	Device analogue ground supply for internal clock multiplier
17, 30, 40	VCCIO	PWR	+3.3V supply to the ADBUS, ACBUS, BDBUS and BCBUS Interface pins (11..16, 18..23, 31..38, 41..48). Leaving the VCCIO unconnected will lead to unpredictable operation on these interface pins.

Table 3.2 Power and Ground Group

Pin No.	Name	Type	Description
4	XTIN	Input	Input to 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5, with suitable loading capacitors to GND. This pin can also be driven by an external 12MHz clock signal. Note that the switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at +3.3V CMOS level or AC coupled to centre around VCC/2
5	XTOUT	Output	Output from 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5, with suitable loading capacitors to GND. XTOUT stops oscillating during USB suspend, so take care using this signal to clock external logic
7	PLLFLTR	Input	External PLL filter circuit input. RC filter circuit must be fitted on this pin
8	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation
9	RESET#	Input	Can be used by an external device to reset VNC1L. This pin can be used in combination with PROG# and the UART interface to program firmware into VNC1L. If not required pull-up to VCC via a 47kΩ resistor.*
10	PROG#	Input	This pin is used in combination with the RESET# pin and the UART interface to program firmware into VNC1L.*

Table 3.3 Miscellaneous Signal Group

* These pins are pulled to VCC via internal 200kΩ resistors.

Pin No.	Name	Type	Description	Combined Interface Mode			
				UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
11	BDBUS0	I/O	5V safe bidirectional data/control bus, BD bit 0				PortBD0
12	BDBUS1	I/O	5V safe bidirectional data/control bus, BD bit 1				PortBD1
13	BDBUS2	I/O	5V safe bidirectional data/control bus, BD bit 2				PortBD2
14	BDBUS3	I/O	5V safe bidirectional data/control bus, BD bit 3				PortBD3

Pin No.	Name	Type	Description	Combined Interface Mode			
				UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
15	BDBUS4	I/O	5V safe bidirectional data/control bus, BD bit 4				PortBD4
16	BDBUS5	I/O	5V safe bidirectional data/control bus, BD bit 5				PortBD5
18	BDBUS6	I/O	5V safe bidirectional data/control bus, BD bit 6				PortBD6
19	BDBUS7	I/O	5V safe bidirectional data/control bus, BD bit 7				PortBD7
20	BCBUS0	I/O	5V safe bidirectional data/control bus, BC bit 0				PortBC0
21	BCBUS1	I/O	5V safe bidirectional data/control bus, BC bit 1				PortBC1
22	BCBUS2	I/O	5V safe bidirectional data/control bus, BC bit 2				PortBC2
23	BCBUS3	I/O	5V safe bidirectional data/control bus, BC bit 3				PortBC3
31	ADBUS0	I/O	5V safe bidirectional data/control bus, AD bit 0	TXD	D0	SCLK	PortAD0
32	ADBUS1	I/O	5V safe bidirectional data/control bus, AD bit 1	RXD	D1	SDI	PortAD1
33	ADBUS2	I/O	5V safe bidirectional data/control bus, AD bit 2	RTS#	D2	SDO	PortAD2
34	ADBUS3	I/O	5V safe bidirectional data/control bus, AD bit 3	CTS#	D3	CS	PortAD3
35	ADBUS4	I/O	5V safe bidirectional data/control bus, AD bit 4	DTR# (DATAACK#)	D4	Not Available	PortAD4
36	ADBUS5	I/O	5V safe bidirectional data/control bus, AD bit 5	DSR# (DATAREQ#)	D5		PortAD5
37	ADBUS6	I/O	5V safe bidirectional data/control bus, AD bit 6	DCD#	D6		PortAD6
38	ADBUS7	I/O	5V safe bidirectional data/control bus, AD bit 7	RI#	D7		PortAD7
41	ACBUS0	I/O	5V safe bidirectional data/control bus, AC bit 0	TXDEN#	RXF#		PortAC0
42	ACBUS1	I/O	5V safe bidirectional data/control bus, AC bit 1		TXE#		PortAC1

Pin No.	Name	Type	Description	Combined Interface Mode			
				UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
43	ACBUS2	I/O	5V safe bidirectional data/control bus, AC bit 2		RD#		PortAC2
44	ACBUS3	I/O	5V safe bidirectional data/control bus, AC bit 3		WR		PortAC3
45	ACBUS4	I/O	5V safe bidirectional data/control bus, AC bit 4		DATAREQ#	DATAREQ#	PortAC4
46	ACBUS5	I/O	5V safe bidirectional data/control bus, AC bit 5, Interface mode selection pin		DATAACK#	DATAACK#	PortAC5
47	ACBUS6	I/O	5V safe bidirectional data/control bus, AC bit 6, Interface mode selection pin				PortAC6
48	ACBUS7	I/O	5V safe bidirectional data/control bus, AC bit 7. To use a 12MHz crystal with VNC1L fit a 47kΩ pull-down resistor. Alternatively, fitting a 47kΩ pull-up resistor on this pin will switch off the internal clock multiplier, allowing the device to be fed with an external 48MHz clock signal into XTIN				PortAC7

Table 3.4 Data and Control Signals

4 Functional Description

The VNC1L is the first of FTDI's Vinculum family of Embedded USB host controller integrated circuit devices. Vinculum can also encapsulate certain USB device classes handling the USB Host Interface and data transfer functions using the in-built MCU and embedded Flash memory. When interfacing to mass storage devices, such as USB Flash drives, Vinculum transparently handles the FAT File Structure using a simple to implement command set. Vinculum provides a cost effective solution for introducing USB host capability into products that previously did not have the hardware resources to do so.

The VNC1L has a Combined Interface which interfaces a controlling application with the Command Monitor. The combined interfaces are UART, Parallel FIFO and SPI.

The VNC1L is supplied un-programmed. It can be programmed before assembly or it can be configured "in the field" with configuration option firmware available from the Vinculum website at http://www.ftdichip.com.

4.1 Key Features

The VNC1L has the following key features:

- Two independent USB Host ports.
- 8 or 32-bit V-MCU Core.
- Dual DMA controllers for hardware acceleration.
- 64k Embedded Flash Program Memory.
- 4k internal Data SRAM.
- 2 x USB 2.0 Slow speed or Full speed Host or Slave ports.
- Automatic Low or Full Speed selection.
- UART, SPI and Parallel FIFO interfaces.
- Up to 28 GPIO pins depending on configuration.
- Low power operation (25mA running/2mA standby).
- FTDI firmware easily updated in the field.
- Multi-processor configuration capable.

4.2 Functional Block Descriptions

The following paragraphs detail each function within VNC1L. Please refer to the block diagram shown in **Figure 2.1**.

USB Transceivers 1 and 2 - The two USB transceiver cells provide the physical USB device interface supporting USB 1.1 and USB 2.0 standards. Low-speed and full-speed USB data rates are supported. Each output driver provides +3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB DATA IN, SE0 and USB Reset condition detection. These cells also include integrated internal USB pull-up or pull-down resistors as required for host or slave mode.

USB Serial Interface Engine (SIE) - These blocks handle the parallel to serial and serial to parallel conversion of the USB physical layer. This includes bit stuffing packets, CRC generation, USB frame generation and protocol error checking.

12 MHz Oscillator - The 12MHz Oscillator cell generates a 12MHz reference clock input to the Clock Multiplier PLL from an external 12MHz crystal.

Clock Multiplier PLL - The Clock Multiplier PLL takes the 12MHz input from the Oscillator Cell and generates 24MHz and 48MHz reference clock signals, which are required by the USB SIE Blocks, the MCU core, System Timer and UART prescalar blocks.

Program and Test Logic - This block provides a means of programming the onboard E-FLASH memory. When PROG# is pulled low and the device is reset by pulsing the #RESET low, the onboard E-FLASH memory is bypassed by an internal hard-coded bootstrap Loader ROM which contains code to allow the E-FLASH memory to be programmed via commands to the UART interface. FTDI provides a software utility

which allows VNC1L to be programmed using this method. The TEST pin is used in manufacturing to enhance the testability of the various internal blocks and should be tied to GND.

DMA Controller 1 and 2 - The twin DMA controllers in VNC1L greatly enhance performance by allowing data from the two USB SIE controllers, UART, FIFO and SPI interfaces to be transferred between each other via the data SRAM with minimal MCU intervention.

Data SRAM - This 4k x 8bit block acts as the data (variable) memory for the Vinculum MCU, though it can also be accessed transparently to the MCU by the twin DMA controllers.

NPU (Numeric Co-processor) – Operations which extensively utilise 32-bit arithmetic, such as calculations relating to the FAT file system, are enhanced by the 32-bit co-processor block.

UART Prescaler - This block provides the master transmit/receive clock for the UART block. By varying the prescaler value, the baud rate of the UART can be adjusted over a range of 300baud to 1Mbaud.

System Timer - The system timer provides a regular interrupt to VNC1L firmware.

Vinculum MCU Core – Processor core based on FTDI's proprietary 8-bit embedded MCU architecture. VMCU has a Harvard architecture i.e. separate code and data space. It supports 64k bytes of program code, 64k bytes of (paged) data space and 256 bytes of I/O space and uses "enhanced CISC" technology. Typically VMCU instructions replace several lines of code in conventional CISC or RISC processors giving RISC like performance in CISC architecture with the advantage over both of excellent code compression in the program ROM space.

E-FLASH Program ROM - The VNCL1L has 64k bytes of embedded Flash (E-FLASH) memory. No special programming voltages are necessary for programming the onboard E-FLASH as these are provided internally on-chip. VNC1L devices are supplied blank and require to be initially programmed using the Bootstrap Loader.

Bootstrap Loader ROM - This is a small block of hard-coded ROM (512 x 8 bits) which bypasses the main E-FLASH memory when PROG# is pulled low. This provides a means of programming the entire E-FLASH memory via the UART interface. A blank device must be programmed with the Bootstrap Loader via the UART interface. A device already programmed may be upgraded via either the UART interface or the USB interface.

UART and FIFO Logic - Optional serial and parallel interfaces to VNC1L that are equivalent to the interfaces on FTDI's FT232 and FT245 ICs.

GPIO Blocks - General purpose I/O pins. Not all I/O pins are available to the user for a particular configuration. Restrictions on use are shown in Table 3.4.

4.3 Programming VNC1L

The VNC1L is shipped as a blank device. It must be programmed (when in bootloader mode) with firmware before use. It can be programmed either pre-assembly, using the VPROG-1 stand alone programmer or programmed in-circuit via the UART interface.

The VNC1L bootloader uses the UART interface to load new firmware into the Vinculum Flash memory. To enable the bootloader, the PROG# pin must be driven low and VNC1L must then be reset by driving the RESET# pin low then high. Run mode can be enabled by driving the PROG# pin high and then resetting VNC1L by driving the RESET# pin low then high.

When VNC1L firmware is updated via a microcontroller with a UART, the microcontroller must be capable of at least 115200 baud.

The firmware can be upgraded in to the Flash memory via the UART interface or via a USB interface.

Examples of how to connect VNC1L in each of these modes is given in http://www.ftdichip.com

5 Firmware Control Interface

There are three firmware interface options for the command monitor on the combined control and data interface. The command monitor interface options are UART, FIFO or SPI. The mode of operation is selected using VNC1L pins 46 and 47.The pin connections used to select the mode of the interface are shown in **Table 5.1**:

Pin No.		Mode
47 (ACBUS6)	46 (ACBUS5)	
Pull-Up	Pull-Up	UART
Pull-Up	Pull-Down	SPI
Pull-Down	Pull-Up	FIFO
Pull-Down	Pull-Down	UART

Table 5.1 Combined Interface Selection

Important : Pins ACBUS5 and ACBUS6 should not be tied directly to GND or VCC.

Pins ACBUS5 and ACBUS6 should be pulled high or low using a resistor of around 47kΩ. These pins are read only at reset, but may then become outputs after the interface choice has been selected. When FIFO mode is selected ACBUS5 will be used as an output by VNC1L Firmware.

5.1 UART Interface

When the data and control buses are configured in UART mode, the interface implements a standard asynchronous serial UART port with flow control. The UART can support baud rates from 300baud to 1Mbaud.
Data transfer uses NRZ (Non-Return to Zero) data format consisting of 1 start bit, 7 or 8 data bits, an optional parity bit, and one or two stop bits. When transmitting the data bits, the least significant bit is transmitted first. Transmit and receive waveforms are illustrated in Figure 5.1 and Figure 5.2:

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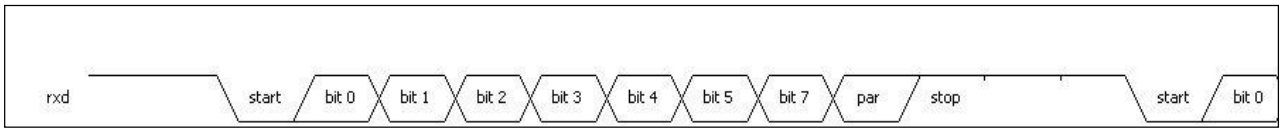

Figure 5.1 UART Receive Waveform

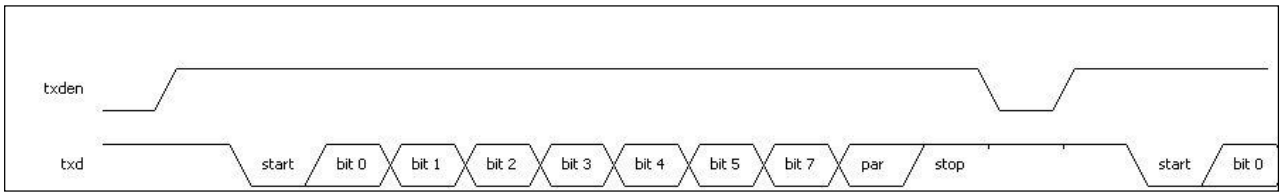

Figure 5.2 UART Transmit Waveform

Baud rate (default =9600 baud), flow control settings (default = RTS/CTS), number of data bits (default=8), parity (default is no parity) and number of stop bits (default=1) are all configurable using the firmware command interface. Please refer to http://www.ftdichip.com (or latest version).

5.1.1 UART Mode Signal Descriptions

Pin No.	Name	Type	Description
31	TXD	Output	Transmit asynchronous data output
32	RXD	Input	Receive asynchronous data input
33	RTS#	Output	Request To Send Control Output
34	CTS#	Input	Clear To Send Control Input
35	DATAACK#	Output	Data Acknowledge (Data Terminal Ready Control) Output
36	DATAREQ#	Input	Data Request (Data Set Ready Control) Input
37	DCD#	Input	Data Carrier Detect Control Input
38	RI#	Input	Ring Indicator Control Input. RI# low can be used to resume the PC USB Host controller from suspend.
41	TXDEN	Output	Enable Transmit Data for RS485 designs

Table 5.2 Data and Control Bus Signal Mode Options - UART Interface

In RS485 designs, a transmit data enable signal, TXDEN, may be used to signal that a transmit operation is in progress. TXDEN will be set high one bit-time before data is transmitted and return low one bit time after the last bit of a data frame has been transmitted.

The ring indicator pin, RI#, is used to wake up VNC1L from suspend mode. The suspend mode can be entered using a firmware monitor command.

5.2 SPI Interface

When the data and control buses are configured in SPI mode, the interface operates as an SPI Slave. An SPI master is required to provide the clock (SCLK) signal and set the chip select (CS) for the duration of the transaction. The SPI interface is a polled 4-wire interface which can operate at speeds up to 12MHz

The SPI interface differs from most other implementations in that it uses a 13 clock sequence to transfer a single byte of data. In addition to a 'Start' state, the SPI master must send two setup bits which indicate data direction and target address. The encoding of the setup bits is shown in Table 5.3. A single data byte is transmitted in each SPI transaction, with the most significant bit transmitted first.

After each transaction VNC1L returns a single status bit. This indicates if a Data Write was successful or a Data Read was valid.

Direction (R/W)	Target Address	Operation	Meaning
1	0	Data Read	Retrieve byte from Transmit Buffer
1	1	Status Read	Read SPI Interface Status
0	0	Data Write	Add byte to Receive Buffer
0	1	N/A	N/A

Table 5.3 SPI Setup Bit Encoding

5.2.1 Signal Descriptions

Pin No.	Name	Type	Description
31	SCLK	Input	SPI Clock input
32	SDI	Input	SPI Serial Data Input
33	SDO	Output	SPI Serial Data Output
34	CS	Input	SPI Chip Select Input

Table 5.4 Data and Control Bus Signal Mode Options - SPI Interface

The VNC1L SPI interface uses 4 signal lines: SCLK, CS, SDI and SDO. **The signals SDI, SDO and CS are always clocked on the rising edge of the SCLK signal.**

CS signal must be raised high for the duration of the entire transaction. For data transactions, the CS must be released for at least one clock cycle after a transaction has completed. It is not necessary to release CS between Status Read operations.

The 'Start' state of SDI and CS high on the rising edge of SCLK initiates the transfer. The transfer finishes after 13 clock cycles, and the next transfer starts when SDI is high during the rising edge of SCLK. The following **Figure 5.3** and **Table 5.5** give details of the bus timing requirements.

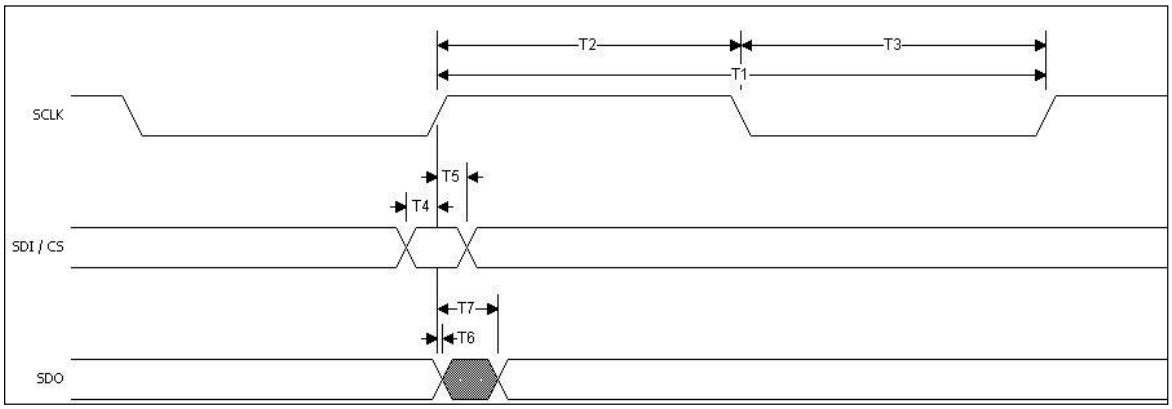

Figure 5.3 SPI Slave Mode Timing

Time	Description	Minimum	Typical	Maximum	Unit
T1	SCLK Period	83	-	-	ns
T2	SCLK High	20	-	-	ns
T3	SCLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold Time	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 5.5 SPI Slave Data Timing

5.2.2 SPI Master Data Read Transaction

The SPI master must periodically poll for new data in VNC1L Transmit Buffer. It is recommended that this is done first before sending any command.

The Start and Setup sequence is sent to VNC1L by the SPI master, see Figure 5.4.

The VNC1L clocks out data from its Transmit Buffer on subsequent rising edge clock cycles provided by the SPI master. This is followed by a status bit generated by VNC1L. The Data Read status bit is defined in Table 5.6.

If the status bit indicates New Data then the byte received is valid. If it indicates Old Data then the Transmit Buffer in VNC1L is empty and the byte of data received in the current transaction should be disregarded.

Status Bit	Meaning	
0	New Data	Data in current transaction is valid data. Byte removed from Transmit Buffer.
1	Old Data	This same data has been read in a previous read cycle. Repeat the read cycle until New Data is received.

Table 5.6 SPI Master Data Read Status Bit

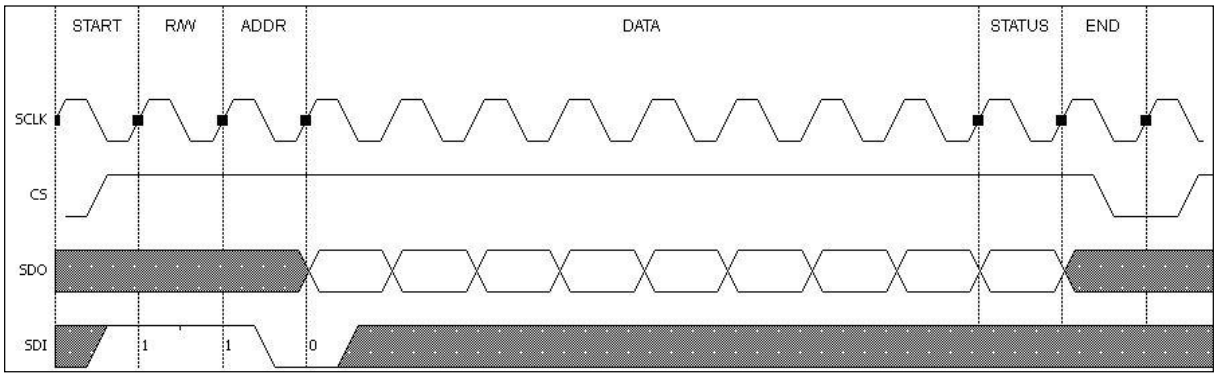

Figure 5.4 SPI Master Data Read (VNC1L Slave Mode)

The status bit is only valid until the next rising edge of SCLK after the last data bit.

During the Data Read operation the CS signal must not be de-asserted.

The transfer completes after 13 clock cycles and the next transfer can begin when SDI and CS are high during the rising edge of SCLK.

5.2.3 SPI Master Data Transaction

During an SPI master Data Write operation the Start and Setup sequence is sent by the SPI master to VNC1L, see Figure 5.5. This is followed by the SPI master transmitting each bit of the data to be written to VNC1L. The VNC1L then responds with a status bit on SDO on the rising edge of the next clock cycle.

The SPI master must read the status bit at the end of each write transaction to determine if the data was written successfully to VNC1L Receive Buffer. The Data Write status bit is defined in Table 5.7. The status bit is only valid until the next rising edge of SCLK after the last data bit.

If the status bit indicates Accept then the byte transmitted has been added to VNC1L Receive Buffer. If it shows Reject then the Receive Buffer is full and the byte of data transmitted in the current transaction should be re-transmitted by the SPI master to VNC1L.

Any application should poll VNC1L Receive Buffer by retrying the Data Write operation until the data is accepted.

Status Bit	Meaning	
0	Accept	Data from the current transaction was accepted and added to the Receive Buffer
1	Reject	Write data was not accepted. Retry the same write cycle.

Table 5.7 SPI Master Data Write Status Bit

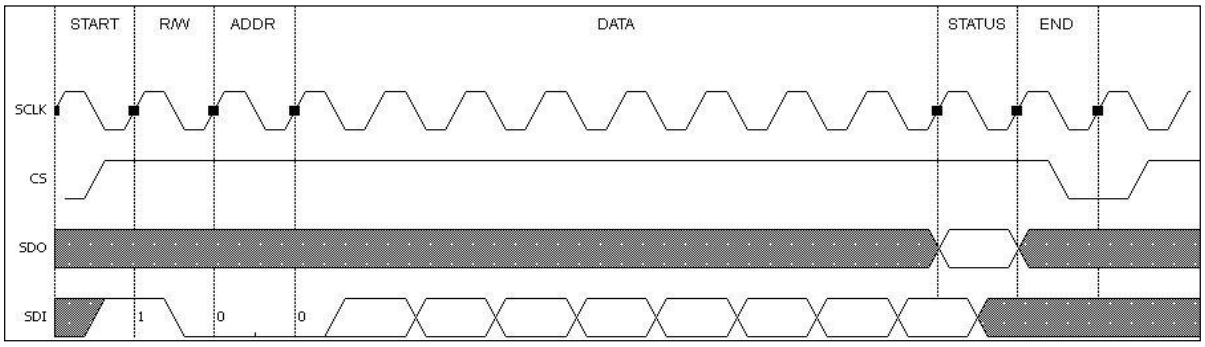

Figure 5.5 SPI Slave Mode Data Write

5.2.4 SPI Master Status Read Transaction

The VNC1L has a status byte which determines the state of the Receive and Transmit Buffers. The SPI master must poll VNC1L and read the status byte.

The Start and Setup sequence is sent to VNC1L by the SPI master, see Figure 5.6. The VNC1L clocks out its status byte on subsequent rising edge clock cycles from the SPI master. This is followed by a status bit generated by VNC1L (also on the SDO) which will always be zero (indicating new data).

The meaning of the bits within the status byte sent by VNC1L during a Status Read operation is described in Table 5.8.

The result of the Status Read transaction is only valid during the transaction itself.

Data read and data write transactions must still check the status bit during a Data Read or Data Write cycle regardless of the result of a Status Read operation.

Bit	Description	Description
0	RXF#	Receive Buffer Full
1	TXE#	Transmit Buffer Empty
2	-	
3	-	
4	RXF IRQEn	Receive Buffer Full Interrupt Enable
5	TXE IRQEn	Transmit Buffer Empty Interrupt Enable
6	-	
7	-	

Table 5.8 SPI Status Read Byte – bit descriptions.

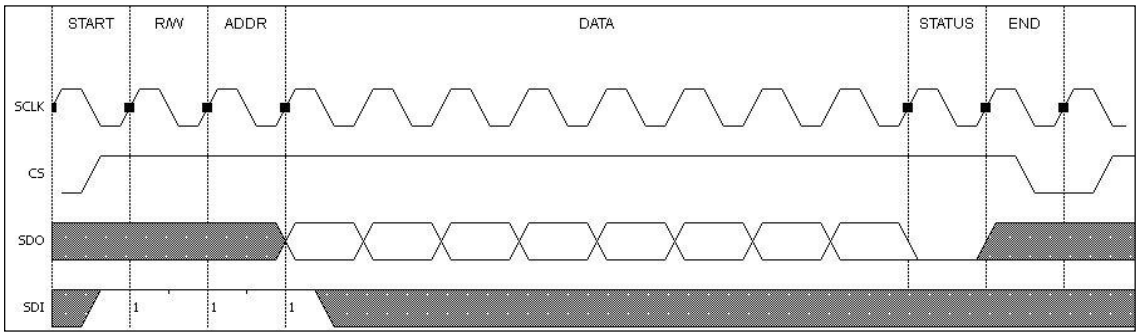

Figure 5.6 SPI Slave Mode Status Read

5.3 Parallel FIFO Interface

When VNC1L data and control buses are configured in the parallel FIFO interface mode, then it is functionally equivalent to FTDI FT245R and FT245B devices.

5.3.1 Signal Descriptions

The Parallel FIFO interface signals are described in Table 5.9.

Pin No.	Name	Type	Description
31	D0	I/O	FIFO Data Bus Bit 0
32	D1	I/O	FIFO Data Bus Bit 1
33	D2	I/O	FIFO Data Bus Bit 2
34	D3	I/O	FIFO Data Bus Bit 3
35	D4	I/O	FIFO Data Bus Bit 4
36	D5	I/O	FIFO Data Bus Bit 5
37	D6	I/O	FIFO Data Bus Bit 6
38	D7	I/O	FIFO Data Bus Bit 7
41	RXF#	Output	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high.
42	TXE#	Output	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low.
43	RD#	Input	Enables the current FIFO data byte on D0...D7 when low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low
44	WR	Input	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low.

Table 5.9 Data and Control Bus Signal Mode Options - Parallel FIFO Interface

5.3.2 Read Transaction

When in parallel FIFO interface mode, the timing of a read operation on the FIFO interface is shown in Figure 5.7 and Table 5.10.

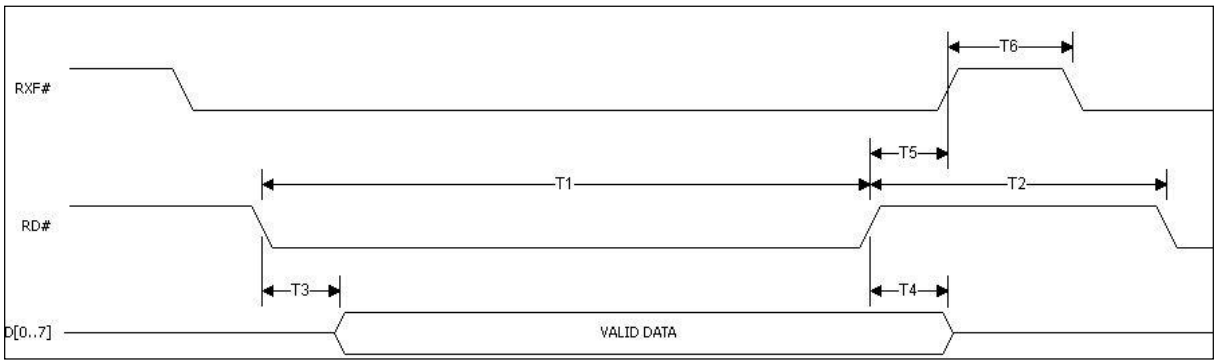

Figure 5.7 FIFO Read Cycle

Time	Description	Minimum	Maximum	Unit
T1	RD Active Pulse Width	50	-	ns
T2	RD to RD Pre-Charge Time	50 + T6	-	ns
T3	RD Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD Inactive*	0	-	ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive After RD Cycle	80	-	ns

Table 5.10 FIFO Read Cycle Timings

*Load = 30pF

5.3.3 Write Transaction

When in parallel FIFO interface mode, the timing of a write operation on the FIFO interface is shown in Figure 5.8 and Table 5.11.

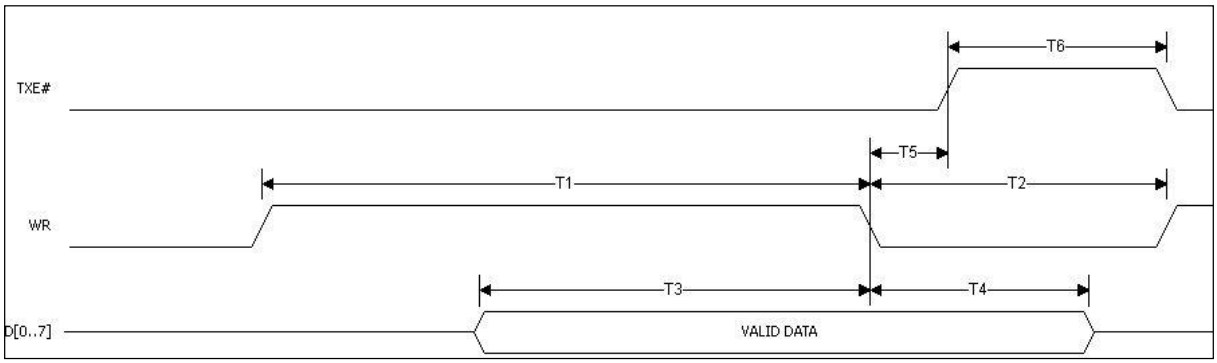

Figure 5.8 FIFO Write Cycle

Time	Description	Minimum	Maximum	Unit
T1	WR Active Pulse Width	50	-	ns
T2	WR to RD Pre-Charge Time	50	-	ns
T3	Data Setup Time before WR Inactive	20	-	ns
T4	Data Hold Time from WR Inactive	0	-	ns
T5	WR Inactive to TXE#	5	25	ns
T6	TXE Inactive After WR Cycle	80	-	ns

Table 5.11 FIFO Write Cycle Timings

6 Device Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for VNC1L are shown in Table 6.1. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C.
Vcc Supply Voltage	0 to +3.6	V
DC Input Voltage - USBDP and USBDM	-0.5 to +(Vcc +0.5)	V
DC Input Voltage - High Impedance Bidirectionals	-0.5 to +5.00	V
DC Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
DC Output Current - Outputs	8	mA
DC Output Current - Low Impedance Bidirectionals	8	mA
Power Dissipation (Vcc = 3.6V)	250	mW

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

6.2 DC Characteristics

DC Characteristics (Ambient Temperature -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3	3.3	3.6	V	
Vcc2	VCCIO Operating Supply Voltage	3	3.3	3.6	V	
Icc1	Operating Supply Current	-	25	-	mA	Normal Operation
Icc2	Operating Supply Current	1.0		2.0	mA	USB Suspend

Table 6.2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	Vcc-0.4		3.6	V	I source = 8mA
Vol	Output Voltage Low			0.4	V	I sink = 8mA
Vin	Input Switching Threshold	0.8	1.4	2.0	V	

Table 6.3 UART and CBUS I/O Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vin	Input Switching Threshold	0.8	1.4	2.0	V	

Table 6.4 RESET# and PROG# Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	
UVol	I/O Pins Static Output (Low)	0		0.3	V	
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVdif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	28		44	Ohms	**

Table 6.5 USB I/O Pin (USBDP, USBDM) Characteristics

** Driver Output Impedance includes the external USB series resistors on USBDP and USBDM pins.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High		0.6		V	Fosc = 12MHz
Vol	Output Voltage Low		0.2		V	Fosc = 12MHz
Vin	Input Switching Threshold		0.4		V	

Table 6.6 XTIN, XOUT Pin Characteristics

7 Application Examples

7.1 Example VNC1L Schematic (MCU – UART Interface)

VNC1L can be configured to communicate with a microcontroller using a UART interface. An example of this is shown in Figure 7.1.

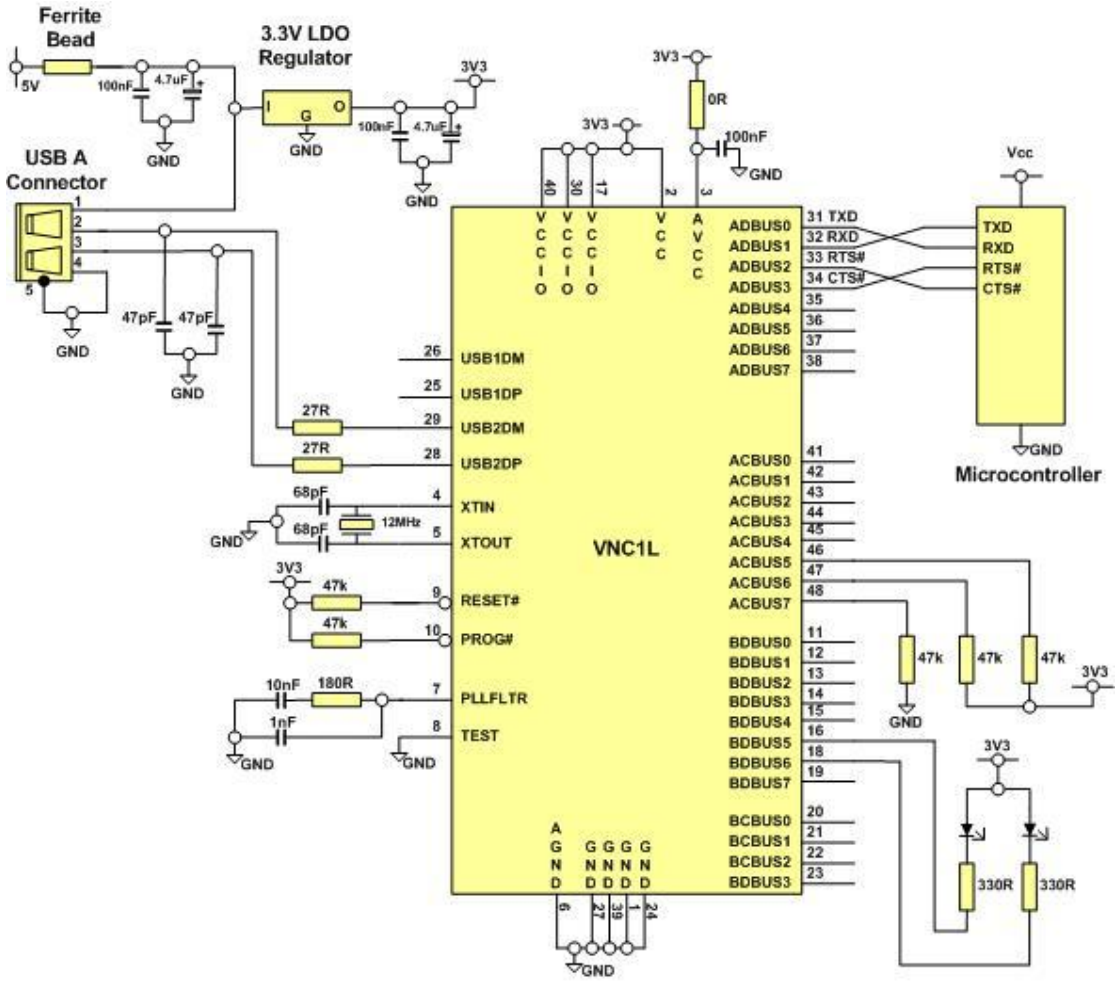

Figure 7.1 VNC1L Schematic (MCU - UART Interface)

Notes:

1. It is recommended that 68pF loading capacitors are used with the 12MHz oscillator.
2. VNC1L is shipped as a blank device. Initial in-circuit programming (using the downloaded ***.rom*** file) can only be done via the UART interface.
3. When in bootstrap mode (PROG# is low and RESET# toggled) then ACBUS5 and ACBUS6 are ignored and the device is forced into UART mode.
4. VNC1L can also be programmed, pre-assembly, using the VPROG1 VNC1L stand-alone programmer – see http://www.ftdichip.com

7.2 Block Diagram - VNC1L Programming Via USB Interface

VNC1L can be programmed from a PC USB port using an FTDI USB-serial converter such as the FT232R. This is the fastest way to reprogram VNC1L Flash memory as data can be transferred to VNC1L at up to 1MBaud.

The required connections between VNC1L and an FT232R device for controlling the PROG# and RESET# pins is shown in Figure 7.2.

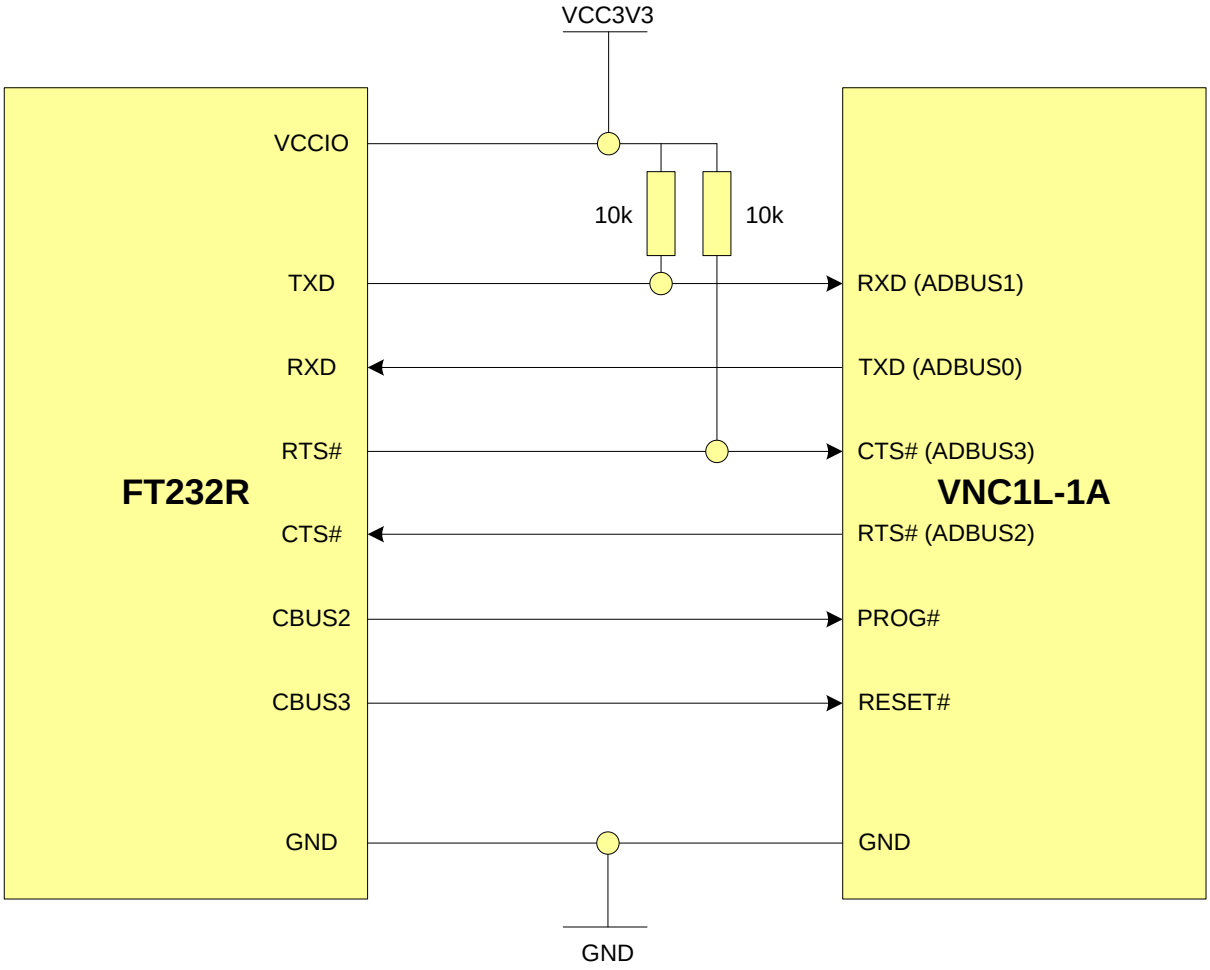

Figure 7.2 VNC1L –Block Diagram of Programming Using USB Connection

Note that CBUS Bit Bang mode must be enabled in the FT232R EEPROM for CBUS2 and CBUS3 to enable this operation. See FTDI application note "AN232R-01 Bit Bang Modes for the FT232R and FT245R" for details of how to use CBUS Bit Bang mode. This is available at **http://www.ftdichip.com**).

To enable the bootloader, the PROG# pin must be held low and the RESET# pin must be pulsed low then high again (this resets VNC1L).

Run mode can be enabled by driving the PROG# pin high and then resetting VNC1L by driving the RESET# pin low then high.

For further examples of connecting VNC1L for programming, please refer to http://www.ftdichip.com

8 Package Parameters

8.1 LQFP-48 Dimensions

VNC1L is supplied in a RoHS Compliant 48 pin LQFP package as standard.

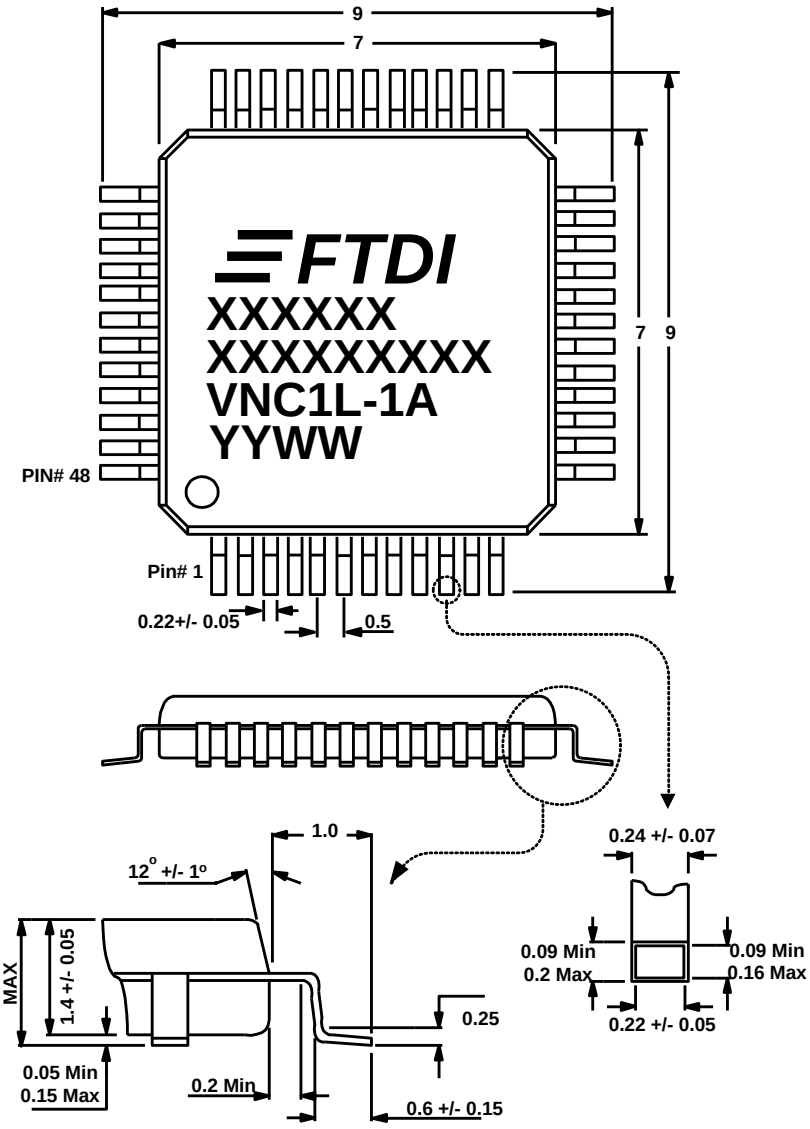

Figure 8.1 LQFP-48 Package Dimensions

The LQFP-48 package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC. This package has a 7.00mm x 7.00mm body (9.00 mm x 9.00 mm including pins). The pins are on a 0.50 mm pitch. The mechanical drawing in Figure 8.1 shows the LQFP-48 package – all dimensions are in millimetres.

The date code format is YYWW where WW = 2 digit week number, YY = 2 digit year number.

An alternative 6mm x 6mm leadless QFN package is also available for projects where PCB area is critical. Contact FTDI for availability.

8.2 Solder Reflow Profile

The recommended solder reflow profile is shown in Figure 8.2.

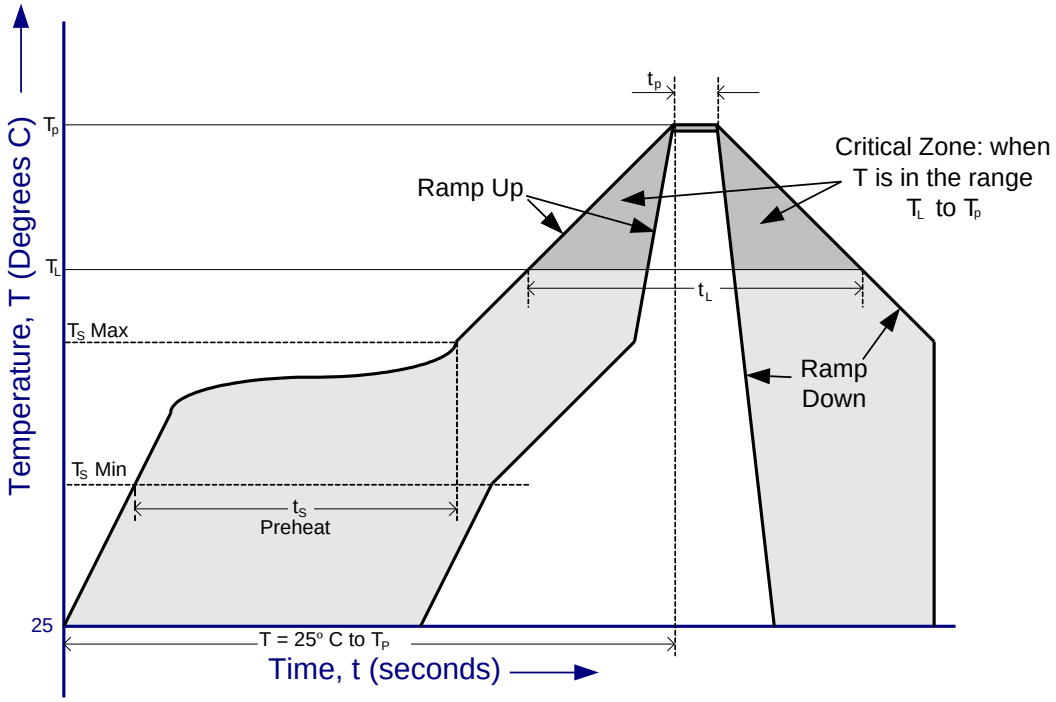

Figure 8.2 VNC1L Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 8.1. Values are shown for both a completely Pb free solder process (i.e. VNC1L is used with Pb free solder) and for a non-Pb free solder process (i.e. VNC1L is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / second Max.
Preheat - Temperature Min (T_S Min.) - Temperature Max (T_S Max.) - Time (t_S Min to t_S Max)	 150°C 200°C 60 to 180 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_P)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_P)	20 to 40 seconds	10 to 30 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 8.1 Reflow Profile Parameter Value

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Appendix B - Revision History

Revision History

Version 0.90	Initial Datasheet Created	July 2006
Version 0.95	Datasheet Update	September 2006
Version 0.96	Datasheet Update	March 2007
Version 0.97	Update Table 5	June 2007
Version 0.98	Layout Update	October 2007
Version 0.99	Datasheet Update	May 2008
Version 1.00	Datasheet Update	May 2008
Version 2.00	Increased temperature range, reformatted + minor edits.	August 2008
Version 2.01	Corrected LED connection in Fig 7.1.	
	Corrected XTIN description.	
	Updated company address info.	11th May 2009
Version 2.02	Update table 3.4, pin 35 and 36.	
	Replaced DATAACK# with DTR# and	
	Replaced DATAREQ# with DSR#	23rd August 2010